18.3 A 10Gb/s Eye-Opening Monitor in 0.13μm CMOS

Behnam Analui[1], Alexander Rylyakov[2], Sergey Rylov[2], Mounir Meghelli[2], Ali Hajimiri[1]

[1]California Institute of Technology, Pasadena, CA
[2]IBM, Yorktown Heights, NY

The channel-imposed degradation of signal quality in high-speed links can be compensated by an equalizer [1]. In an adaptive equalizer, a feedback mechanism is required to measure and report the eye quality at the equalizer output. An eye-opening monitor (EOM) is a circuit block that periodically reports a quantitative measure of the quality of the signal eye that it is sampling [2].

In this paper, an EOM circuit architecture that maps both the vertical and horizontal opening of the received eye to a two-dimensional error diagram is proposed. The error diagram is directly correlated to the eye opening in both dimensions. It contains information about the shape of the eye and serves as the cost function for updating the equalizer coefficients. The EOM circuit overlaps a rectangular mask with the received signal eye. Any data transition passing inside the mask is counted as an error. The area of the mask is swept in horizontal and vertical dimensions independently. The error diagram is generated by recording the error count for different mask geometries. The operation is illustrated in Fig. 18.3.1 for one mask size. An error is flagged when a transition crosses either of the two vertical sides of the mask. Two reference voltages, V_H and V_L, define the vertical opening of the mask and two phases of the sampling clock, ϕ_{early} and ϕ_{late}, determine its horizontal opening. Data is continuously compared with V_H and V_L and the results are sampled at early and late phases.

Figure 18.3.2 shows the architecture of the EOM circuit. An external full-rate clock is divided by two to generate I and Q phases. Two phase rotators interpolate between I and Q and between $\overline{I}$ and Q to create respectively early and late phases. Therefore, the output phase of each rotator covers half of the bit period. Each rotator has a 15b thermometer-encoded control line that results in a phase step of 6°. When both sets of control bits are zero, ϕ_{early} and ϕ_{late} are in phase with Q and overlap in the center of the eye. Every positive edge on $next\_\phi_{early}$ moves ϕ_{early} one step to the left. Similarly, every positive edge on $next\_\phi_{late}$ moves ϕ_{late} one step to the right. The 16th positive edge on either $next\_\phi_{early}$ or $next\_\phi_{late}$ automatically resets the phase to the center position. The D-flip flops (DFF) sample the comparators' outputs at both ϕ_{early} and ϕ_{late}. As the sampling clocks are half-rate, each DFF block consists of two DFFs to sample at both rising and falling edges of the clocks. This avoids skipping any data transition.

Processing the errors caused by early and late samples separately allows the EOM to differentiate data transitions that cross the left of the eye mask from those that cross the right side and enables it to capture asymmetrical eye diagrams. The final error output passes through a digital divider with four selectable divide ratios. A larger divide ratio is selected in order to measure cases with high error counts.

The comparator circuits use a differential CML topology, as shown in Fig. 18.3.3. The lower comparator reference is generated by swapping V_H and V_L [2]. The reference levels can be adjusted through either an off-chip signal or an on-chip DAC. The DAC sets $V_H = V_{cm} + n\Delta V$ and $V_L = V_{cm} - n\Delta V$, where V_{cm} is input common mode and $1 \le n \le 7$. Every positive edge on *next_ref* increases n by one. The eighth edge resets n to 1. The step size, ΔV, is adjustable externally. The phase-rotator circuit consists of two parallel differential stages, as Fig. 18.3.3 shows. The differential control lines, s_0-s_{15}, steer the tail current between the two stages to adjust the input phases weights and thus generate the proper interpolated output phase.

To quantitatively compare received eye qualities, a mask error rate (MER) for a given mask is defined. MER is the ratio of the number of transitions falling inside the given mask to the total number of transitions. MER for a given mask increases as the quality of the monitored eye degrades. Masks of different shape may have the same MER. The combined area inside the eye that covers all the masks with the same MER is defined as the effective *eye opening* for the given MER. This effective eye opening contains information about the shape of the eye and is not necessarily rectangular. The proposed EOM circuit measures the effective eye opening for different MER values. By separately stepping the $next\_\phi_{early}$, $next\_\phi_{late}$, and *next_ref* signals, the architecture provides three degrees of freedom for getting several mask sizes. Seven settings for the differential reference voltage DAC and 15 for each phase rotator provide 210 different masks. The number of masks can be increased by applying reference voltages directly from off-chip sources with smaller step size.

The EOM circuit is implemented in a 0.13μm standard CMOS technology. On-wafer measurements from 1 to 12.5Gb/s with a 2^{31}-1 PRBS source and 1.2V supply shows successful error-diagram measurement. The EOM operates reliably even at severe conditions when a closed eye with 10^{-2} BER is applied to the input. It consumes about 275mA from a 1.2V supply and is functional at 10Gb/s with supply voltage as low as 1V. Figure 18.3.4 shows the *error_out* signal when a 10Gb/s signal with 41ps peak-to-peak sinusoidal jitter (SJ) is applied to the input and both $next\_\phi_{early}$ and $next\_\phi_{late}$ are stepped at about 3MHz. The mask vertical opening is 120mV. There is an error-free region (no toggle) for a small mask opening but as the mask gets wider the zoomed *error_out* signal depicts that the error frequency gradually increases. The periodic behavior of the *error_out* signal is due to the self-resetting mechanism of the phases. Figure 18.3.5 is the measured eye opening at three different MER when various amounts of SJ is added to the 10Gb/s, 2^{31}-1 PRBS input. As expected, the measured eye opening monotonically decreases as jitter closes the eye.

Figure 18.3.6 illustrates the two-dimensional error diagram that is generated by measuring the frequency of the *error_out* signal for various mask sizes. Computer-controlled reference voltages and trigger signals for $next\_\phi_{early}$ and $next\_\phi_{late}$ automatically sweep mask sizes. Early and late phases are stepped separately resulting in capturing the asymmetrical shape of the eye. The diagram demonstrates about 70dB dynamic range for MER. The die occupies 1.7×1.7mm² as in Fig. 18.3.7. The active area is only 400×660μm².

Acknowledgement:
The authors thank J. Tierno, T. Zwick, M. Beakes, S. Gowda, D. Friedman, M. Soyuer and M. Oprysko of IBM and J. Ewen of JDSU for technical feedback and support.

References:
[1] H. Wu et al., "Differential 4-tap and 7-tap Transverse Filters in SiGe for 10Gb/s Multimode Fiber Optic Link Equalization," *ISSCC Dig. Tech. Papers*, pp. 180-181, Feb., 2003.
[2] T. Ellermeyer et al., "A 10Gb/s Eye Opening Monitor IC for Decision-Guided Optimization of the Frequency Response of an Optical Receiver," *ISSCC Dig. Tech. Papers*, pp. 50-51, Feb., 2000.

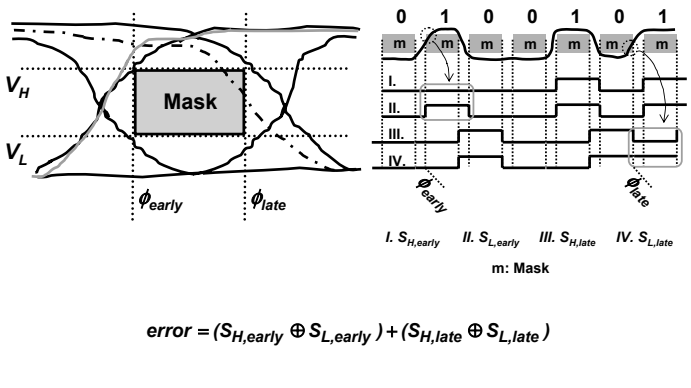

Figure 18.3.1: Eye quality mask and error definition.

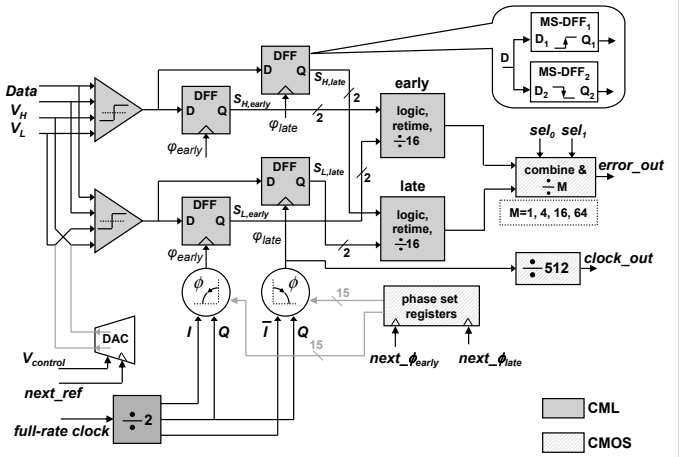

Figure 18.3.2: The EOM circuit architecture.

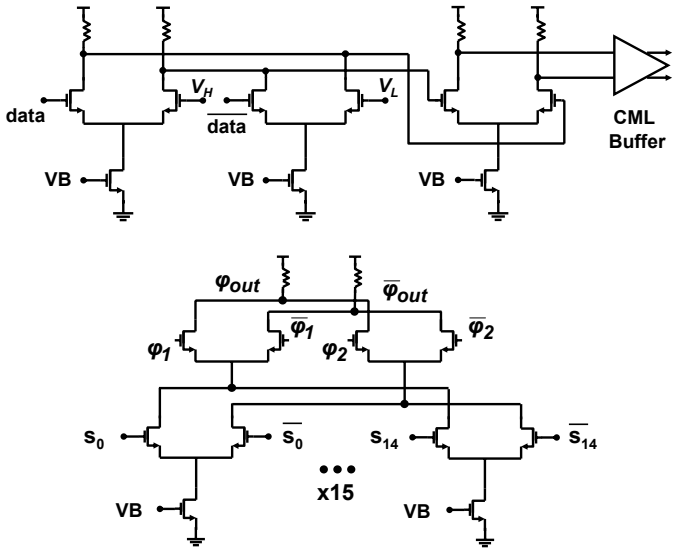

Figure 18.3.3: The comparator (top) and phase rotator (bottom) circuits.

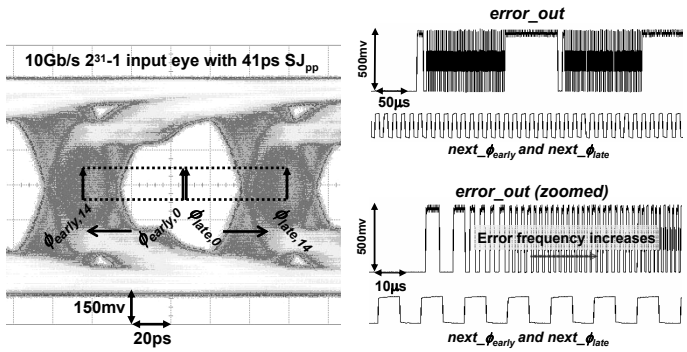

Figure 18.3.4: The *error_out* signal after horizontal mask sweep.

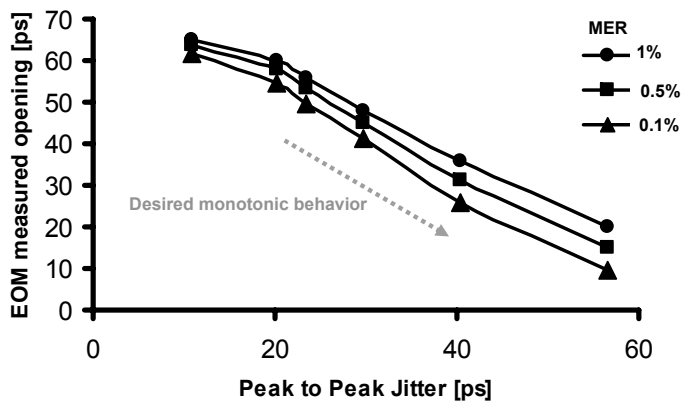

Figure 18.3.5: Measured eye opening for different input jitter levels.

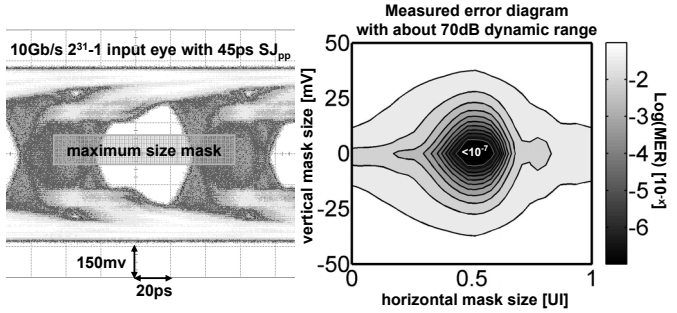

Figure 18.3.6: Measured error diagram.

Continued on Page 602

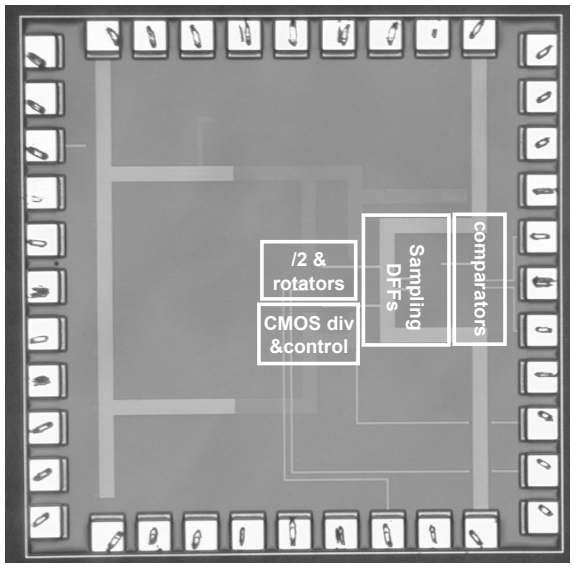

Figure 18.3.7: The EOM die micrograph.

