mm-Wave Phased Arrays in Silicon with Integrated Antennas

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Introduction

In the last few decades the puissant desire to miniaturize the digital circuits to achieve higher speed and larger density has shaped the evolution of the silicon based technologies. This development has not been always beneficial to the analog and RF designers. Although smaller parasitic capacitors and shorter transistor channels have improved f_T and f_{max} of the transistors, extremely thin metal layers, highly doped substrates, and low breakdown voltage transistors have severely affected the performance of analog and RF building blocks. For example, thin metal layers have increased the loss and lowered the quality factor of the building blocks such as capacitors and inductors and low breakdown voltage transistors have made the power generation quite challenging.

Current generations of silicon based technologies, namely, 90nm and 130nm CMOS and 130nm BiCMOS, enable RF designers to demonstrate unprecedented level of integrations at mm-wave frequencies by providing high f_T transistors. Recently, several V- and W-band transceivers and even single-chip phased array systems have been published in the silicon based technologies [1][2]. In most of these works, experimental results prove the accuracy of the lumped element models for transistors, inductors, capacitors and even transmission lines at W-band and above. However, the situation is very different when it comes to integrated antennas. To the best of the authors' knowledge there is no foundry provided models for designing reliable on-chip antennas at this time. At low frequencies (e.g., below 10GHz) large wavelengths compared to the chip dimensions, makes it inefficient to integrate the antennas on the same chip as the transistors and lumped elements due to the large area needed to implement high efficiency antennas. However this may not be a significant problem at mm-wave frequencies as wavelengths become small enough to allow for antenna integration. However, to implement efficient on-chip antennas at these frequencies new problems need to be addressed. For instance, at mm-wave frequencies, high dielectric constant of silicon (ε_r= 11.7), and substrate thickness comparable to the wavelength increases the vulnerability of the antenna performance to the substrate modes [3]. Also the inevitable high doping levels of silicon substrates used to implement the active devices generates a lossy substrate (resistivity of about 10 Ω-cm). In this paper we address these issues and demonstrate the feasibility of the antenna integration on a standard silicon-based technology. Dipole antennas, as well as a four channel phased array transceiver including VCO, dividers and phase shifters, are all implemented on the same

substrate which occupies 6.8mm x 3.8mm. Circuits of the receiver, transmitter, and signal generation blocks are extensively discussed in [1] and [2]. In this paper we focus on the antenna aspects of the design.

Antenna Design Challenges in mm-Wave Frequencies

It is well known that substrate modes can be excited in thick substrates with high dielectric constant. Figure 1 shows the normalized power coupled into substrate modes for a dipole located on a grounded and ungrounded substrates. These values are normalized to the dipole's free space radiated power given by [3]:

$$P_0 = \omega^2 \mu_0^{3/2} \varepsilon_0^{1/2} I^2 d^2 / 12\pi \tag{1}$$

where I is the current, ω is the angular frequency, and d is the effective length of the dipole.
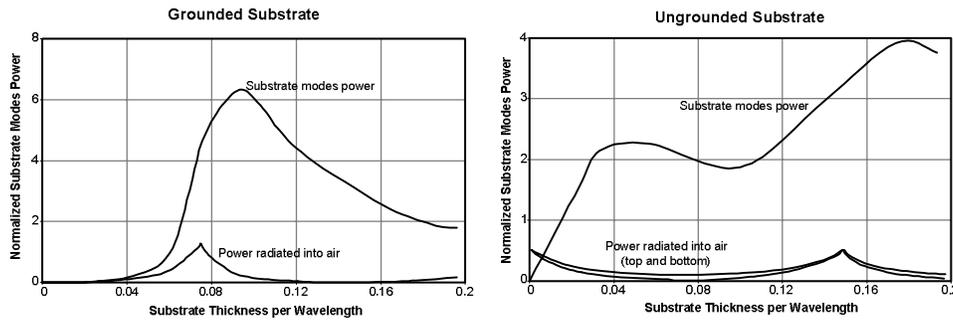
Fig.1) Substrate modes and radiated power for grounded and ungrounded substrates [3]

In the past, several techniques have been used to overcome the substrate modes problem. One of the well known ways to alleviate this problem is using a dielectric lens [3]. A hemispherical lens with the same dielectric constant as silicon's can be utilized to remove these substrate modes and couple the power into air. Also a quarter wavelength matching layer on the lens surface can be used to match the silicon impedance, 110 Ω, to the air's, 377 Ω [3]. This combination of the hemispherical lens and the matching layer mimics a narrow band semi infinite boundary condition for a dipole antenna placed on the air-silicon boundary. Another way to reduce the substrate modes power is exploiting the MEMS technology to remove the lossy silicon substrate underneath the antenna. An example of this can be found in [4]. In our design we have attached a hemispherical silicon lens with diameter of about one inch to the backside of the substrate and radiated from backside as well.

Details of the Design and Measurement

The W-band four channel phased array transceiver [1][2] with integrated dipole antennas are designed in the IBM 8HP 130nm Silicon-Germanium(SiGe) BiCMOS process. Seven metal layers (5 in copper and 2 in aluminum) are

available in this process. The bottom four copper layers have thicknesses of approximately 0.3μm each and the fifth layer is about 0.5μm thick. The top two layers, layers 6 and 7, are made in aluminum and have thickness of about 1.2μm and 4.0μm, respectively. The distance between the bottom layer and the top one is less than 15μm. To minimize the antenna-substrate spacing all eight antennas, four on the RX side and four on the TX side, are implemented in bottom metal layers. To reduce the antenna metal loss, three bottom layers are connected in parallel with vias to form the dipole antennas. On the receiver side, the dipole antennas and pads are connected to the inputs of low noise amplifiers. Pads are used to accurately measure the receiver gain using on-chip probing where the dipole antennas can be disconnected from LNA input by utilizing a laser with micrometer resolution. After measuring the receiver gain with calibrated wafer probes, an unaltered chip is picked and this time the pads are trimmed out with the laser. In this case, only the antennas remain connected to the LNAs input. The chip micrograph and a magnified picture of the layout of the phased array transceiver with integrated antennas and the pads are shown in Figure 2.

To reduce the substrate loss, the fabricated chip is thinned down to 100μm. Due to the layout constraints, antennas are placed at the chip edge and to maintain a uniform dielectric constant substrate underneath the antennas, an undoped silicon slab with the same thickness of silicon chip is abutted to the chip. For mechanical stability, a 500μm silicon wafer is used to hold the chip and the silicon lens is attached to the backside of the undoped wafer. The picture of the prototype is shown in Figure 3. A 2-axis spherical far field measurement technique is utilized to measure the radiation pattern while a W-band horn antenna is used to irradiate the integrated dipoles. The 3-D measured patterns of two middle antennas are shown in Figure 4 where -40°<θ<40° and 0°<φ<180°. In this plot X=Sin(θ)×Cos(φ), Y= Sin(θ)×Sin(φ), and Z=Gain[dB]. Maximum peak gain of about +8dB is achieved in this measurement. As seen in Figure 4 due to the off-axis properties, [5], the peaks of two antennas occur at two different directions. Future work will be focused of modifying the lens and the prototype to achieve broader overlapping patterns.

Conclusion

W-band integrated dipole antennas and a four channel phased transceiver are implemented in IBM 130nm Silicon Germanium BiCMOS process. The chip requires no high frequency electrical connection to the outside world. It includes the complete receiver, transmitter, signal generation blocks, phase shifters [1][2], and on-chip dipole antennas. A hemispherical silicon lens with a diameter of about one inch is used to remove the substrate modes. Receiver gain is measured separately using on-chip probing. A maximum antenna gain of about +8dB is achieved in this measurement.
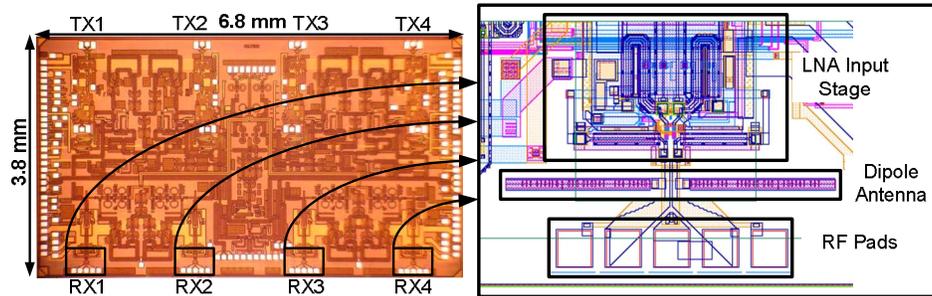
Fig.2) Chip micrograph [1][2] and integrated antennas
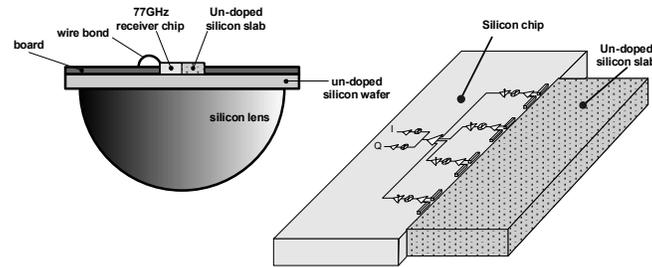
Fig.3) Board Setup Configuration
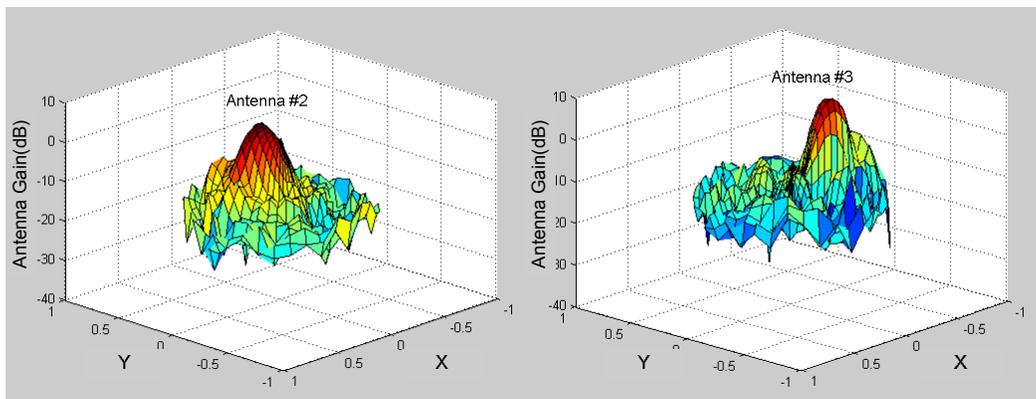
Fig.4) Radiation pattern (X=Sin(θ)×Cos(φ), Y= Sin(θ)×Sin(φ), and Z=Gain[dB])

References

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