10.3 Equalization of IM3 Products in Wideband Direct-Conversion Receivers

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As scaling reduces the breakdown voltage of CMOS devices and as system integration trends demand the further elimination of off-chip components, there arises a great need to improve the linearity of RF receivers. Of particular interest is the direct-conversion architecture, which is currently the workhorse of the mobile telecommunications industry. Although much work has been recently reported in improving the IIP2 of these receivers, the IIP3 requirements still necessitate the use of an inter-stage SAW filter in many applications.

In order to remove the SAW filter and to reduce the linearity requirements of the receiver circuitry, in this paper, an alternate path (AP) in parallel with the main path (MP) is introduced (Fig. 10.3.1). The AP generates IM3 products in the analog domain and downconverts them to baseband (BB) using the same LO signal as the MP. The IM3 products are then digitized and used as inputs to an equalizer that cancels the baseband IM3 products in the MP. This idea has recently been posited in a system-level study [1]; however, the challenges of implementing this system with an integrated RF front-end have not yet been addressed. This solution has the advantages of being both power-efficient and robust. Since the AP must only pass IM3 products, the dynamic ranges of its constituent blocks can be over 10dB less than those of the MP, allowing for significant power savings in its overall design. As problematic blocker conditions occur less than 10% of the time, the time-averaged power dissipation of the AP is further reduced from its nominal value by powering it on only when needed. The adaptive nature of the equalization guarantees robustness in the presence of changes in temperature, LO frequency, and blocker characteristics.

The receiver architecture proposed in this paper is shown in Fig. 10.3.2. In order to provide a quantitative design objective, the UMTS standard is targeted. The single-ended-to-differential conversion previously handled by an inter-stage SAW filter is now performed by a balun. The balun is followed by high-IIP2 MP mixers [2] driven by Cherry-Hooper LO buffers. The MP BB filter is an active-RC 3rd-order Chebyshev architecture that drives an 8b pipelined ADC with f_s=50MHz. The AP is a scaled-down version of the MP, with the primary difference being the inclusion of an IM3 generator. For area efficiency, the AP mixer dispenses with the IM2 tuning inductor used in the MP while resistively loaded differential pairs serve as LO buffers. The AP 1st-order BB filter drives an 8b pipelined ADC with f_s=16.66MHz.

In a proper design, the IM3 generator requires a dynamic range of ~10dB above the desired IM3 cancellation ratio. Unlike other approaches [3] that use the 3rd-order Taylor series term of the MOSFET, this design, shown in Fig. 10.3.3, exploits the stronger 2nd-order term by using a conventional squaring circuit and by finishing the cubing with a Gilbert multiplier. Two Gilbert multipliers in series also accomplish a cubing, but generate a higher IM5 product since the switching pair port to the multiplier is highly nonlinear. As it produces a single-ended output, the squaring circuit must be followed by an active balun. To improve the generator CMRR, the negative terminal of the balun is tied to a replica squaring circuit whose inputs are shorted. This branch only generates common-mode signal, which is then rejected by the CMRR of the balun.

The implemented path equalization is partitioned into fixed and adaptive portions. This choice stems from the fact that adaptive equalization of the known path difference is computationally inefficient. The fixed portion consists of a 3-tap IIR filter in the AP. The remaining difference between the two paths is a complex DC gain and a small random mismatch in the baseband filtering characteristic. This difference is broadband in the frequency domain and by the duality principle corresponds to a small number of FIR taps required in the adaptive equalizer.

The normalized LMS (NLMS) algorithm is chosen for the adaptive equalization due to its simplicity and convergence speed. The division associated with this algorithm can be log2-quantized, allowing the use of a barrel shifter as a divider. Although complex NLMS can equalize the phase skew between the MP and AP, it cannot compensate for the difference in I-Q mismatches between the two paths. As shown in Fig. 10.3.4, an additional degree of freedom in the design is added to overcome this issue by feeding the complex corrected signal back to independent I and Q taps on each of the incoming AP signals. Yet another consideration is that the performance of adaptive equalizers is limited in the presence of random DC offset. To handle this issue, the digital back-end includes DC-offset trimming circuitry on the AP and matching HPFs on both paths. Periodic DC trimming must be performed prior to the AP HPFs, or the step response incurred during AP power on will prolong the convergence of the adaptive equalizer.

The implemented system consists of an RF front-end integrated in 0.13µm CMOS, a BB section on PCB, and a digital back-end on an FPGA platform. The integrated portion of the AP consumes 5.7mA from a 1.2V supply and 0.2mm^2 of active die area. The analog discrete AP components draw 7.6mA from a 2.7V supply, numbers that could be reduced in an integrated implementation. The digital circuitry of the AP and equalizer uses a total of 52 18b MAC operations at 16.66MHz. Based on the results obtained in [4], and assuming that the multipliers consume half of the total digital power, the back-end would dissipate approximately 14mA under a 1.3V supply.

For a common duplexer [5], the worst-case specified UMTS IMD condition, with values referred to the LNA input, is -26dBm TX leakage at 1.98GHz, a -34dBm CW blocker at 2.05GHz, when the receiver LO frequency is set to 2.12GHz. Figure 10.3.5 shows that under these conditions, where the TX leakage is modeled by a QPSK signal set to UMTS standards, the resultant total input-referred error is improved by 23dB to -98dBm under equalization. From a specification standpoint, this corresponds to an effective out-of-band IIP3 improvement from -9.2dBm to +3.9dBm. The convergence behavior and performance summary of the system are shown in Fig. 10.3.6 for this case.

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[1] M. Valkama, A.S.H. Ghadam, L. Anttila, M. Renfors, "Advanced Digital Signal Processing Techniques for Compensation of Nonlinear Distortion in Wideband Multicarrier Radio Receivers," *IEEE Trans. on Microwave Theory and Techniques*, vol. 54, pp. 2356-2366, Jun. 2006.
[2] A. Liscidini, M. Brandolini, D. Sanzogni and R.Castello, "A 0.13µm CMOS Front-End, for DCS1800/UMTS/802.11b-g with Multiband Positive Feedback Low-Noise Amplifier," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 981-989, Apr. 2006.
[3] F. Shearer and L. MacEachern, "A Precision CMOS Analog Cubing Circuit," *IEEE NEWCAS*, pp. 281-284, June 2004.
[4] S. Hsu, S.K. Mathew, M.A. Anders et al., "A 110 GOPS/W 16-bit Multiplier and Reconfigurable PLA Loop in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 256-264, Jan. 2006.
[5] muRata, Part # DFYK61G95LBJCA.

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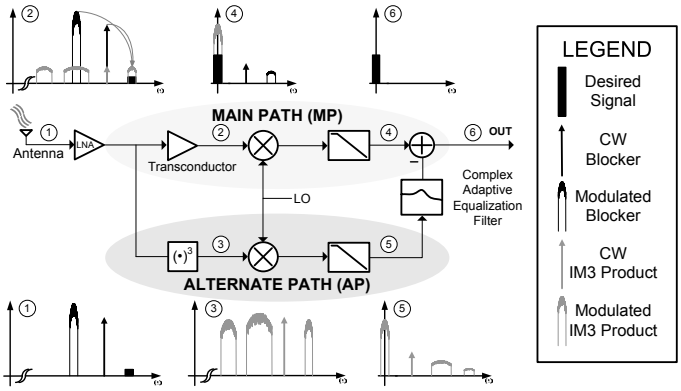


Figure 10.3.1: IM3 equalization concept.

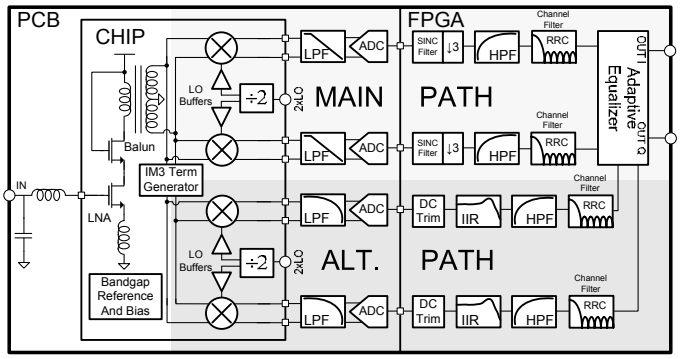


Figure 10.3.2: UMTS receiver architecture.

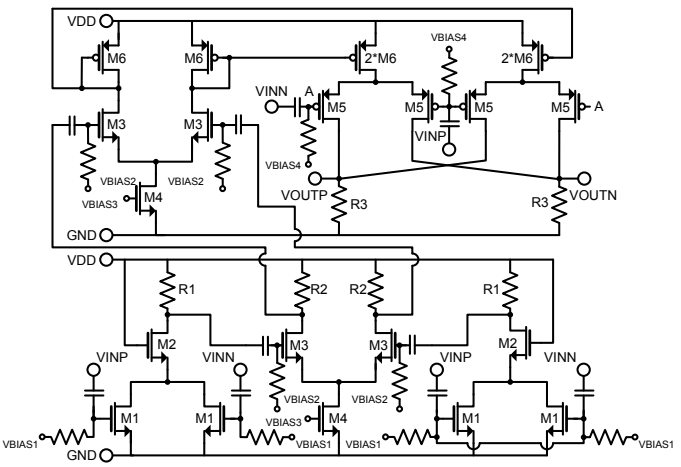


Figure 10.3.3: IM3 term generator schematic.

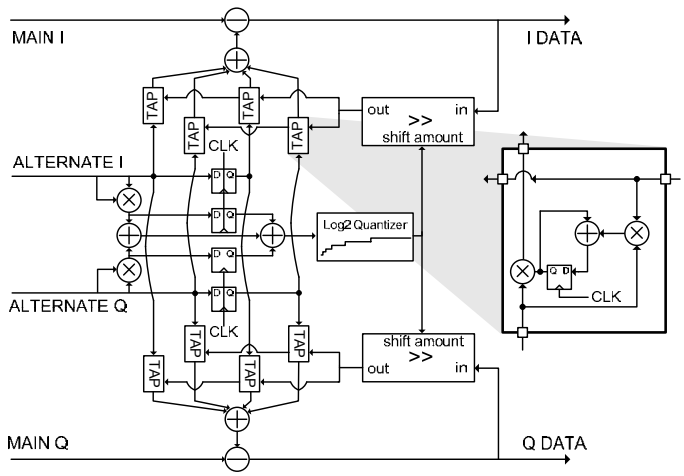


Figure 10.3.4: Enhanced NLMS adaptive equalizer block diagram.

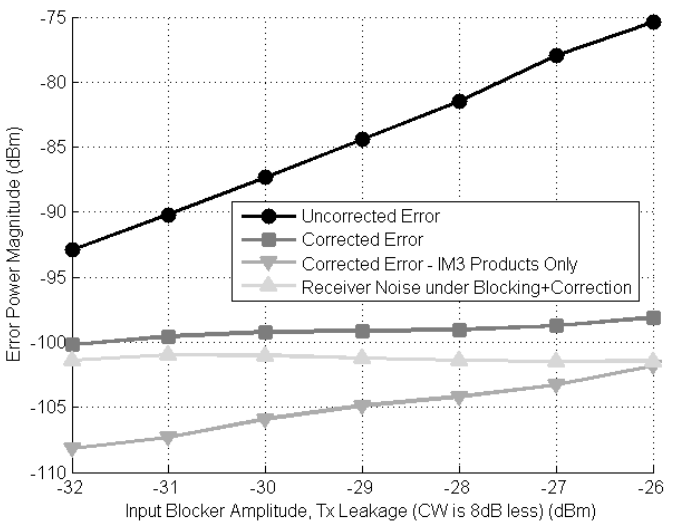
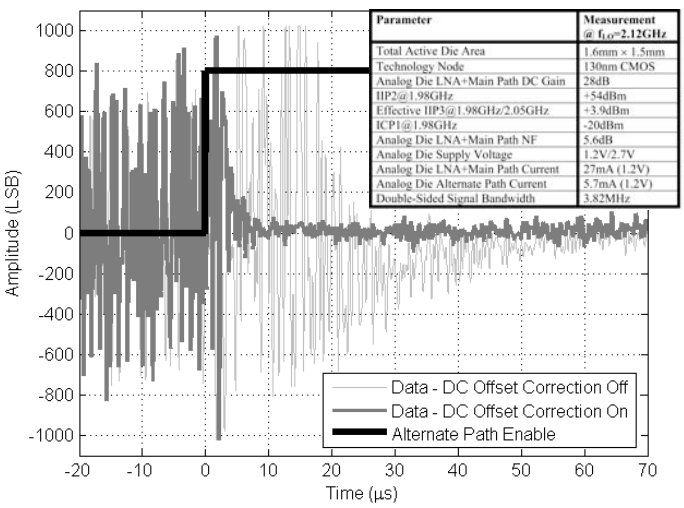


Figure 10.3.5: Measured input-referred error under worst-case blocking scenario.



Parameter	Measurement @ f_{LO}=2.12GHz
Total Active Die Area	1.6mm × 1.5mm
Technology Node	130nm CMOS
Analog Die LNA+Main Path DC Gain	28dB
IIP2@1.98GHz	+54dBm
Effective IIP3@1.98GHz/2.05GHz	+3.9dBm
ICP1@1.98GHz	-20dBm
Analog Die LNA+Main Path NF	5.6dB
Analog Die Supply Voltage	1.2V/2.7V
Analog Die LNA+Main Path Current	27mA (1.2V)
Analog Die Alternate Path Current	5.7mA (1.2V)
Double-Sided Signal Bandwidth	3.82MHz

Figure 10.3.6: Measured convergence behavior of adaptive equalization algorithm and performance summary.

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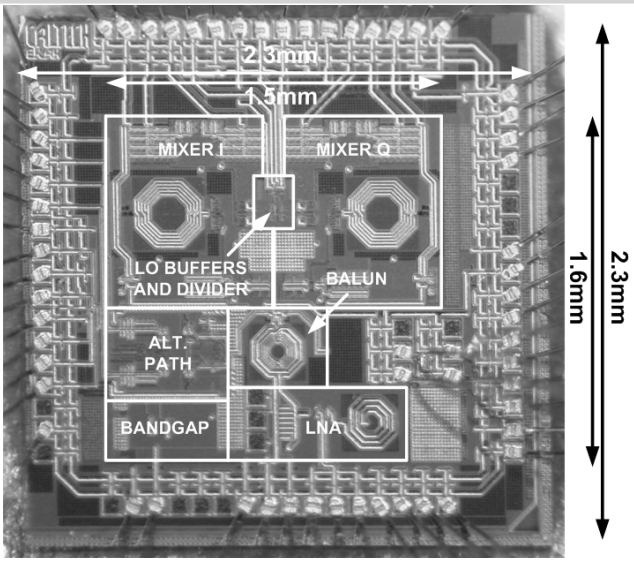

Figure 10.3.7: Chip micrograph.

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