Concepts and Methods in Optimization of Integrated *LC* VCOs

Donhee Ham, *Student Member, IEEE,* and Ali Hajimiri, *Member, IEEE*

***Abstract*—Underlying physical mechanisms controlling the noise properties of oscillators are studied. This treatment shows the importance of inductance selection for oscillator noise optimization. A design strategy centered around an inductance selection scheme is executed using a practical graphical optimization method to optimize phase noise subject to design constraints such as power dissipation, tank amplitude, tuning range, startup condition, and diameters of spiral inductors. The optimization technique is demonstrated through a design example, leading to a 2.4-GHz fully integrated, *LC* voltage-controlled oscillator (VCO) implemented using 0.35-μm MOS transistors. The measured phase-noise values are −121, −117, and −115 dBc/Hz at 600-kHz offset from 1.91, 2.03, and 2.60-GHz carriers, respectively. The VCO dissipates 4 mA from a 2.5-V supply voltage. The inversion mode MOSCAP tuning is used to achieve 26% of tuning range. Two figures of merit for performance comparison of various oscillators are introduced and used to compare this work to previously reported results.**

***Index Terms*—Analog integrated circuits, CMOS integrated circuits, *LC* oscillators, optimization, phase noise, radio frequency, voltage-controlled oscillators.**

I. Introduction

INTEGRATED *LC* voltage-controlled oscillators (VCOs) are common functional blocks in modern radio frequency communication systems and are used as local oscillators to up- and downconvert signals. Due to the ever-increasing demand for bandwidth, very stringent requirements are placed on the spectral purity of local oscillators. Efforts to improve the phase-noise performance of integrated *LC* VCOs have resulted in a large number of realizations [1]–[23]. Despite these endeavors, design and optimization of integrated *LC* VCOs still pose many challenges to circuit designers as simultaneous optimization of multiple variables is required.

A computer-aided optimization technique using *geometric programming* has been recently used to find the optimum design for certain *LC* oscillator topologies efficiently [24], [25]. Despite its efficiency, it provides limited physical insight into choosing the optimum design, as it completely relies on the computer to perform the optimization. Therefore, even in the presence of such CAD tools, firm understanding of the underlying tradeoffs among the design parameters is essential to enhance circuit innovations and increase design productivity. This is especially important when the number of design parameters is large, as any optimization tool *unjustifiably* exploits the limitations of the models used.

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The authors are with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125 USA.

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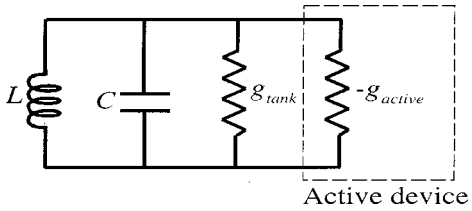

Fig. 1. Steady-state parallel *LC* oscillator model.

To address this issue, we consider underlying physics of *LC* oscillators in this paper, concluding that *inductance selection process* plays a central role in oscillator noise optimization. An investigation of phase-noise properties leads to a design strategy based on an inductance selection scheme, providing a basis for a detailed optimization methodology presented later in this work. This optimization process entails an intuitive graphical method to visualize the design constraints such as tank amplitude, frequency tuning range, and startup condition, allowing minimization of phase noise while satisfying all design constraints.

Section II studies *LC* oscillators from a physical standpoint, providing essential insights into the noise characteristics of *LC* oscillators. In Section III, a specific oscillator topology is chosen as a design example and design constraints are imposed on the oscillator. The inherent properties of phase noise lead to a design strategy. Section IV explains the details of our graphical optimization process. Elaborate simulation results of the optimized VCO accurately predicting phase noise are shown in Section V. Section VI presents the experimental results and compares the performance of our VCO to that of other reported *LC* oscillators to prove the adequacy of our design methodology.

II. Underlying Physics of *LC* Oscillators

In this section, we will perform a simplified analysis of oscillator noise to obtain essential understanding of the basic tradeoffs in an *LC* oscillator using the *noise-to-carrier ratio* (NCR) as a measure of oscillator performance. A more accurate approach leading to a design strategy for phase-noise optimization will be presented in Section III. Although the following argument is limited to the oscillators with parallel *LC* tanks, a series tank can be analyzed using a dual line of argument.

A. Oscillator Voltage Amplitude

Fig. 1 shows the model for a parallel *LC* oscillator in steady state, where the conductance $g_{\rm tank}$ represents the tank loss and $-g_{\rm active}$ is the effective negative conductance of the active devices that compensates the losses in the tank.

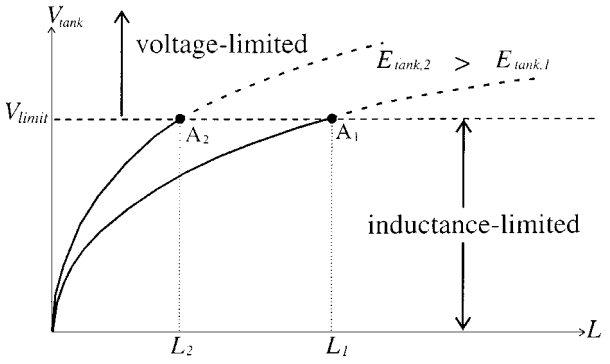

Fig. 2. $E_{\rm tank}$ versus L curves obtained from (2) for two different tank energies $E_{\rm tank,2} > E_{\rm tank,1}$. With an increasing inductance, the tank amplitude grows along the solid parts of the curves until it reaches $V_{\rm limit}$ (inductance-limited regime). Once the tank amplitude reaches $V_{\rm limit}$, it stops growing with the further increase of inductance (voltage-limited regime). The parts of curves with broken lines are unrealizable.

Two modes of operation, named *current-* and *voltage-limited regimes*, can be identified for a typical *LC* oscillator considering the bias current as the independent variable [18]. In the current-limited regime, the tank amplitude $V_{\rm tank}$ linearly grows with the bias current according to $V_{\rm tank} = I_{\rm bias}/g_{\rm tank}$ until the oscillator enters the voltage-limited regime. In the voltage-limited regime, the amplitude is limited to $V_{\rm limit}$, which is determined by the supply voltage and/or a change in the operation mode of active devices (e.g., MOS transistors entering triode region). Thus, $V_{\rm tank}$ can be expressed as

$$V_{\rm tank} = \begin{cases} I_{\rm bias}/g_{\rm tank} & (I\text{-limited}) \\ V_{\rm limit} & (V\text{-limited}). \end{cases} \tag{1}$$

These two modes of operation can be viewed from a different perspective, by using the tank inductance L as the independent variable instead of $I_{\rm bias}$. Noting that the tank energy $E_{\rm tank}$ is defined as $E_{\rm tank} \equiv CV_{\rm tank}^2/2$, $V_{\rm tank}$ can be expressed in terms of $E_{\rm tank}$, i.e.

$$V_{\rm tank}^2 = \frac{2E_{\rm tank}}{C} = 2E_{\rm tank}\omega_0^2 L \tag{2}$$

where $\omega_0 = 1/\sqrt{LC}$ is the oscillation frequency. The tank amplitude grows with L for given $E_{\rm tank}$ and ω_0 as indicated by (2) and depicted in Fig. 2 for two different tank energies $E_{\rm tank,1} < E_{\rm tank,2}$. While being *the same* as the current-limited regime, we refer to this mode as *inductance-limited regime* when L is the independent variable. Therefore, any equation valid in the current-limited regime must be valid in the inductance-limited regime and *vice versa*. This alternative denomination will facilitate the understanding of various tradeoffs in oscillator design throughout this work. Once the tank amplitude reaches $V_{\rm limit}$, it stops increasing with further increase of the inductance and the oscillator will enter the voltage-limited regime as before.

Note that many different inductors with the same inductance, L, can be made in any technology. For example, different on-chip spiral inductors with the same L can be designed using different geometric parameters such as diameter, number of turns, etc. [24]. However, only one of these designs will offer the minimum loss, or the smallest equivalent parallel conductance, g_L. Unless otherwise specified, from this point on, whenever we refer to an inductance L, we assume that this optimization is already performed [24] and hence L corresponds to the inductor with the minimum loss. Note that the minimum loss g_L is a function of L.

The equivalence of the current- and inductance-limited regimes can be used to combine (1) and (2) to determine the relation between $E_{\rm tank}$ and $I_{\rm bias}$ in the inductance-limited regime. Assuming that the losses due to the on-chip spiral inductors are dominant in the integrated *LC* oscillators, (i.e., $g_{\rm tank} \approx g_L$)

$$E_{\rm tank} \propto I_{\rm bias}^2/(Lg_L^2) \quad (L\text{-limited}). \tag{3}$$

While (2) is valid in both inductance- and voltage-limited regimes, it is easier to deal with a constant quantity $V_{\rm limit}$ in the voltage-limited regime, and hence we can rewrite (2) as

$$V_{\rm tank}^2 = \begin{cases} 2E_{\rm tank}\omega_0^2 L & (L\text{-limited}) \\ V_{\rm limit}^2 & (V\text{-limited}) \end{cases}. \tag{4}$$

B. Oscillator Voltage Noise

The *equipartition theorem* of thermodynamics [26] states that at absolute temperature T, each independent degree of freedom for a system in equilibrium has a mean energy of $kT/2$. For instance, noting that in a parallel *RC* circuit, only one independent initial condition can be defined for the capacitor, the equipartition theorem states that $C\langle v_n^2\rangle/2 = kT/2$, which leads to the well-known kT/C noise, i.e.

$$\langle v_n^2\rangle = \frac{kT}{C}. \tag{5}$$

In the parallel *LC* oscillator of Fig. 1, the voltage noise $v_{\rm n}$ in the capacitor and the current noise $i_{\rm n}$ in the inductor are generally correlated and do not represent two independent degrees of freedom. However, we may still apply the equipartition theorem to the oscillator as a first-order approximation to obtain

$$\langle v_n^2\rangle \approx \frac{kT}{C} = kT\omega_0^2 L. \tag{6}$$

which shows the kT/C dependence of the mean squared voltage noise across the parallel *LC* tank. In other words, for a given oscillation frequency, the mean squared voltage noise is proportional to the inductance, which is valid in both inductance- and voltage-limited regimes.

One important observation is that the oscillator has a similar response to both the tank energy $E_{\rm tank}$ and the thermal energy $E_{thermal} = kT/2$, as expected intuitively and indicated by (2) and (6), respectively.

C. Noise-to-Carrier Ratio (NCR) and a Mechanical Analogy

Using (4) and (6), we can express the NCR of an *LC* oscillator for a given oscillation frequency as

$$\frac{\langle v_n^2\rangle}{V_{\rm tank}^2} \propto \begin{cases} 1/E_{\rm tank} & (L\text{-limited}) \\ L & (V\text{-limited}). \end{cases} \tag{7}$$

Equation (7) shows that although $V_{\rm tank}$ increases with L for a given $E_{\rm tank}$, as seen in Fig. 2, the NCR stays constant in the in-

ductance-limited regime and *does not* depend on the value of the inductor. However, once the oscillator enters the voltage-limited regime, the NCR increases with L. Therefore, choosing an inductance L that places the oscillator in the voltage-limited regime results in *waste of inductance* and will only increase the NCR. An important observation is that for a given $E_{\rm tank}$, a larger tank amplitude obtained by increasing the inductance L *does not* result in a better noise performance because the oscillator has a similar response to both the tank energy and the thermal energy, as noted earlier. On the other hand, the NCR can indeed be improved by increasing the tank energy, as can be seen from (7), which will inevitably result in larger power dissipation.

We can draw a mechanical analogy to the *LC* oscillator to help us understand the dependence of the NCR on the value of the inductor. Consider a mass-spring oscillator in which a mass m is fastened to one end of a spring with a spring constant k, while the other end of the spring is kept stationary. The mass is immersed in water and subject to random bombardment of water molecules. The loss due to the water friction is compensated by a hand which follows the oscillation of the mass and continuously injects compensating energy into the system. The hand is assumed to have undesirable yet inherent shaking.

The comparison between the differential equations for the velocity of the mass and the voltage across the parallel *LC* tank reveals the analogy of the mass m and the spring constant k to the capacitance C and the inverse of the inductance $1/L$, respectively. The mass velocity corresponds to the voltage across the parallel *LC* tank. The random bombardment of water molecules and the hand shaking correspond to the tank noise and the active device noise, respectively. The hand can only make limited displacements and never allows the mass to exceed its range. This introduces an upper bound for the maximum displacement and hence the maximum velocity of the mass,[1] resulting in a *velocity-limited regime* as an analog to the voltage-limited regime.

As expected intuitively, the mass of the oscillator has a similar response to the oscillation energy and the thermal energy. Therefore, a smaller mass results in a larger maximum velocity, a larger velocity noise, and hence a constant noise-to-signal ratio for a given oscillation energy until the oscillation reaches the velocity-limited regime. In the velocity-limited regime, a reduction in mass degrades the noise-to-signal ratio as the velocity noise keeps increasing while the maximum velocity stays constant.

D. Fundamental Relation between Loss and Noise

An oscillator can be viewed as an energy conversion engine as shown in Fig. 3. In an oscillator, the active device acts as a means to transfer energy from the dc power supply to the resonator and convert it from dc to ac. As pointed out in the previous subsection, a larger $E_{\rm tank}$ results in a better NCR. Therefore, every effort should be made to maximize the *energy transfer efficiency* of active devices (see Fig. 3), as it will directly increase the tank energy of the resonator. The energy loss in the active device is usually a strong function of its voltage and current waveforms and the energy transfer efficiency can be improved by proper timing of the voltage and current as in certain oscillator topologies, such as Colpitts [27].

[1]Noting that $kx_{\rm max}^2/2 = mv_{\rm max}^2/2$.

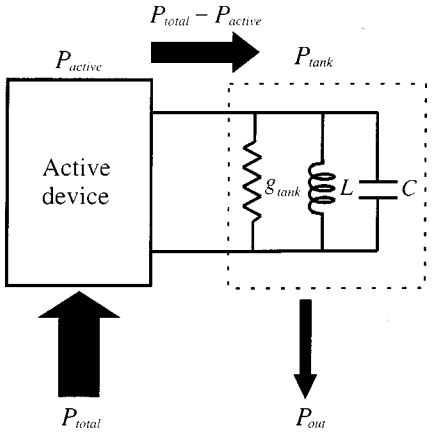

Fig. 3. *LC* oscillator as an energy conversion engine. The *energy transfer efficiency* of the active device can be defined as $(P_{\rm total} - P_{\rm active})/P_{\rm total}$.

It has been shown that such efficient operation of active devices is closely linked to the exploitation of cyclostationarity to reduce noise contributions from active devices [27]. This operational perspective can be viewed from a fundamental angle. In *any* physical system, loss components and noise have an intimate connection, because any quantity representing dissipation such as resistance is the macroscopic average of a large number of microscopic fluctuating components. The *fluctuation-dissipation theorem* of statistical physics states the proportionality of noise and loss parameters and provides the associated proportionality constant [26]. The reduced energy loss in the active device by proper timing implies an enhanced screening of resonator from the loss components in the active devices, which will directly reduce active device's fractional noise contribution to the resonator according to the fluctuation-dissipation theorem. This explains the underlying physics for the active device noise reduction due to cyclostationary effects [27].

E. Design Insights

Although (7) provides essential insights into the oscillator noise as a function of $E_{\rm tank}$, the bias current $I_{\rm bias}$ is a more practical design parameter for electrical oscillators. To that end, we convert (7) into

$$\frac{\langle v_n^2\rangle}{V_{\rm tank}^2} \propto \begin{cases} Lg_L^2/I_{\rm bias}^2 & (L\text{-limited}) \\ L & (V\text{-limited}) \end{cases} \tag{8}$$

by using (3).

Two important concepts of *waste of inductance* and *waste of power* in the voltage-limited regime can be seen from (8). Increasing L beyond the value that puts the oscillator at the edge of the voltage-limited regime will degrade the NCR in proportion to the excess inductance, and hence will result in *waste of inductance*. Neglecting this distinction between the voltage- and inductance-limited regimes can lead to noise optimization guidelines promoting maximization of L [6]. Similarly, increasing the bias current in excess of the value that places the oscillator at the borderline of the two regimes will not improve the NCR and therefore induces the more commonly appreciated concept of *waste of power*.

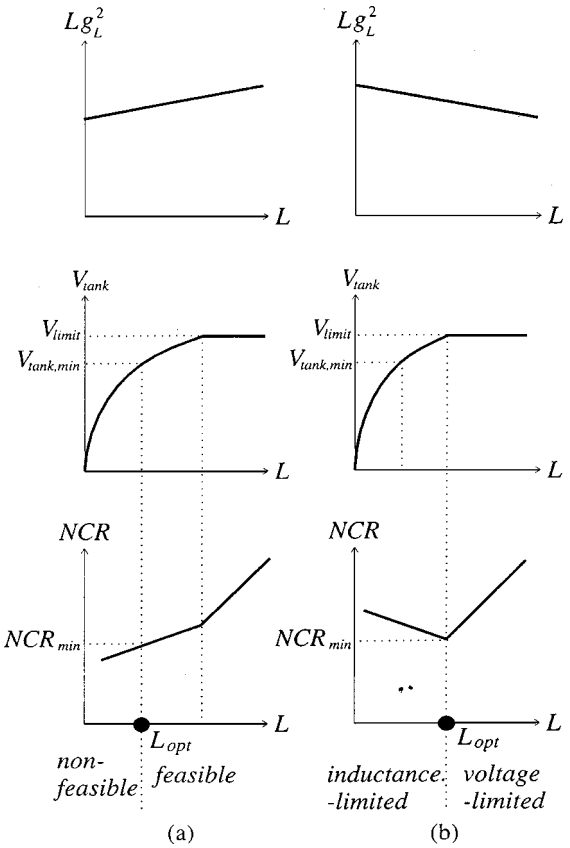

Fig. 4. $Lg_L^2, V_{\rm tank}$, and NCR versus L for a given $I_{\rm bias}$. (a) Lg_L^2 increasing with an increasing inductance L. (b) Lg_L^2 decreasing with an increasing inductance L.

Based on (8), the optimum NCR for a given bias current is obtained in the inductance-limited regime when Lg_L^2 assumes its minimum value. The specific behavior of Lg_L^2 with the inductance has a strong dependence on the particular implementation of the inductor. Now, we investigate two hypothetical, yet illustrative, cases to show how the optimum inductance for the optimum NCR can be obtained for a given $I_{\rm bias}$.

Case 1) Lg_L^2 increasing with L: First, we consider the case in which Lg_L^2 increases with the inductance. As can be seen from (8), a smaller inductance results in a better NCR for a given bias current. However, the inductance cannot be reduced indefinitely since in practice, we always have a minimum tank amplitude constraint $V_{\rm tank} \geq V_{\rm tank,min}$ and/or a startup condition. The excessive reduction of inductance will eventually violate the minimum tank amplitude or the startup constraint. Consequently, the optimum inductance for the optimum NCR is determined when the design lies at the verge of the tank amplitude or startup constraint.[2] Hypothetical curves for Lg_L^2, $V_{\rm tank}$, and NCR versus L for a fixed bias current in this case are shown in Fig. 4(a), where the minimum tank amplitude constraint is the limiting mechanism for this reduction.

[2]The startup constraint is normally imposed by specifying the minimum small-signal loop gain between 2 and 3. Hence, the design at the verge of the startup constraint still has a sufficient margin on the loop gain.

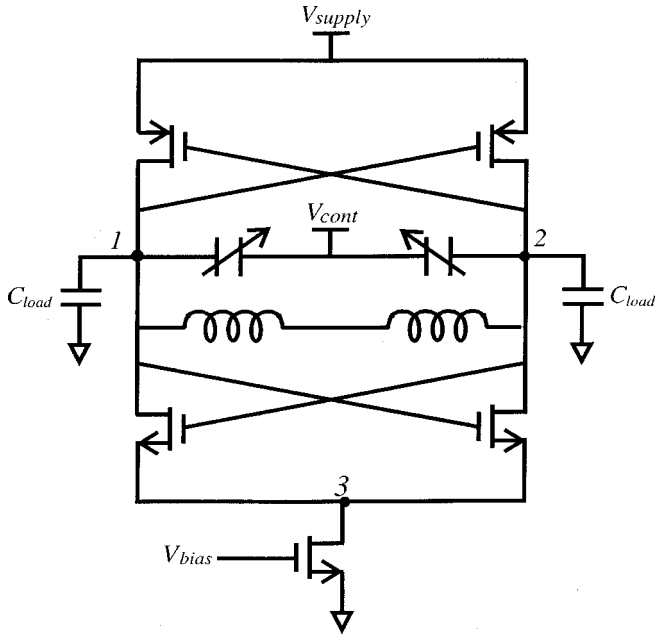

Fig. 5. VCO core schematic.

Case 2) Lg_L^2 decreasing with L: Now we consider the case where Lg_L^2 decreases with increasing inductance. In this case, (8) shows that a larger inductance in the inductance-limited regime results in a better NCR for a given bias current. Hence, the optimum inductance for the optimum NCR is the one that places the design at the edge of the inductance-limited regime, as seen in hypothetical curves for Lg_L^2, $V_{\rm tank}$, and NCR versus L for a fixed bias current of Fig. 4(b).

F. Phase Noise Versus NCR

The NCR was used in this section to investigate the general properties of oscillator noise. While being informative, the NCR lacks specific information on the frequency dependence of noise or its conversion mechanism. Unlike the NCR, phase noise bears spectral information about the oscillator noise and thus assumes a different mathematical expression from (8). Nevertheless, similar central concepts, such as waste of power, waste of inductance, power–noise tradeoff, and the importance of the inductance selection will reappear in expressions for phase noise, as will be seen later in Section III. Now, a more detailed design strategy based upon specific noise properties of a practical *LC* oscillator will be developed through a design example in the following section.

III. *LC* VCO Topology, Design Constraints, and Design Strategy

In this section, we demonstrate the design strategy through the oscillator topology of Fig. 5. Design constraints are specified and a design strategy specific to the circuit is devised for phase-noise optimization.

A. Design Topology

The cross-coupled *LC* oscillator of Fig. 5 is selected as a vehicle to demonstrate our optimization process. Full exploitation

TABLE I
TWELVE INITIAL DESIGN VARIABLES

Components	Initial design variables
Transistors	W_n, W_p, L_n, L_p
Spiral inductors	b, s, n, d
Varactors	$C_{v,max}$, $C_{v,min}$
Load capacitors	C_{load}
Bias current	I_{bias}

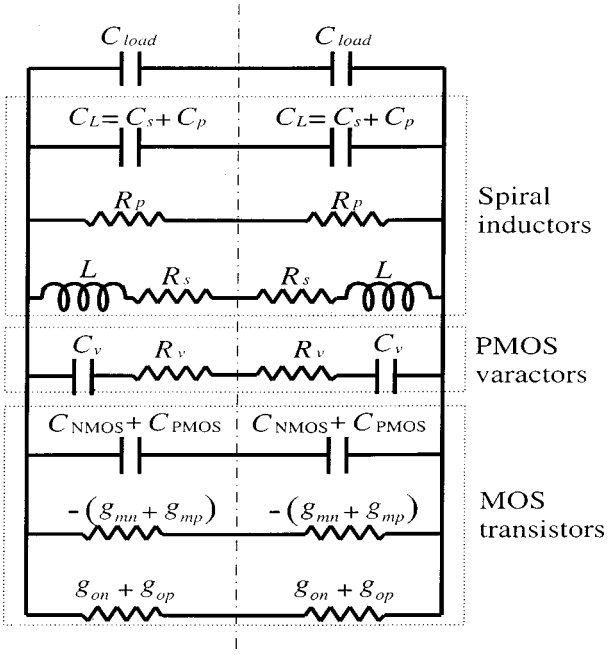

Fig. 6. Equivalent oscillator model.

of differential operation lowers undesirable common-mode effects such as extrinsic substrate and supply noise amplification and upconversion. The oscillation amplitude of this structure is approximately a factor of two larger than that of the nMOS-only structure due to the pMOS pair [18], [28], [29]. The rise and fall time symmetry is also incorporated to further reduce the $1/f$ noise upconversion [27]. These properties result in a better phase-noise performance for a given tail current.

There are twelve initial design variables associated with this specific oscillator: MOS transistors dimensions (W_n, W_p, L_n, and L_p), geometric parameters of on-chip spiral inductors (metal width b, metal spacing s, number of turns n, and diameter d), maximum and minimum values of the varactors ($C_{\mathrm{v,max}}$ and $C_{\mathrm{v,min}}$), load capacitance (C_{load}) and tail bias current in the oscillator core (I_{bias}). These design variables are listed in Table I. Later, we will reduce the number of independent design variables to six through proper design considerations.

The equivalent circuit model of the oscillator is shown in Fig. 6 [25], where the broken line in the middle represents either the common mode or ground. The symmetric spiral inductor

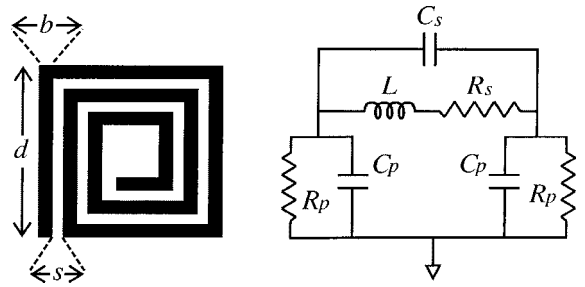

Fig. 7. Symmetric spiral inductor model.

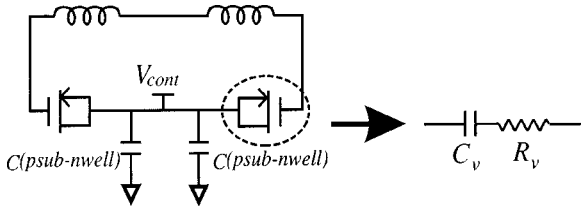

Fig. 8. *LC* tank and MOSCAP varactor.

model of Fig. 7 [30] with identical *RC* loading on both terminals is used as a part of the tank model. Varactors for frequency tuning are made out of the gate channel capacitor of standard pMOS transistors in inversion mode. They are modeled with a capacitor C_v in series with a resistor R_v as in Fig. 8, which is used as a part of the tank model.

In Fig. 6, C_{NMOS} and C_{PMOS} are the total parasitic capacitances of the nMOS and pMOS transistors, respectively,[3] and g_m and g_o are small-signal transconductance and output conductance of the transistors, respectively. Although the values of g_m and g_o vary with the change of the operating points of transistors in the course of oscillation, we will use the values of g_m and g_o when the voltage across the *LC* tank is zero. This approximation facilitates the analytical expression of design constraints. We will justify that the approximation does not mislead the design shortly. All the electrical parameters in the equivalent circuit model can be expressed in terms of design variables, by utilizing existing formulae for transistor parameters and on-chip resonator parameters [24], [25].

The frequently appearing parameters in our optimization process are the tank loss g_{tank}, effective negative conductance $-g_{\mathrm{active}}$, tank inductance L_{tank}, and tank capacitance C_{tank} of Fig. 1, given by

$$2g_{\mathrm{tank}} = g_{on} + g_{op} + g_v + g_L \tag{9}$$

$$2g_{\mathrm{active}} = g_{mn} + g_{mp} \tag{10}$$

$$L_{\mathrm{tank}} = 2L \tag{11}$$

$$2C_{\mathrm{tank}} = C_{\mathrm{PMOS}} + C_{\mathrm{NMOS}} + C_L + C_v + C_{load} \tag{12}$$

respectively, where g_L and g_v are the effective parallel conductance of the inductors and varactors, respectively.[4] As g_{tank} and C_{tank} assume certain range of values as the varactor capacitance varies, their maximum and minimum values will be denoted by subscripts $\max$ and $\min$.

[3] $C_{\mathrm{NMOS}} = C_{gs,n} + C_{db,n} + 4C_{gd,n}$, $C_{\mathrm{PMOS}} = C_{gs,p} + C_{db,p} + 4C_{gd,p}$.
[4] $g_L = 1/R_p + R_s/(L\omega)^2$ and $g_v = (C_v\omega)/Q_v$.

B. Design Constraints

Design constraints are imposed on power dissipation, tank amplitude, frequency tuning range, startup condition, and diameter of spiral inductors.

First, the maximum power constraint is imposed in the form of the maximum bias current $I_{\max}$ drawn from a given supply voltage V_{supply}, i.e.

$$I_{\text{bias}} \leq I_{\max}. \tag{13}$$

Second, the tank amplitude is required to be larger than a certain value, $V_{\text{tank,min}}$, to provide a large enough voltage swing for the next stage:

$$V_{\text{tank}} = \frac{I_{\text{bias}}}{g_{\text{tank,max}}} \geq V_{\text{tank,min}}. \tag{14}$$

The subscript $\max$ in $g_{\text{tank,max}}$ signifies the worst-case scenario. Since g_L is the dominant term in (9), the approximation for g_o mentioned earlier does not lead to a significant error.

Third, the tuning range of the oscillation frequency is required to be in excess of a certain minimum percentage of the center frequency, ω, i.e.

$$L_{\text{tank}}C_{\text{tank,min}} \leq \frac{1}{\omega_{\max}^2} \tag{15}$$

$$L_{\text{tank}}C_{\text{tank,max}} \geq \frac{1}{\omega_{\min}^2} \tag{16}$$

where $(\omega_{\max} - \omega_{\min})/\omega$ = (minimum fractional tuning range) and $(\omega_{\max} + \omega_{\min})/2 = \omega$.

Fourth, the startup condition with a small-signal loop gain of at least $\alpha_{\min}$ can be expressed as

$$g_{\text{active}} \geq \alpha_{\min} g_{\text{tank,max}} \tag{17}$$

where the worst-case condition is imposed by $g_{\text{tank,max}}$. To overcome the possible error that the approximation for g_m mentioned previously might cause, we can select a conservative minimum small-signal loop gain $\alpha_{\min}$ (e.g., 3).

Finally, we specify a maximum diameter for the spiral inductor as $d_{\max}$, i.e.

$$d \leq d_{\max} \tag{18}$$

to limit the die area.

C. Phase Noise in the Cross-Coupled Topology

In the $1/f^2$ region, the phase noise is given by [27]

$$\mathcal{L}\{f_{\text{off}}\} = \frac{1}{8\pi^2 f_{\text{off}}^2} \cdot \frac{1}{q_{\max}^2} \cdot \sum_n \left(\frac{\overline{i_n^2}}{\Delta f} \cdot \Gamma_{\text{rms,n}}^2 \right) \tag{19}$$

where f_{off} is the offset frequency from the carrier and $q_{\max}$ is the total charge swing of the tank. The *impulse sensitivity function* (ISF), Γ, represents the time-varying sensitivity of the oscillator's phase to perturbations [27]. Each $\Gamma_{\text{rms,n}}$ in (19) is the root mean square (RMS) value of the ISF for each noise source and is $1/\sqrt{2}$ for an ideal sinusoidal waveform. It can be evaluated more accurately from simulations, as shown in Section V.

The $\overline{i_n^2}/\Delta f$ terms in the sum of (19) represent the equivalent differential noise power spectral density due to drain current noise, inductor noise, and varactor noise, and they are given by [18], [31], [32]

$$\frac{\overline{i_{M,d}^2}}{\Delta f} = 2kT\gamma(g_{d0,n} + g_{d0,p}) \tag{20}$$

$$\frac{\overline{i_{\text{ind}}^2}}{\Delta f} = 2kTg_L \tag{21}$$

$$\frac{\overline{i_{\text{var}}^2}}{\Delta f} = 2kTg_{\text{v,max}} \tag{22}$$

where $\gamma \sim 2/3$ and $\gamma \sim 2.5$ for long- and short-channel transistors, respectively. g_{d0} is the channel conductance at zero V_{DS} and is equal to g_m for long-channel transistors, while it is given by $2I_{\text{drain}}/(L_{\text{channel}}E_{\text{sat}})$ for short-channel transistors [32].[5] $g_{\text{v,max}}$ in the varactor noise power spectral density is used for the worst-case noise.

D. Dominance of Drain Current Noise

In this subsection, we demonstrate the dominance of drain current noise for the design topology of Fig. 5, which will be used to simplify (19).

According to (9), (21) and (22), the equivalent current noise density due to the varactors and the inductors is less than $4kTg_{\text{tank,max}}$, i.e.

$$\frac{\overline{i_{\text{ind}}^2}}{\Delta f} + \frac{\overline{i_{\text{var}}^2}}{\Delta f} < 4kTg_{\text{tank,max}}. \tag{23}$$

While $g_m = g_{d0}$ for long-channel transistors, $g_m < g_{d0}$ for short-channel transistors by definition of the short-channel regime, i.e.

$$\frac{g_m}{g_{d0}} = \frac{L_{\text{channel}}E_{\text{sat}}}{2(V_{GS} - V_{TH})} < 1. \tag{24}$$

Therefore, from (10) and (20), we obtain

$$\frac{\overline{i_{M,d}^2}}{\Delta f} \geq 4kT\gamma g_{\text{active}} \tag{25}$$

where the equality and the inequality are valid for the long- and short-channel transistors, respectively.

Now the ratio of the equivalent current noise density due to the tank components to that of the drain current can be upper bounded using (23) and (25), i.e.

$$\frac{\overline{i_{\text{ind}}^2}/\Delta f + \overline{i_{\text{var}}^2}/\Delta f}{\overline{i_{M,d}^2}/\Delta f} < \frac{4kTg_{\text{tank,max}}}{4kT\gamma g_{\text{active}}} \leq \frac{1}{\gamma\alpha_{\min}} \tag{26}$$

where we used the startup condition (17) to obtain the last inequality. The inequality of (26) predicts that with $\alpha_{\min} = 3$ the drain current noise contributes more than 88% of the circuit noise for short-channel transistors. This prediction agrees well with the simulation result shown later.

Now by taking only the dominant drain current noise term into account in (19), we can obtain an insightful approximation

[5] E_{sat} is the electric field at which the carrier velocity reaches half its saturation velocity.

for phase noise. Using (19) and (20) while replacing $q_{\max}$ with $V_{\text{tank}}/(L_{\text{tank}}\omega^2)$, we obtain

$$\mathcal{L}\{f_{\text{off}}\} \propto \frac{L^2 I_{\text{bias}}}{V_{\text{tank}}^2} \tag{27}$$

where $g_{d0} = 2I_{\text{drain}}/(L_{\text{channel}}E_{\text{sat}})$ was used for short-channel transistors[6] and $\Gamma_{\text{rms}}^2 = 1/2$ was used for a pure sinusoidal waveform. Equation (27) can be easily interpreted by noting that $V_{\text{tank}} = I_{\text{bias}}/g_{\text{tank}} \approx I_{\text{bias}}/g_L$ in the inductance-limited regime and $V_{\text{tank}} = V_{\text{limit}} = V_{\text{supply}}$ in the voltage-limited regime, i.e.

$$\mathcal{L}\{f_{\text{off}}\} \propto \begin{cases} L^2 g_L^2/I_{\text{bias}} & (L\text{-limited}) \\ L^2 I_{\text{bias}}/V_{\text{supply}}^2 & (V\text{-limited}). \end{cases} \tag{28}$$

This equation will be used to define a convenient design strategy in the following subsection.

E. Design Strategy

The properties of phase noise in (28) lead to a design strategy for phase-noise optimization. For a given bias current, phase noise in (28) increases with an increasing L in the voltage-limited regime, which corresponds to *waste of inductance*. Equation (28) also indicates that for a given inductance L, phase noise increases with the bias current in the voltage-limited regime, inducing *waste of power*. Note that (28) ignores the cyclostationary effects that can change the dependence of the phase noise on the bias current in the voltage-limited regime. A more rigorous treatment taking the cyclostationary noise into account shows that phase noise reaches a plateau with an increase of the bias current in the voltage-limited regime [18]. Even with this consideration, the current that places the design in the voltage-limited regime causes waste of power, as unnecessary power dissipation occurs without a significant improvement in phase noise.

For typical on-chip spiral inductors, the minimum effective parallel conductance g_L for a given inductance L decreases with an increasing inductance when the diameter of the inductor is constrained as in (18) [24]. An example of such dependence is shown in Fig. 9 where the optimization for the minimum g_L for a given L constrained to (18) was performed using *geometric programming* [24]. Using the data of Fig. 9, it can be seen that the factor $L^2 g_L^2$ in (28) increases with an increasing inductance, as shown in Fig. 10. Consequently, for a given I_{bias}, phase noise increases with the inductance in the inductance-limited regime and *a smaller inductance results in a better phase noise*.

However, the inductance L cannot be indefinitely reduced, since it will eventually violate the tank amplitude constraint (14) or the startup constraint (17). This can be seen from the simulated g_L versus L curve in Fig. 9: with a decreasing L, g_L rapidly increases and (14) and (17) will be eventually violated. The optimum inductance is then the one that places the oscillator at the verge of either the tank amplitude or the startup constraint.

Now we demonstrate the power-noise tradeoff in the design of *LC* oscillators, assuming that the inductance reduction is limited by the tank amplitude constraint (14). One can obtain the optimum inductance for a given I_{bias} by calculating the maximum allowable g_L using $I_{\text{bias}}/g_{\text{tank}} \approx I_{\text{bias}}/g_L = V_{\text{tank,min}}$. This maximum allowable g_L will correspond to the minimum (and hence optimum) allowable L in Fig. 9. The optimum $L^2 g_L^2/I_{\text{bias}}$ given in (28) is then plotted for different values of I_{bias} in Fig. 11. As can be seen from Fig. 11, a larger bias current results in a better optimum phase noise, concluding that I_{bias} should always be set to its maximum value allowed by (13). Hence, this design constraint is tight.

The design strategy for the oscillator in Fig. 5 can be summarized in the following way: Find *the minimum inductance* that satisfies both the tank amplitude and startup constraints for *the maximum bias current* allowed by the design specifications. This design strategy will be executed using a practical graphical optimization method in the following section.

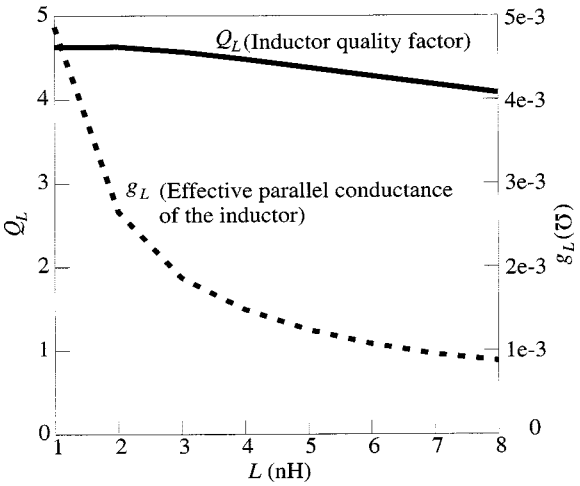

Fig. 9. Simulated maximum inductor quality factor Q_L and minimum effective parallel conductance g_L versus the inductance L.

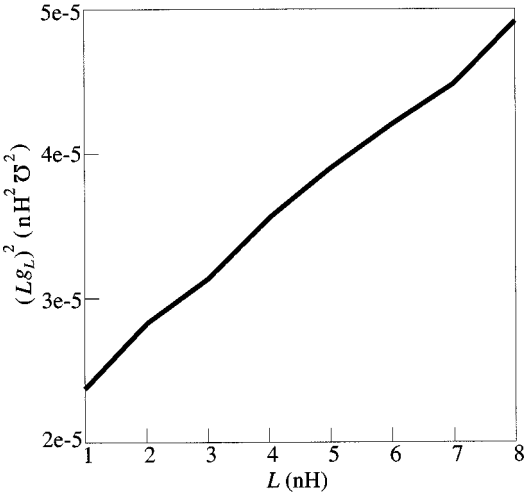

Fig. 10. $L^2 g_L^2$ versus the inductance L.

IV. *LC* VCO Optimization Via Graphical Methods

As mentioned earlier, phase noise of the *LC* oscillator in Fig. 5 can be optimized by reducing the inductance as far as both the tank amplitude and startup constraints allow. While it may

[6] $I_{\text{bias}} = 2I_{\text{drain}}$.

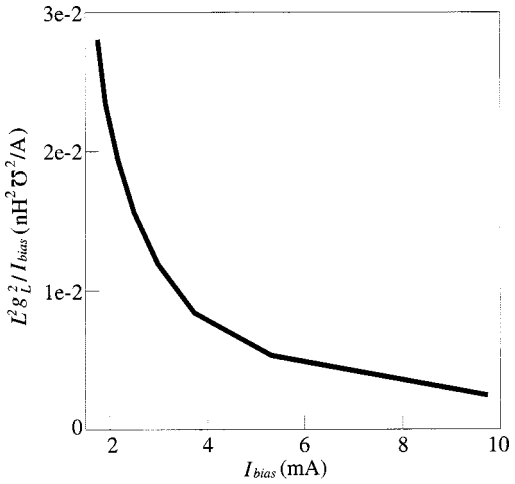

Fig. 11. $L^2 g_L^2 / I_{\rm bias}$ versus the bias current $I_{\rm bias}$.

appear trivial, performing such inductance reduction is challenging in practice, as the L-reduction should be executed while satisfying all the design constraints. This challenge can be overcome by visualizing the design constraints graphically.

It is noteworthy that the following optimization will result in a *near-optimum* design, as time-varying effects such as cyclostationarity, are ignored and the ISF is assumed to have an RMS value of $1/\sqrt{2}$. A final quick fine-tuning simulation has to be performed to obtain the most accurate predictions, as shown in the next section.

Now we demonstrate the optimization process, starting with the reduction of the number of independent design variables through appropriate design considerations, in the context of a numerical example.

A. Independent Design Variables and Numerical Design Constraints

In this subsection, we reduce the number of design variables from the original twelve to six [33]. First, as shown in the previous section, the power consumption constraint (13) is tight and $I_{\rm bias}$ is set to $I_{\rm max}$. Second, in the cross-coupled MOS transistors, both channel length L_n and L_p are set to the minimum allowed by the process technology to reduce parasitic capacitance and achieve the highest transconductance. Also, a symmetric active circuit with $g_{mn} = g_{mp}$ [7] is used to improve the $1/f^3$ corner of phase noise, which establishes a relation between W_p and W_n. Therefore, MOS transistors introduce only one independent design variable, W_n. Third, MOSCAP varactors introduce only one design variable $C_{\rm v,max}$ since in a typical varactor, the ratio $C_{\rm v,max}/C_{\rm v,min}$ is primarily determined by underlying physics of the capacitor and remains constant for a scalable layout. Fourth, the size of the output driver transistors can be preselected so that they can drive a 50-Ω load with a specified output power with the worst-case minimum tank amplitude of $V_{\rm tank,min}$. This results in a specific value for $C_{\rm load}$, excluding it from the set of design variables. Table II shows the reduced set of independent design variables, together with their abbreviated notation that will be used from now on.

[7]This is an approximate criterion. More accurate criteria for minimization of $1/f$ noise can be found in [29].

TABLE II
SIX INDEPENDENT DESIGN VARIABLES

Components	Design variables	Notation
Transistors	W_n	w
Spiral inductors	b, s, n, d	b, s, n, d
Varactors	$C_{v,max}$	c

TABLE III
EXAMPLE OF DESIGN CONSTRAINTS

Eq.	Specifications	Value
N/A	V_{supply}	2.5V
(13)	I_{max}	4mA
(14)	$V_{tank,min}$	2V
(15),(16)	f_{center}	2.4GHz
(15),(16)	minimum tuning range	15%
(17)	α_{min}	3
(18)	d_{max}	200μm

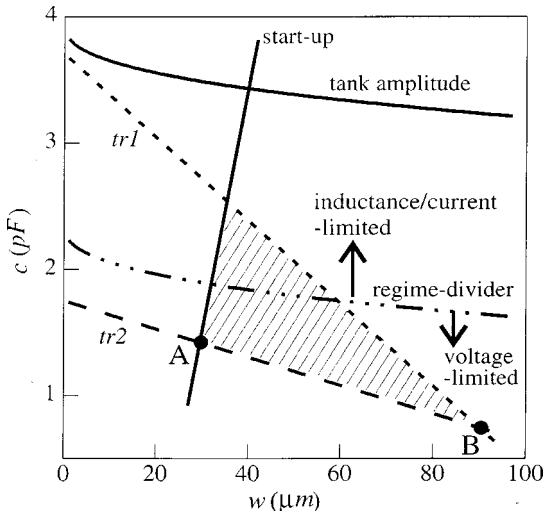

Fig. 12. Design constraints for $I_{\rm bias} = 4$ mA.

To demonstrate a typical design problem, specific numerical design constraints are imposed in accordance with Section III-B as shown in Table III.

B. Identification of Feasible Design Regions

In this subsection, L is fixed to show how feasible design points in the *cw* plane can be identified. The numerical value of the selected inductance in this subsection is 2.7 nH where the inductor geometric parameters, b, s, n, and d, are chosen such that g_L becomes minimum for this value of L.

The design constraints given by (14)–(17) are visualized in Fig. 12 in the *cw* plane, where w is in micrometers and c is in picofarads. The tank amplitude line is the loci of the *cw* points resulting in a tank amplitude of $V_{\rm tank,min} = 2$ V, using (14). Points below this tank amplitude line correspond to $V_{\rm tank}$ larger than 2 V. The broken line with one dash and three consecutive

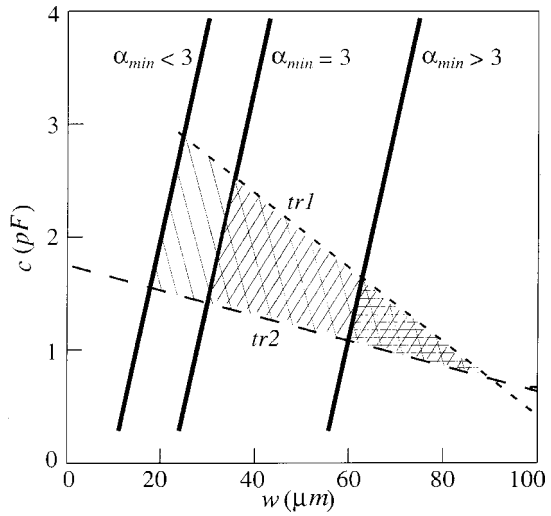

Fig. 13. Effect of changes in the minimum small-signal loop gain.

dots represents the *regime-divider line*, below which the oscillation occurs in the voltage-limited regime with the tank amplitude of $V_{\rm limit} = V_{\rm supply} = 2.5$ V. The $tr1$ and $tr2$ lines are obtained from (15) and (16), respectively. A tuning range of at least 15% with a center frequency of 2.4 GHz is achieved if a design point lies below the $tr1$ line and above the $tr2$ line. The startup line is obtained from (17). The small-signal loop gain is over $\alpha_{\rm min} = 3$ on the right-hand side of the startup line to guarantee startup. The shaded region in Fig. 12 satisfies all the constraints in (14) to (17) and therefore represent a set of feasible design points.

Further intuition can be obtained from this graphical representation. For instance, the effect of the startup condition on the size of the region of plausible design can be seen in Fig. 13. It shows the effect of the loop-gain constraint, where increasing the minimum small-signal loop gain $\alpha_{\rm min}$ shrinks the region of feasibility. Intuitively, a higher small-signal loop gain requires larger transistor dimensions, and therefore the resultant increase in the parasitic capacitances makes it more difficult to obtain the desired tuning range.

The dominance of drain current noise lowers the dependence of phase noise on transistor width w and the maximum capacitance of varactors c. Therefore, the phase-noise difference across the feasible design area in the *cw* plane is expected be small. For example, in Fig. 12, phase-noise difference between points $\mathbf{A}$ and $\mathbf{B}$ is no more than 0.5 dB where the phase noise was calculated from (19). This fact is well reflected in phase-noise approximation (28), which suggests a strong dependence of phase noise on the choice of inductor rather than c and w.

C. Inductance Selection

We now execute the design strategy obtained in Section III, exploiting the graphical representation of the design constraints. As $g_{\rm tank} \approx g_L$ increases with a decreasing L as shown in Fig. 9, the L-reduction will translate the tank amplitude line downward and the startup line to the right, shrinking the feasible design area in the *cw* plane. For g_L in excess of a certain critical value, either the minimum tank amplitude constraint or the startup constraint will be violated, as can be seen from (9), (14) and (17). The inductance corresponding to this critical g_L is the optimum inductance $L_{\rm opt}$. Tuning range constraints are of no concern for the L-reduction process as decreasing L increases the capacitance budget, relaxing the tuning-range constraints. With $L = L_{\rm opt}$, there exists only a single feasible design point in the *cw* plane, which lies on either the tank amplitude line or the startup line.

Different scenarios can be envisioned depending on the order the constraints are encountered with the reduction of L, as shown in Fig. 14. If the tank amplitude limit is reached first, the single feasible design point lies on the tank amplitude line at $L = L_{\rm opt}$, as shown in Fig. 14(a). This unique design point $\mathbf{A}$ in the *cw* plane represents the optimum c and w.

On the other hand, when the startup constraint becomes active first, the region of feasibility will shrink to a single point $\mathbf{B}$ located on the startup line, as shown in Fig. 14(b) and (c). Two different cases can be identified here. If point $\mathbf{B}$ lies in the inductance-limited regime (between the tank amplitude and regime-divider lines) as shown in Fig. 14(b), point $\mathbf{B}$ will correspond to the optimum design and no further action is necessary. However, if $\mathbf{B}$ resides in the voltage-limited regime (below the regime-divider line), as depicted in Fig. 14(c), the design suffers from waste of power. In this case, the bias current should be reduced to make the regime-divider line translate downward and pass through point $\mathbf{B}$.[8]

D. Summary of the Optimization Process

The design optimization process can be summarized as follows. Set the bias current to $I_{\rm max}$, and pick an initial guess for the inductance value. Find the inductor with this inductance that minimizes g_L. This can be done using the method proposed in [24] or using simulation tools such as ASITIC [34]. Plot the design constraints in the *cw* plane using the selected inductor. If there are more than one feasible design points in the *cw* plane, decrease the inductance and repeat until the feasible design area shrinks to a single point, as in Fig. 14. The single design point in the *cw* plane represents the optimum c and w and the corresponding inductor with $L = L_{\rm opt}$ is the optimum inductor. If the single design point lies in the voltage-limited regime, the bias current should be reduced from $I_{\rm max}$ until the regime-divider line passes through the single feasible design point to avoid waste of power.

E. Robust Design

The graphical visualization of design constraints can help us cope with possible process variations, leading to a robust design. In the presence of process variations, the constraint lines turn into bands as shown hypothetically in Fig. 15. The broken and solid lines represent design constraints in the slow and fast process corner, respectively. The robust design points are selected inside the inner triangle, sides of which consist of broken lines. The shaded area in the figure represents unreliable design in the presence of process variations. Accordingly, the optimiza-

[8]The startup and tuning range lines show little dependence on the bias current. It is obvious that the tuning range is not affected by the bias current. The startup constraint is almost independent of the bias current as the transconductance of short-channel transistors shows little dependence on the bias current.

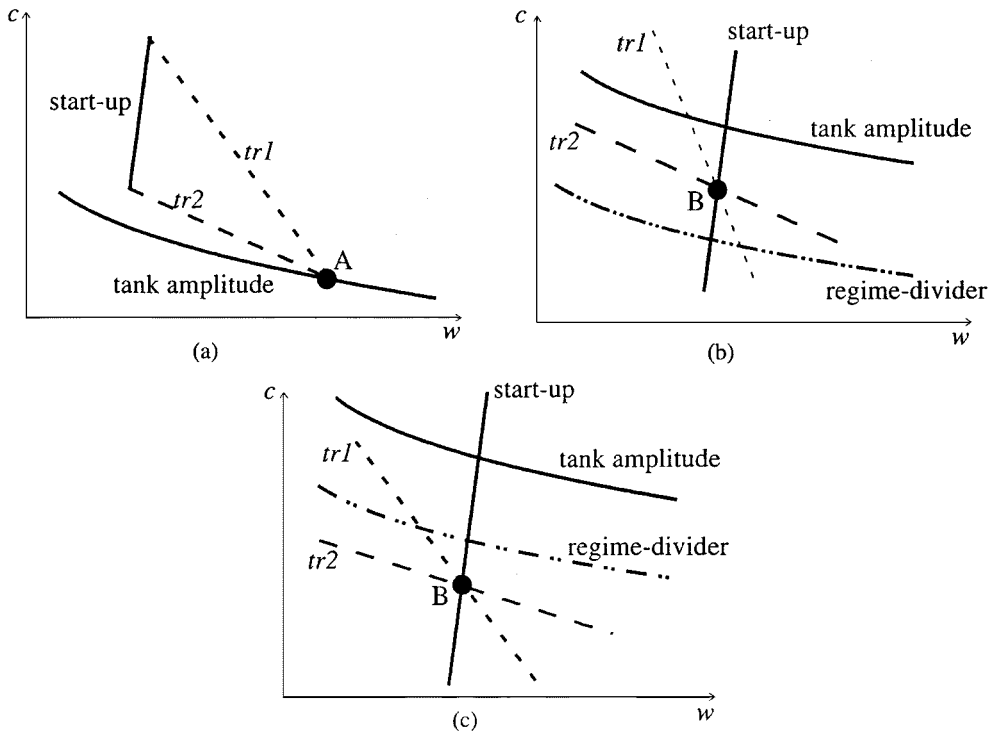

Fig. 14. Design constraints with $L = L_{\text{opt}}$. (a) L-reduction limited by the tank amplitude constraint. (b) L-reduction limited by the startup constraint without waste of power. (c) L-reduction limited by the startup constraint with waste of power.

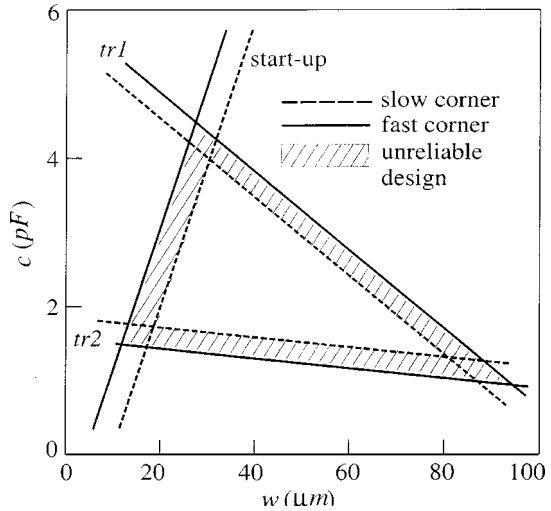

Fig. 15. Process variations and resultant constraint change.

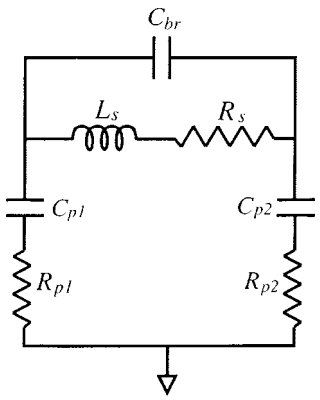

Fig. 16. Non-symmetric spiral inductor model.

tion process should instead be modified to turn the region of reliable design to a single point.

V. Simulation

Validity of the approximations made in the previous sections can be verified using simulations. In this section, an accurate phase-noise simulation is performed [33] on the VCO designed using our optimization process. The more accurate non-symmetric equivalent circuit for spiral inductors used in simulations is depicted in Fig. 16. This non-symmetric model was developed using ASITIC to address the physical asymmetry of the spiral structure [34].

Phase-noise simulation is performed at a center frequency of 2.22 GHz with a tail current of 4 mA. The impulse sensitivity functions (ISFs) of various noise sources are obtained by performing the charge injection simulation [27] and are depicted in Fig. 17 for the pMOS, nMOS, and tail transistors. The cyclostationary effect of the drain current noise due to the periodic operating point change can be taken into account by the *noise modulating function* (NMF), which is proportional to $\sqrt{g_{d0}}$ [27]. The simulated NMF for pMOS and nMOS transistors is shown in Fig. 18. The effective ISF, which is the product of the original ISF and the NMF for the drain current noise, is depicted in Fig. 19.

The total simulated phase noise is -120 dBc/Hz at 600-kHz offset from a 2.22-GHz carrier. The circuit noise contributions from each noise source are shown in Table IV. Note that most of the circuit noise is contributed by the drain current noise of the cross-coupled transistors, as demonstrated earlier. The ap-

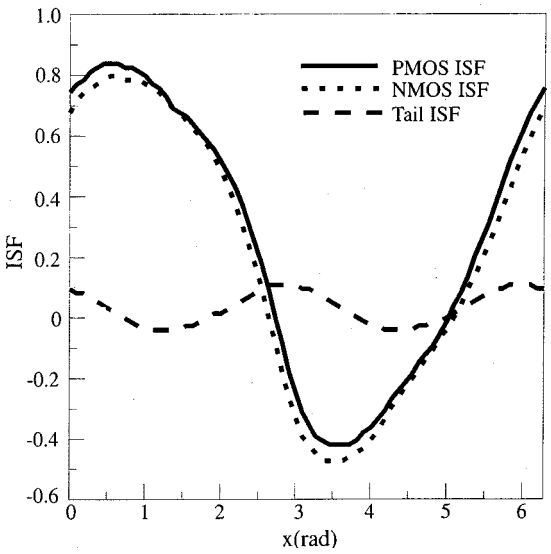

Fig. 17. Impulse sensitivity function (ISF).

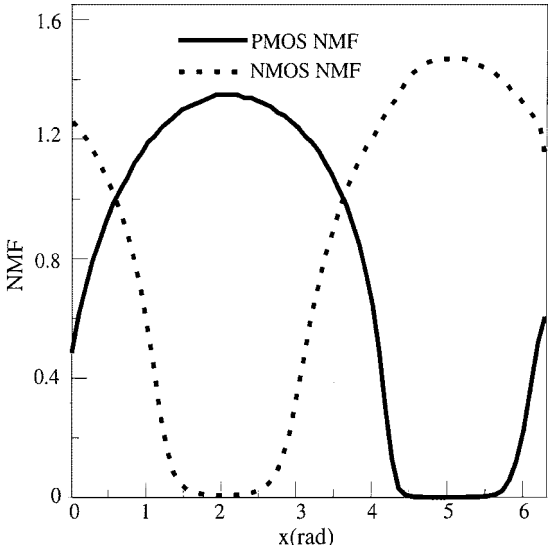

Fig. 18. Noise modulating function (NMF).

proximate equation (28) predicts a phase noise of -121 dBc/Hz at 600-kHz offset. This is only 1 dB different from the simulation results, confirming the validity of the assumption leading to (28). The $1/f$ noise reduction factors are 0.18 and 0.25 for nMOS and pMOS transistors, respectively [27].

VI. Experimental Results

Table V summarizes performance of the VCO, which was implemented in a three-metal 0.35-μm BiCMOS technology, only using MOS transistors. Fig. 20 shows the VCO chip photograph. A tuning range of 26% is achieved, as shown in Fig. 21. Phase noise is measured using an HP8563 spectrum analyzer with phase-noise measurement utility. The measured phase noise at 2.2 GHz is about 3 dB higher than the simulated phase noise.

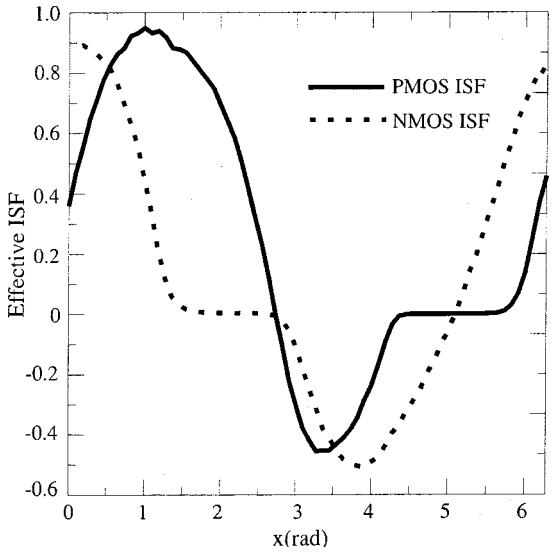

Fig. 19. Effective ISF.

TABLE IV
Simulated Result of Noise Contributions from Each Noise Source

Noise source	PSD (A^2/Hz)	Contribution
Drain current	6.90×10^{-23}	86 %
Gate	1.20×10^{-24}	1.5%
Inductor	4.49×10^{-24}	5.6 %
Varactor	1.77×10^{-24}	2.2 %
Tail current	3.73×10^{-24}	4.7%

TABLE V
VCO Performance Summary

Supply voltage	2.5V
Current (core)	4mA
Center frequency	2.33GHz
Tuning range	26 %
Output power (50-Ω load)	0dBm
Phase noise ($f_c = 1.91GHz$, @$600kHz$)	-121dBc/Hz
Phase noise ($f_c = 2.03GHz$, @$600kHz$)	-117dBc/Hz
Phase noise ($f_c = 2.63GHz$, @$600kHz$)	-115dBc/Hz

This 3-dB difference can be attributed to the uncertain channel noise factor, γ, degradation of tank amplitude caused by the parasitic resistors in metal layers, and high sensitivity of the oscillation frequency to extrinsic supply and control line noise due to the high VCO gain at this frequency.

To measure the phase noise more accurately, we increased the control voltage up to 3.5 V, which further reduced the oscillation frequency to 1.91 GHz where the VCO gain is very low. Fig. 22 shows a plot of phase noise versus offset frequency from

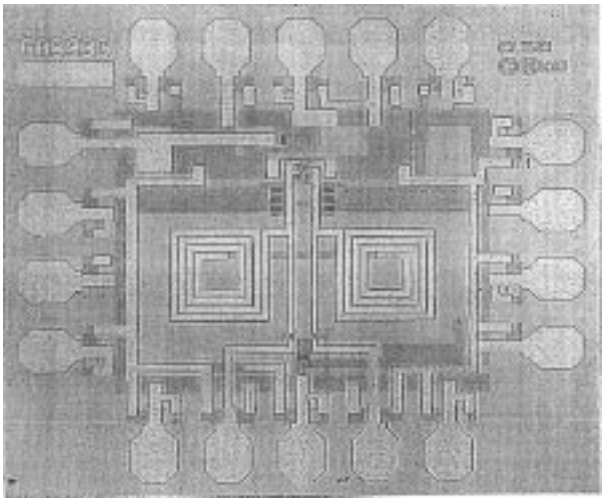

Fig. 20. Chip photograph.

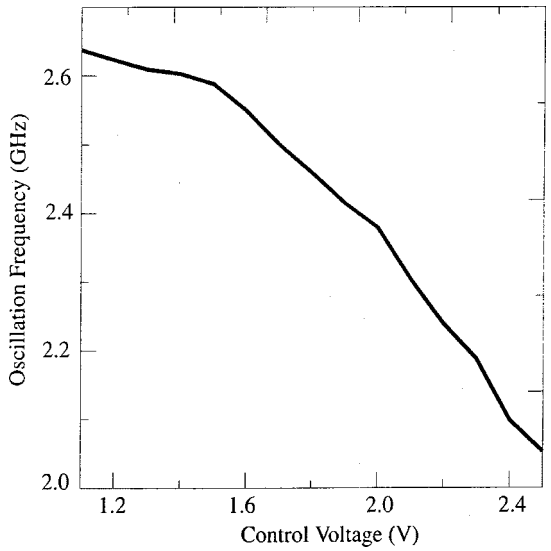

Fig. 21. Frequency tuning.

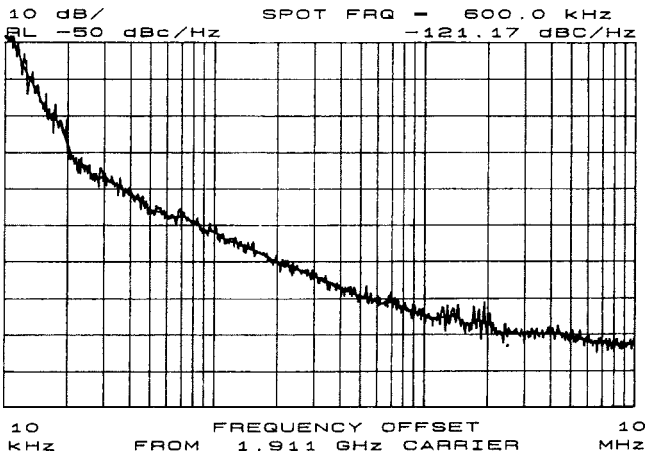

Fig. 22. Measured phase noise versus $f_{\rm off}$ at 1.91 GHz.

the 1.91-GHz carrier. The phase-noise measurement at 600-kHz offset from the 1.91-GHz carrier yields −121 dBc/Hz.

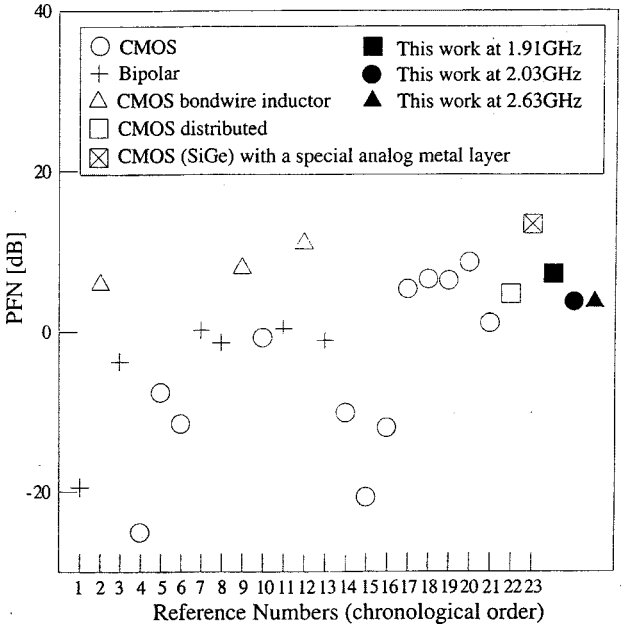

Fig. 23. PFN for various oscillators.

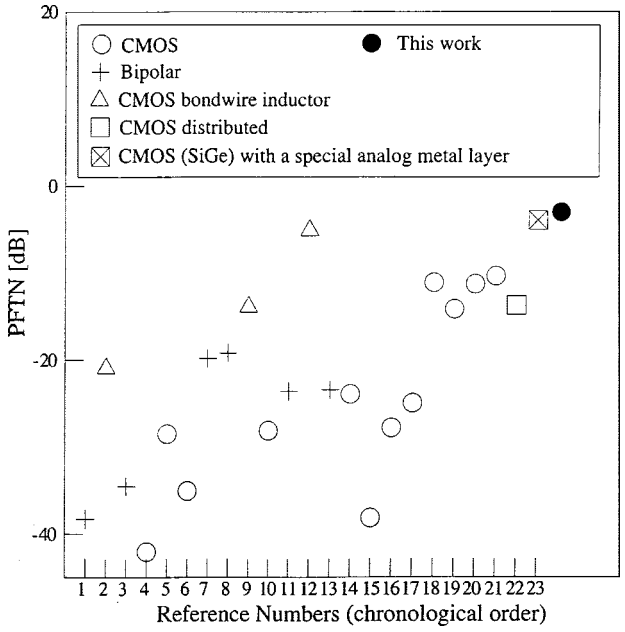

Fig. 24. PFTN for various oscillators.

To compare the performance of our oscillator to recently reported results [1]–[23], we define two figures of merit. First, *power-frequency-normalized* (PFN) figure of merit

$$\mathrm{PFN} = 10\log\left[\frac{kT}{P_{\rm sup}}\cdot\left(\frac{f_0}{f_{\rm off}}\right)^2\right] - \mathcal{L}\{f_{\rm off}\} \qquad (29)$$

was devised, noting that phase noise of an oscillator measured at an offset $f_{\rm off}$ from a carrier at f_0 is proportional to f_0^2 and inversely proportional to $f_{\rm off}^2$ [35] as well as the power dissipated in the resistive part of the tank. As the power dissipated in the resistive part of the tank cannot be easily calculated from the VCO specification, phase noise is normalized to $kT/P_{\rm sup}$

in (29), where $P_{\rm sup}$ is the total dc power dissipated in the VCO. PFN is a unitless figure of merit expressed in dB. A larger PFN corresponds to a better oscillator.

To take tuning range into account in the comparison of different oscillators, a second figure of merit called *power-frequency-tuning-normalized* (PFTN)

$$\mathrm{PFTN} = 10\log\left[\frac{kT}{P_{\rm sup}}\cdot\left(\frac{f_{\rm tune}}{f_{\rm off}}\right)^2\right] - \mathcal{L}\{f_{\rm off}\} \qquad (30)$$

was devised where $f_{\rm tune} = f_{\max} - f_{\min}$. Note that PFTN is a normalization of PFN to the squared tuning range $(f_{\rm tune}/f_0)^2$. Again, a larger PFTN corresponds to a better oscillator.

Using these two figures of merit, the designed oscillator is compared to those reported in [1]–[23] in Figs. 23 and 24. The reported oscillator in this paper has the second largest PFN and the largest PFTN among the oscillators with on-chip inductors using standard metal layers.

VII. Conclusion

Fundamental physics of *LC* oscillators was presented to provide essential understanding of the noise properties of the oscillators. A design strategy centered around an inductance selection scheme was executed using an insightful graphical method to minimize phase noise subject to several design constraints imposed on power, tank amplitude, tuning range, startup, and diameter of spiral inductors. A 2.4-GHz fully integrated *LC* VCO was designed using our optimization technique and implemented as a design example. A tuning range of 26% was achieved with the inversion mode MOSCAP tuning. The measured phase noise was −121, −117, and −115 dBc/Hz at 600 kHz offset from 1.91, 2.03, and 2.60-GHz carriers, respectively. The designed VCO dissipates only 4 mA from a 2.5-V supply voltage. Comparison with other oscillators using two figures of merit, PFN and PFTN, supports the adequacy of our design methodology.

Acknowledgment

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Donhee Ham (S'99) received the B.S. degree in physics from the Seoul National University, Seoul, Korea, in 1996 and the M.S. degree in physics from the California Institute of Technology, Pasadena, CA, in 1999, where he worked at the Laser Interferometer Gravitational Wave Observatory (LIGO). He is currently working toward the Ph.D. degree in electrical engineering at the California Institute of Technology, where his research interest is in high-speed and RF integrated circuits.

During the summer of 2000, he was with the Mixed-Signal Communications IC Design group at the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he investigated wide-bandwidth distributed amplifiers.

Mr. Ham ranked first at the School of Natural Science of Seoul National University and earned the Seoul National University Presidential Top Honor Prize on graduation in 1996. He was a Li Ming Scholarship receipient at the California Institute of Technology during 1999, and received an IBM research fellowship in 2000.

Ali Hajimiri (S'95–M'98) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from the Stanford University, Stanford, CA, in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies (Bell Labs), Holmdel, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, as an Assistant Professor of electrical engineering, where his research interests are high-speed and RF integrated circuits. He is a coauthor of *The Design of Low Noise Oscillators* (Boston, MA: Kluwer, 1999) and has received several U.S. and European patents. He is a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD). He has served as Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Dr. Hajimiri was the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, the Netherlands. He was a corecipient of the International Solid-State Circuits Conference 1998 Jack Kilby Outstanding Paper Award and the winner of the IBM faculty partnership award.