Silicon-Based Distributed Voltage-Controlled Oscillators

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***Abstract*—Distributed voltage-controlled oscillators (DVCOs) are presented as a new approach to the design of silicon VCOs at microwave frequencies. In this paper, the operation of distributed oscillators is analyzed and the general oscillation condition is derived, resulting in analytical expressions for the frequency and amplitude. Two tuning techniques for DVCOs are demonstrated, namely, the inherent-varactor tuning and delay-balanced current-steering tuning. A complete analysis of the tuning techniques is presented. CMOS and bipolar DVCOs have been designed and fabricated in a 0.35-μm BiCMOS process. A 10-GHz CMOS DVCO achieves a tuning range of 12% (9.3–10.5 GHz) and a phase noise of −103 dBc/Hz at 600 kHz offset from the carrier. The oscillator provides an output power of −4.5 dBm without any buffering, drawing 14 mA of dc current from a 2.5-V power supply. A 12-GHz bipolar DVCO consuming 6 mA from a 2.5-V power supply is also demonstrated. It has a tuning range of 26% with a phase noise of −99 dBc/Hz at 600 kHz offset from the carrier.**

***Index Terms*—Distributed oscillators, frequency tuning, transmission lines, voltage-controlled oscillators.**

I. Introduction

THE ever-increasing demand for larger bandwidth in the digital communication market, wired or wireless, is pushing integrated circuits for operation at higher frequencies. Traditionally, these high-frequency circuits have been implemented in compound semiconductor technologies (such as GaAs and InP). Recently, silicon, particularly CMOS, has emerged as a promising low-cost alternate for RF and microwave integrated circuits (ICs). Furthermore, silicon-based ICs are highly suitable for system-on-a-chip implementations. However, silicon suffers from larger parasitic elements both in active and passive devices, and therefore new design techniques are needed at such high frequencies.

Voltage-controlled oscillators (VCOs) are essential building blocks for frequency synthesizers and clock-and-data recovery loops. Monolithic ring and *LC* oscillators have been commonly used as VCOs in such systems. Ring VCOs have inferior noise performance but can generate quadrature signals more readily, while *LC* VCOs offer better phase noise for a given power dissipation. However, it becomes more difficult to achieve all the desired VCO specifications simultaneously as the frequency of operation approaches the self-resonance frequency of the on-chip inductors and the cutoff frequency of transistors f_T. More specifically, to operate at higher frequencies, the tank"s *LC* product should decrease. However, the inductor loss, parasitic capacitances of transistors, and loading from the next stage (e.g., output buffers) do not scale at the same rate. This results in the choice of even smaller L, which corresponds to larger power dissipation for a given oscillation amplitude, and more stringent constraints on the tuning capability of such an *LC* VCO [1]. These limitations make it necessary to pursue alternative approaches, such as distributed oscillators.

Distributed oscillators originate from distributed amplifiers (also known as traveling wave amplifiers) [2]–[5], which have been widely used for wide-band amplification. A distributed amplifier achieves a higher gain–bandwidth product by absorbing the parasitic capacitances of transistors into transmission lines and effectively trades larger delay for a better gain–bandwidth product. Correspondingly, a distributed oscillator can operate at frequencies close to f_T. Also, through a proper choice of number of stages, a distributed oscillator can generate low-noise quadrature signals, which is realized by using dividers or poly-phase filters in current implementations.

Skvor *et al.* [6] proposed to build a VCO by operating a distributed amplifier in the *reverse* gain mode, feeding the signal from the drain dummy load back to the gate line. A discrete 4-GHz distributed oscillator was demonstrated using four GaAs pHEMTs and microstrip lines on a printed circuit board [7]. Recently, using the forward gain operation mode, Kleveland *et al.* [8] showed a 0.18-μm CMOS 17-GHz distributed oscillator with off-chip termination and without any tuning capability.

Despite these advances, it is not clear how integrated distributed oscillators using low-f_T silicon transistors can be tuned without significantly lowering the loop gain and hence increasing the power dissipation for reliable operation. Therefore, it is necessary to devise new tuning techniques for such distributed voltage-controlled oscillators (DVCOs). Also, a systematic and analytical approach to the design of DVCOs is needed to be able to make accurate *a priori* predictions of frequency and amplitude.

This paper addresses these issues and is organized in the following manner. Section II will introduce the operation of distributed amplifiers and distributed oscillators through a detailed analysis of the oscillation condition. This analysis leads to general expressions for the amplitude and frequency of distributed oscillators. Two tuning techniques for DVCOs will be demonstrated in Section III, considering the advantages and disadvantages of each. The design and layout issues will be discussed in Section IV. Finally, experimental results for a 10-GHz CMOS DVCO and a 12-GHz bipolar DVCO will be presented in Section V.

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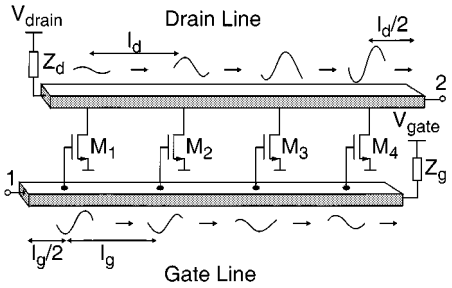


Fig. 1. Basic distributed amplifier.

II. Analysis

In this section, general analyses of distributed amplifiers and distributed oscillators are presented. Although the discussion is carried out in MOS terminology, it is equally valid for bipolar implementations.

A. Distributed Amplifiers

The basic distributed amplifier consists of two transmission lines, the gate line and drain line, and transistors providing gain as shown in Fig. 1. The forward (to the right in the figure) wave on the gate line is amplified by each transistor. The incident wave on the drain line travels forward in synchronization with the traveling wave on the gate line. Each transistor adds power in phase to the signal at each tap point on the drain line. The forward traveling wave on the gate line and the backward (traveling to the left) wave on the drain line are absorbed by terminations matched to loaded characteristic impedance of the gate line Z_g and drain line Z_d, respectively. Assuming that the number of transistors on the line is large and their spacing is much smaller than half wavelength, their input and output capacitances may be considered distributed,[1] Z_g is given by

$$Z_g \approx \sqrt{\frac{j\omega L_g + R_g}{j\omega\left(C_g + \frac{c_{\text{in}}}{l_g}\right) + G_g}} \tag{1}$$

where L_g, R_g, C_g, G_g are the series inductance and resistance and parallel capacitance and conductance of the gate transmission line per unit length, respectively, and c_{in} is the small signal input capacitance of the amplifying stage, which is a MOS transistor in this case. A similar expression can be obtained for Z_d, i.e.,

$$Z_d \approx \sqrt{\frac{j\omega L_d + R_d}{j\omega\left(C_d + \frac{c_{\text{out}}}{l_d}\right) + G_d}} \tag{2}$$

where L_d, R_d, C_d, G_d are the series inductance and resistance and parallel capacitance and conductance of the drain transmission line per unit length, respectively, and c_{out} is the output capacitance of the amplifying stage.

[1]This approximation leads to an underestimation of propagation delay.

The complex propagation constants of the transmission lines are also changed due to the transistor loading, i.e.,

$$\gamma_g \approx \sqrt{(j\omega L_g + R_g)\cdot\left[j\omega\left(C_g + \frac{c_{\text{in}}}{l_g}\right) + G_g\right]} \tag{3}$$

$$\gamma_d \approx \sqrt{(j\omega L_d + R_d)\cdot\left[j\omega\left(C_d + \frac{c_{\text{out}}}{l_d}\right) + G_d\right]} \tag{4}$$

It can be seen from (1)–(4) that device parasitic capacitances are absorbed into the capacitive component of the transmission lines and therefore contribute mainly to the real part of Z_0 and the imaginary part of γ, which do not induce loss.

The gain of the distributed amplifier can be calculated in the following way. Note that the voltage at the kth tap of the gate line is related to the gate line's segment length l_g and complex propagation constant of the loaded gate line γ_g through [9]

$$v_{gk} = v_1 e^{(k-\frac{1}{2})\gamma_g l_g} \tag{5}$$

where v_1 is the voltage at the input node **1** in Fig. 1. This is assuming that the gate line is terminated to Z_g on the right end. Also assuming that the drain line is terminated to Z_d on the left end, the wave going out of the drain of each transistor sees an impedance of $Z_d/2$, which is the parallel combination of the two Z_ds seen on the left and right. The generated wave at the kth drain tap traveling to the right is therefore given by

$$E_{dk} = -g_m \frac{Z_d}{2} v_{gk} = -g_m \frac{Z_d}{2} v_1 e^{-(k-\frac{1}{2})\gamma_g l_g} \tag{6}$$

where g_m is the small signal transconductance of each transistor.[2] Note that a simple g_m can be used to the first order since the transistor parasitic capacitances are primarily absorbed into the real part of Z_0 and the imaginary part of γ. These generated waves travel through different lengths of drain line to reach the output node **2**. Therefore, the total wave traveling to the right at the output is given by superposition, i.e.,[3]

$$\begin{aligned} E_{i2} &= \sum_{k=1}^{n} E_{dk} e^{-(n-k+\frac{1}{2})\gamma_d l_d} \\ &= -g_m \frac{Z_d}{2} v_1 \cdot \sum_{k=1}^{n} e^{-(k-\frac{1}{2})\gamma_g l_g} \cdot e^{-(n-k+\frac{1}{2})\gamma_d l_d} \\ &= -g_m \frac{Z_d}{2} v_1 \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} \end{aligned} \tag{7}$$

where n is the number of transistors.

Part of this incident wave will be reflected due to the impedance mismatch at node **2**, since in general the load impedance Z_L is different from Z_d. The reflected wave E_{r2} is related to the incident wave E_{i2} through the reflection coefficient, i.e.,

$$\Gamma_2 \equiv \frac{E_{r2}}{E_{i2}} = \frac{Z_L - Z_d}{Z_L + Z_d}. \tag{8}$$

[2]The inherent base transit time in bipolar transistors is included in C_π, which is absorbed into the gate line.

[3]Using the identity $a^n - b^n = (a-b)(a^{n-1} + a^{n-2}b + \cdots + b^{n-1})$.

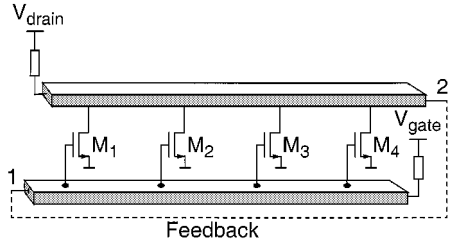


Fig. 2. Basic distributed oscillator.

The *voltage* at node **2** is thus related to the incident wave by

$$v_2 = E_{i2} + E_{r2} = E_{i2} \cdot \frac{2Z_L}{Z_L + Z_d}. \tag{9}$$

Combining (7) and (9), the following general expression for the voltage gain of the amplifier can be obtained:

$$\begin{aligned} A_v &= \frac{v_2}{v_1} \\ &= -g_m(Z_L \| Z_d) \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} \end{aligned} \tag{10}$$

To gain more insight into (10), let us consider the special case where $\gamma l \equiv \gamma_d l_d = \gamma_g l_g$. This can be achieved by having different lengths and widths for the drain and gate lines in the design to guarantee that the product is the same on both lines. Then the voltage gain of (10) can be written as

$$\begin{aligned} A_v &= -n g_m(Z_L \| Z_d) \cdot e^{-\gamma n l} \\ &= -n g_m(Z_L \| Z_d) \cdot e^{-\alpha n l} \cdot e^{-j\beta n l} \end{aligned} \tag{11}$$

where $\gamma = \alpha + j\beta$, in which α and β are the attenuation and phase constant of the transmission lines, respectively.

A distributed amplifier has a relaxed gain–bandwidth tradeoff compared to a lumped amplifier due to its distributed nature, where the parasitic capacitances of transistors are absorbed into the transmission lines as can be seen from (1)–(4). Also, transistor output signals add directly on the drain line as shown in (7). Therefore, the overall voltage gain can be larger than unity even when the voltage gain of each transistor may be less than one. The extended bandwidth of the distributed amplifier comes at the price of larger time delay [11]. Although this might be undesirable in certain applications, we can use it to our advantage in a distributed oscillator.

B. Distributed Oscillators

A distributed oscillator can be formed by feeding the output of a distributed amplifier (node **2**) back to its input (node **1**) as shown in Fig. 2. Intuitively, the oscillation frequency is determined by the round-trip time delay, i.e., the time it takes the wave to travel through the transmission lines and then get amplified by one of the transistors. It is noteworthy that, with the proper choice of the number of transistors and their spacing, a distributed oscillator can also generate quadrature signals.

Breaking the feedback loop at nodes **1** and **2**, the distributed oscillator reduces to the distributed amplifier of Fig. 1 with a load impedance $Z_L = Z_g$ and a source impedance of $Z_S = Z_d$. Assuming ac short circuit in the feedback path, e.g., by using a large ac coupling capacitor, the ac voltages at nodes **1** and **2** should be equal and in phase in steady state. Therefore, the large-signal gain from **1** to **2** should be 1, which can be approximately calculated from (10) by replacing the small-signal g_m with the large-signal transconductance of each transistor G_m as defined in [10]. Then, the following general oscillation condition is obtained:

$$G_m \cdot (Z_g \| Z_d) \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} = -1. \tag{12}$$

This complex equality determines both the amplitude and the frequency of the oscillation. In the special case of equal propagation properties for both lines, i.e., $\gamma l \equiv \gamma_d l_d = \gamma_g l_g$, (12) reduces to

$$G_m \cdot (Z_g \| Z_d) \cdot n \cdot e^{-\alpha n l} \cdot e^{-j\beta n l} = -1. \tag{13}$$

Assuming purely real characteristic impedance for the gate and drain lines, the last term on the left-hand side of (13) should be -1, i.e., $nl\beta = \pi$. Noting that $\beta = 2\pi f / v_{\text{phase}}$, the oscillation frequency is

$$f_o \approx \frac{v_{\text{phase}}}{2nl} \approx \frac{1}{2nl\sqrt{LC}} \tag{14}$$

where $v_{\text{phase}} \approx 1/\sqrt{LC}$ is the phase velocity in the line, and L and C are the inductance and the capacitance per unit length of the *loaded* transmission lines. Several observations can be made.

1) This expression makes intuitive sense as $2nl$ is the total length of the transmission lines in the oscillator and v_{phase} is the propagation velocity of the wave on the line. However, the signal only travels through a length of nl from node 1 to 2. The factor of 2 is caused by the 180° phase shift due to the inverting gain of transistors. Therefore, it verifies that the frequency is determined by the round-trip time delay. Furthermore, if $\gamma_d l_d \neq \gamma_g l_g$, the oscillation frequency can be determined by calculating the gate and drain line propagation delays, i.e.,

$$\begin{aligned} f_o &\approx \left(\frac{n l_g}{v_g} + \frac{n l_d}{v_d} \right)^{-1} \\ &\approx \frac{1}{n l_g \sqrt{L_g \left(C_g + \frac{c_{\text{in}}}{l_g} \right)} + n l_d \sqrt{L_d \left(C_d + \frac{c_{\text{out}}}{l_d} \right)}} \end{aligned} \tag{15}$$

where

$$\begin{aligned} v_d &\approx 1 \Big/ \sqrt{L_d \left(C_d + \frac{c_{\text{out}}}{l_d} \right)} \\ v_g &\approx 1 \Big/ \sqrt{L_g \left(C_g + \frac{c_{\text{in}}}{l_g} \right)} \end{aligned} \tag{16}$$

are the phase velocities on the loaded gate line and drain line, respectively. The accuracy of (15) is verified in Section V.

2) Equation (14) can be written as $f_o \approx 1/\sqrt{L_{\rm tot}C_{\rm tot}}$, where $L_{\rm tot} = 2nlL$ and $C_{\rm tot} = 2nlC$ are the inductance and capacitance of the entire loaded gate and drain lines. Therefore, the oscillation frequency given by (14) is approximately 2π times larger than that of a lumped oscillator with a tank inductance and capacitance of values $L_{\rm tot}$ and $C_{\rm tot}$, respectively.
3) $f_0 = \pi f_c/2n$, where $f_c = 1/(l\sqrt{LC})$ is the cutoff frequency of the loaded transmission line and represents the frequency at which no signal travels along the transmission line. This implies that for a given frequency, a larger number of smaller transistors (larger n), and hence a smaller section length l, would result in a higher f_c to f_0 ratio and hence a frequency and amplitude closer to those predicted by (14)–(16).

The magnitude part of (13) can be solved for G_m to determines the amplitude. Noting that, for amplitude $V_{\rm amp}$, much larger than quiescent gate overdrive, $V_{GS}-V_T$, the large-signal transconductance is $G_m \approx 2I_D/V_{\rm amp}$[4] [11], and hence the oscillation amplitude is given by

$$V_{\rm amp} \approx \frac{2I_D}{G_m} \approx 2nI_D(Z_g||Z_d)e^{-\alpha nl} \tag{17}$$

where $e^{-\alpha nl}$ is the loss of the full length of the transmission line and it is assumed that $Z_g||Z_d$ is real. This expression is valid for both MOS and bipolar implementations of the oscillator as long as the amplitude is large. It is noteworthy that (17) reduces to the previously known expression for the amplitude of a lumped oscillator [11] for $n = 1$.

The above analysis is based on the assumption that the transistor loading can be treated as distributed over the total length of the transmission lines. Although this is strictly valid only for a very large number of small transistors, the derived oscillation conditions are a good approximation, as shown in Section V.

III. Tuning

Frequency tuning is an essential feature whenever the oscillator is used in a phase-locked system. Usually the specified tuning range is considerably larger than the required range to accommodate for process variations and incomplete modeling and therefore it is necessary to have a large tuning range.

According to (14), the oscillation frequency is proportional to the phase velocity of the loaded transmission lines, $v_{\rm phase}$, and inversely proportional to the total length of transmission lines, $2nl$. This leads to two approaches for frequency tuning: changing the phase velocity and/or changing the effective length of the transmission lines.

A. Inherent-Varactor Tuning

The most straightforward way of changing the phase velocity is by introduction of explicit varactors on the transmission lines and hence changing the phase velocity, $v_{\rm phase} \approx 1/\sqrt{LC}$. Unfortunately, this approach suffers from a severe reduction in the oscillation frequency due to the extra zero-bias capacitance added to the lines which does not contribute to the tuning. This will cancel the advantages obtained by using a distributed structure, namely, higher operation frequency. Also the quality factor Q of the varactors significantly degrades at higher frequencies which makes them even more undesirable.

[4]This expression is valid in the case of a bipolar transistor too as long as the amplitude is much larger than kT/q.

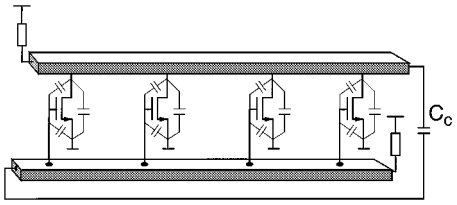


Fig. 3. Inherent-varactor tuning.

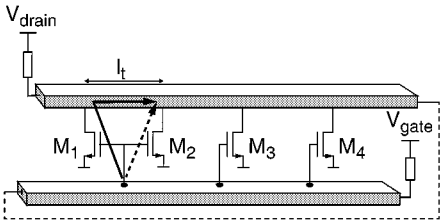


Fig. 4. Path-length adjustment tuning.

Fortunately, the parasitic capacitances of transistors can be used as inherent varactors. Therefore, by varying the dc voltage on the transistors, we can change these parasitic capacitances to tune the oscillation frequency. However, if applied blindly, the changes in the control voltage will change the dc operating point of the transistors, and thus vary their transconductance and output resistance. This will in turn change the oscillation amplitude, which is an undesirable effect. Therefore, any tuning technique should guarantee stable operation point with changes in the control voltage. This goal can be achieved by biasing the transistors using current sources.

Tuning can be achieved by adjusting the dc level of the gate line or drain line in Fig. 3, while maintaining a constant quiescent current using current source biasing, as will be shown in Section III-B. It is essential to introduce an ac coupling capacitor C_c between the drain and gate lines to be able to control the dc voltages on the two lines independently. With this modification, it is possible to change the nonlinear capacitances of transistors (such as C_{gs} and C_{gd}) as well as their transconductances, g_m, by changing the dc voltages. Changes in C_{gd} have the largest effect on the tuning range as the voltage across C_{gs} does not change significantly due to the constant current biasing scheme. Circuit simulations confirm this observation.

B. Delay-Balanced Current-Steering Tuning

An alternative way of changing the round-trip time delay is to change the length of the transmission lines. Although the physical length cannot be changed, the effective length can be varied, i.e., we can control and change the path for the waves to travel. The basic concept is shown in Fig. 4, where the gates of M_1 and M_2 are connected to the same point on the gate line while separated on the drain line by l_t. To understand the operation in this tuning mode, let us consider two extreme cases. In the first case, when M_1 is on and M_2 is off, the signal travels along the solid path. In the second extreme case when M_2 is on and M_1 is off, the signal travels along the dashed path. The latter is shorter

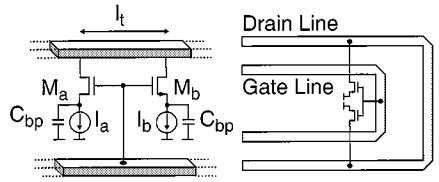


Fig. 5. Drain line tuning section.

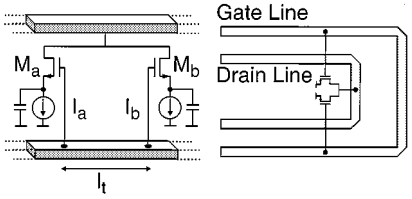


Fig. 6. Gate line tuning section.

than the former by l_t. Therefore, the round-trip time delay can be varied by selecting either the solid or dashed path, and thus the oscillation frequency can be tuned accordingly.

The path-length adjustment can be implemented by *current steering* [15]. Fig. 5 shows a section of a DVCO using such tuning technique, which we call a drain-line-tuning (DLT) section. The gain transistors M_a and M_b share the same tap point on the gate line, while their drains are connected to the drain line at two different points. The transistors are biased using current sources I_a and I_b, and their sources are ac-grounded using two bypass capacitors to maintain the high-frequency gain while suppressing the low-frequency parasitic oscillations. The bias current of each transistor is then controlled independently of the dc voltage on the gate and drain lines. The effective length of the drain line can be changed by varying the ratio of I_a and I_b to tune the oscillation frequency continuously. The difference between the minimum and maximum effective lengths of the drain line is controlled by l_t. Thus, the tuning range is determined by the ratio of l_t to the total length of transmission lines, as will be shown analytically. A "U-turn" structure can be used in the layout of a DLT to minimize the length of interconnection wires to the transmission lines and avoid extra unbalanced delay from these wires, as shown in Fig. 5.

A DVCO tuned by DLTs experiences the problem of delay mismatch as the transistor loading on the gate line is more concentrated than on the drain line. The delay mismatch is deteriorated by the fact that the gate capacitance is usually larger than the drain output capacitance. Also, the total length of the drain line is longer than the gate line if the U-turn structure is used which results in more delay mismatch. Therefore, the traveling wave on the drain line will lag the gate wave in phase. This phase mismatch between the gate and drain lines affects the oscillator"s phase condition and makes it difficult for the oscillator to maintain phase shift around the loop. In other words, it degrades the synchronization of the waves on the gate and drain lines. If not resolved, this phase mismatch will degrade the phase noise and tuning range.

To remedy this problem, the delay mismatch between the gate and drain lines must be minimized. This can be done using the structure of Fig. 6, which is complementary to that of Fig. 5 in that the gain transistors share the same drain tap point but are

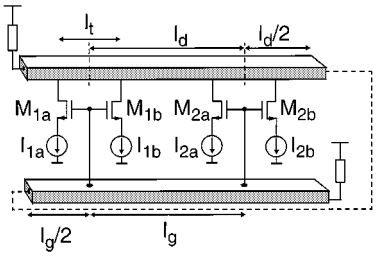


Fig. 7. DVCO using DLTs.

separated on the gate line by the same distance as the separation on the drain line of Fig. 5. We will refer to this structure as gate-line-tuning (GLT) section. A pair of these complementary sections can be used to cancel the delay mismatch. We will refer to this tuning technique as *delay-balanced current-steering tuning*.

Now we can extend the previous analysis of distributed oscillators to a DVCO using the current-steering tuning technique. For simplicity, we consider a DVCO with only DLTs (Fig. 7), assuming that there is no phase mismatch. The analysis of a delay-balanced DVCO with both DLTs and GLTs can also be performed using the same approach. The bias currents of M_a in Fig. 5 and all the similar transistors in other DLTs are the same. We will refer to these transistors as group $\mathbf{A}$ and transistor M_b and its counterparts in the other DLTs as group $\mathbf{B}$. The large-signal transconductance of each transistor in group $\mathbf{A}$ and group $\mathbf{B}$ will be shown with G_{ma} and G_{mb}, respectively. An analysis similar to that of the original distributed oscillator of Fig. 2 will be applied to both groups to find the new oscillation condition in the presence of tuning. The resultant voltage at node $\mathbf{2}$ due to the transistors of group $\mathbf{A}$ is

$$v_{2a} = -G_{ma}V_1(Z_g||Z_d)\cdot e^{-\gamma_d l_t/2}\cdot e^{-(\gamma_d l_d+\gamma_g l_g)/2} \cdot\frac{e^{-\gamma_d n l_d}-e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d}-e^{-\gamma_g l_g}}. \quad (18)$$

Similarly, for group $\mathbf{B}$

$$v_{2b} = -G_{mb}V_1(Z_g||Z_d)\cdot e^{\gamma_d l_t/2}\cdot e^{-(\gamma_d l_d+\gamma_g l_g)/2} \cdot\frac{e^{-\gamma_d n l_d}-e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d}-e^{-\gamma_g l_g}}. \quad (19)$$

Superimposing these two voltages, the following steady-state oscillation condition is obtained:

$$(G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{\gamma_d l_t/2})\cdot(Z_g||Z_d) \cdot e^{-(\gamma_d l_d+\gamma_g l_g)/2}\cdot\frac{e^{-\gamma_d n l_d}-e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d}-e^{-\gamma_g l_g}} = -1. \quad (20)$$

In the special case of $\gamma l \equiv \gamma_d l_d = \gamma_g l_g$, (20) simplifies to

$$2n(Z_g||Z_d)e^{-\gamma n l}(G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{\gamma_d l_t/2}) = -1. \quad (21)$$

Assuming that $|\gamma l_t| \ll 1$, (21) simplifies to the following expressions for frequency as shown in the Appendix:

$$f \approx \frac{v_{\text{phase}}}{2nl}\left(1+\frac{G_{mb}-G_{ma}}{G_{mb}+G_{ma}}\cdot\frac{l_t}{2nl}\right). \quad (22)$$

As can be seen from (22), as long as l_t is small compared to the total length of the transmission line, the tuning range is

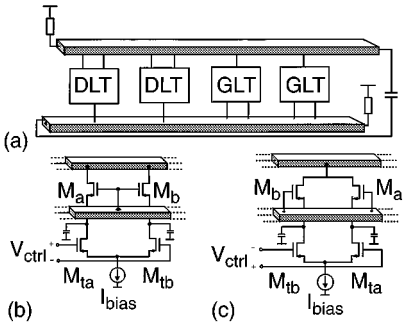


Fig. 8. Delay-balanced current-steering tuning.

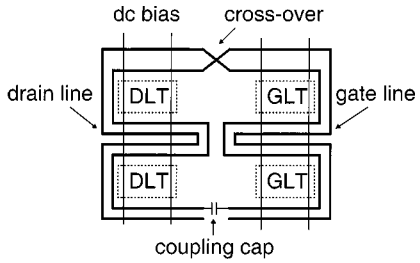


Fig. 9. Floor plan of a DVCO.

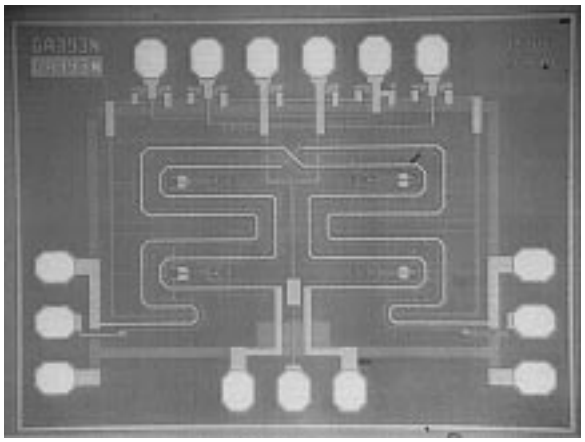


Fig. 10. Die photo of the CMOS DVCO.

directly proportional to the tuning length l_t. However, if l_t increases excessively, the phase difference between contributions from transistor groups A and B as well as the loss on l_t increase, as can be seen from (21). Both effects decrease the total loop gain and, hence, set a practical upper bound for l_t.

IV. Design and Layout

The designed DVCOs comprise two GLTs [Fig. 8(b)] and two DLTs [Fig. 8(c)], as shown in Fig. 8(a). In each section, I_a and I_b are implemented using a current source $I_{\rm bias}$ and two current steering transistors M_{ta} and M_{tb}. The differential control voltage steers the tail current between M_a and M_b. The channel lengths of transistors M_{ta} and M_{tb} should be chosen longer than the minimum channel lengths to allow for a larger and more uniform range of the differential control voltage, $V_{\rm control}$. Longer channel length also reduces the excess channel noise of these devices, which improves the phase noise of the oscillator [12], [13]. The ac coupling capacitor between the end of the drain line and beginning of the gate line is used to allow the inherent-varactor tuning. This dual differential and single-ended tuning capability allows for simultaneous coarse- and fine-tuning in a frequency synthesizer, which is useful for improving the capture range in a phase-locked loop.

An important issue in the design of DVCOs is the modeling of the transmission lines [16]. In this design, coplanar striplines are used for their high Z_0 and low loss. Full-wave EM simulations with HFSS [14] are used to extract circuit parameters for the transmission lines. The coplanar striplines have a metal thickness of 3 μm, a vertical spacing to the substrate of 4.2 μm, a signal-line width of 3 μm, a ground-line width of 8 μm, and a lateral spacing between them of 10 μm. The inductance and capacitance per unit length do not vary significantly with frequency. They are L = 0.72 μH/m and C = 81 pF/m around frequencies of interest.

Since the circuit operates at microwave frequencies and any conductive line can act as a transmission line, special attention should be paid to the layout. Fig. 9 shows the floor plan of a DVCO. A few important considerations are highlighted here. The gate and drain lines should be parallel to maintain synchronization of waves and their spacing should be large enough to lower interference. Due to the feedback path in the oscillator, a crossing where one transmission line goes underneath the other is inevitable. This crossing is implemented using both *metal*1 and *metal*2 lines to minimize the loss and compensate for the thickness difference between the top layer and the lower metal layers and thus impedance difference between the drain line and gate line. Enough vias are introduced at the crossing point to minimize the resistance. There are reverse-biased PN junctions (also known as laminations) underneath the entire transmission line structure to suppress Eddy currents in the substrate and thus lower the loss to some extent. In each section, the two gain transistors have identical distances from the tap points on the transmission lines in order not to introduce unbalanced excess delay as shown in Figs. 3 and 4. The dc bias lines pass underneath and are perpendicular to the transmission lines to minimize the capacitive loading on the lines.

V. Experimental Results

A. Test Setup

In our test setup, the chip is attached to a circuit board with conductive adhesive. The dc pads are wire-bonded to the PCB. A microwave probe station equipped with microwave coplanar probes is used to probe the RF pads on the sides. The probes are connected to the measurement instruments and bias circuitry through coaxial cables. An HP 8563E spectrum analyzer is used to measure the oscillation frequency and the output power. The measured insertion loss from the probes to the spectrum analyzer is 4.3 dB at 10 GHz and 6.3 dB at 12 GHz, respectively. Therefore, any measured power on the spectrum analyzer should be adjusted for the extra loss.

B. CMOS DVCO

A 10-GHz CMOS DVCO is fabricated in a 0.35-μm BiCMOS technology using only CMOS transistors. Fig. 10 shows its chip micrograph. It occupies an area of 1.4 mm $\times$ 1 mm, including

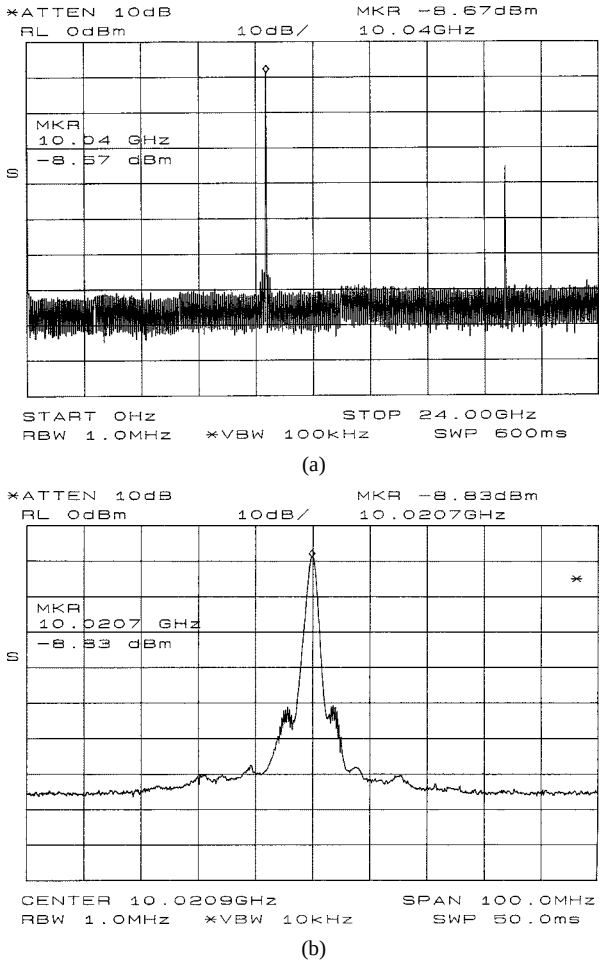


Fig. 11. Output power spectrum of the CMOS DVCO. (a) Harmonics. (b) Detailed.

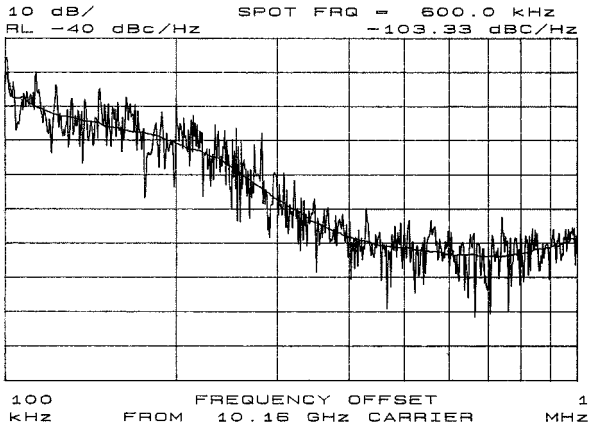


Fig. 12. Phase noise of the CMOS DVCO.

the pads. The total length of transmission lines is about 7 mm. It is noteworthy that CMOS transistors in a BiCMOS process are known to have inferior f_T compared to transistors of comparable size in pure CMOS technologies.

The measured power spectrum is shown in Fig. 11, which should be adjusted for the 4.3-dB loss in the setup. The center frequency of the oscillator is 10.0 GHz and the output power is −4.5 dBm. Fig. 12 shows the single-side-band (SSB) phase noise. The phase noise is −103 dBc/Hz at 600 kHz offset from

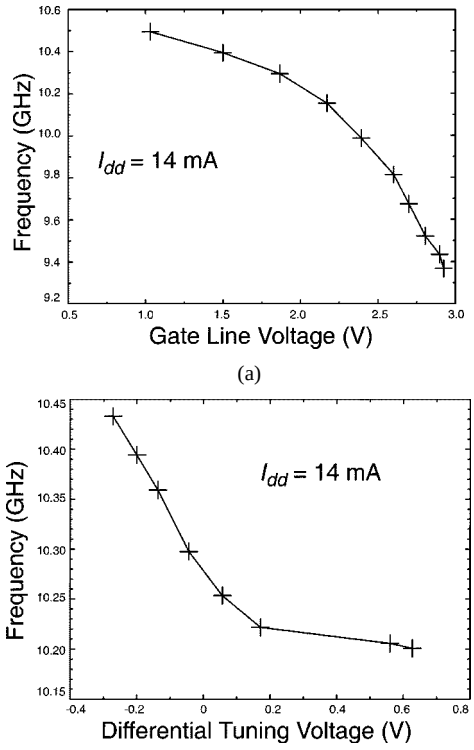


Fig. 13. Tuning of the CMOS DVCO. (a) Inherent-varactor tuning. (b) Delay-balanced current-steering tuning.

a 10.2-GHz carrier with a total drain current of 14 mA. Deterministic modulation sidebands induced by external interference can be observed in Fig. 11(b). These sidebands degrade the measured phase noise at higher offset frequency from the carrier.

A tuning range of 9% (9.5–10.4 GHz) can be obtained using the inherent-varactor tuning with a total drain current of 14 mA. The output power variation is 2.7 dB over this tuning range. If maintaining a constant output power is not required, the tuning range can be extended to 12%, as shown in Fig. 13(a). The measured tuning range of the delay-balanced current-steering tuning technique is 2.5% around the center frequency set by the inherent-varactor tuning, as shown in Fig. 13(b) for a center frequency of 10.3 GHz.

Using transmission line parameters obtained from EM simulations with HFSS ($L = 0.72$ μH/m, $C = 81$ pF/m) and the circuit parameters ($l_g = l_d = 0.9$ mm, $l_t = 0.3$ mm, $n = 4$, $C_{\text{in}} = 188$ fF/stage, $C_{\text{out}} = 152$ fF/stage), (15) predicts a center frequency of $f_0 = 9.97$ GHz, in good agreement with measurement results.

The measured output power from the gate and drain terminations versus total drain current are compared in Fig. 14. These measurements are good indicators of the oscillator"s internal voltage levels.

C. Bipolar DVCO

The 12-GHz bipolar DVCO is fabricated using the same BiCMOS process. Fig. 15 shows its chip micrograph. It occupies an area of 1.2 mm × 1 mm. The total length of the transmission lines is about 5 mm, which primarily controls the center frequency.

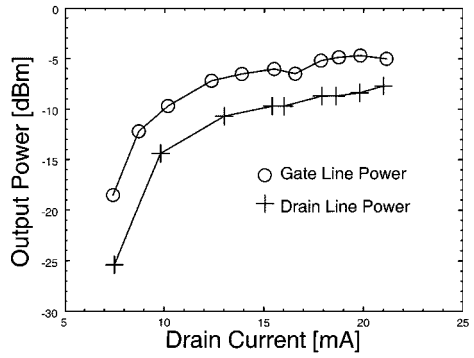


Fig. 14. Power consumption versus output power for the CMOS DVCO.

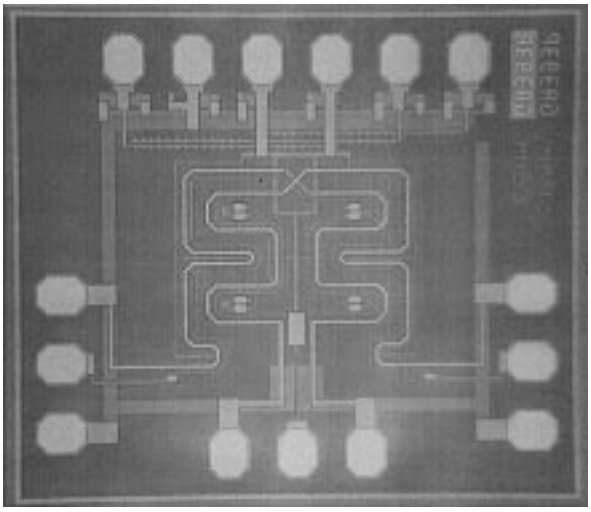


Fig. 15. Die photo of the bipolar DVCO.

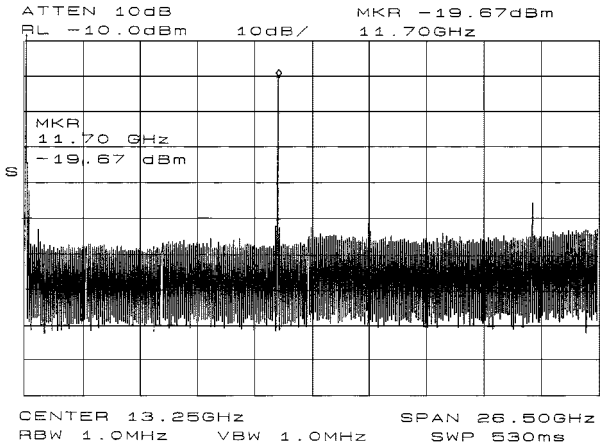


Fig. 16. Output power spectrum of the bipolar DVCO.

The measured power spectrum and phase noise spectrum of the 12-GHz DVCO are shown in Figs. 16 and 17. A phase noise of -99 dBc/Hz at 600 kHz offset from a 11.7-GHz carrier is achieved on 6-mA bias current from a 2.5-V dc supply. This power dissipation is comparable to low-power lumped VCOs operating at lower frequencies. A better phase noise can be achieved by increasing the bias current.

The inherent-varactor tuning on the collector line achieves a tuning range of 12% (10.6–12 GHz) with 2-dB output

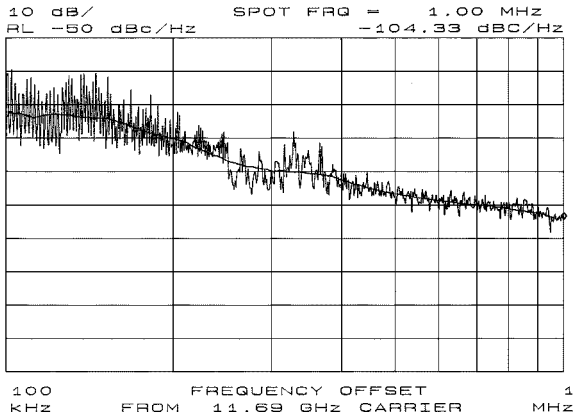
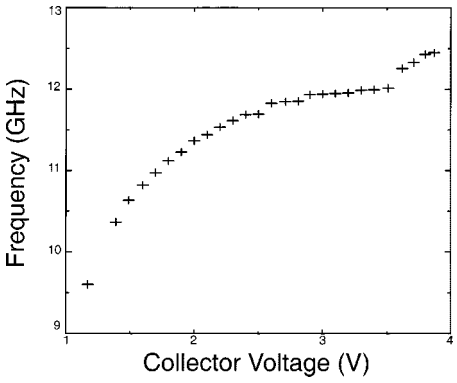
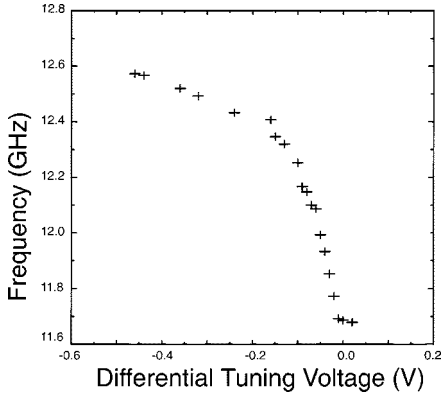


Fig. 17. Phase noise spectrum of the bipolar DVCO.



(a)



(b)

Fig. 18. Tuning of the bipolar DVCO: (a) inherent-varactor tuning and (b) delay-balanced current-steering tuning.

power variation around a center frequency of 11.3 GHz. This tuning range can be extended to 26% by tolerating larger output variation, as shown in Fig. 18(a). The delay-balanced current-steering tuning achieves a tuning range of 7.4% around the center frequency set by the inherent-varactor tuning, as shown in Fig. 18(b).

Using transmission line parameters obtained from EM simulations with HFSS ($L = 0.72$ μH/m, $C = 81$ pF/m) and the circuit parameters ($l_g = l_d = 0.6$ mm, $l_t = 0.2$ mm, $n = 4$, $C_{\text{in}} = 386$ fF/stage, $C_{\text{out}} = 116$ fF/stage), (15) predicts a center frequency of $f_0 = 11.3$ GHz, in good agreement with measurement results.

VI. Conclusion

In this paper, a systematic approach to the analysis of distributed oscillators has been presented. The general oscillation condition has been derived, leading to analytical expressions for the amplitude and frequency. The derived frequency condition also leads to two tuning approaches: inherent-varactor tuning and a novel delay-balanced current-steering tuning. In the latter approach, the effective length of the transmission line is changed by changing the signal path. The introduced problem of delay mismatch can be remedied by delay balancing via the combination of DLTs and GLTs. CMOS and bipolar DVCOs have been implemented using these tuning techniques in a 0.35-μ m BiCMOS technology. The 10-GHz CMOS DVCO achieves a tuning range of 12% (9.3–10.5 GHz) and a phase noise of -103 dBc/Hz at a 600-kHz offset from a 10.2-GHz carrier, drawing 14 mA of current from a 2.5-V supply. The 12-GHz bipolar DVCO achieves 26% of tuning range with a phase noise of -99 dBc/Hz at a 600-kHz offset from the carrier. It consumes only 6 mA from a 2.5-V supply.

Appendix

Equation (21) can be rewritten as

$$2n(Z_g||Z_d)\cdot e^{-\alpha nl} \cdot e^{-j\beta nl}(G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{\gamma_d l_t/2})=-1. \quad \text{(A1)}$$

Defining

$$\begin{aligned} Ae^{j\theta} &= G_{ma}e^{-\gamma_d l_t/2}+G_{mb}e^{\gamma_d l_t/2} \\ &= \cos\left(\frac{\beta l_t}{2}\right)(G_{ma}e^{-\alpha l_t/2}+G_{mb}e^{\alpha l_t/2}) \\ &\quad + j\sin\left(\frac{\beta l_t}{2}\right)(-G_{ma}e^{-\alpha l_t/2}+G_{mb}e^{\alpha l_t/2}) \end{aligned} \quad \text{(A2)}$$

where

$$\theta \approx \tan\theta = \tan\left(\frac{\beta l_t}{2}\right)\cdot\frac{G_{mb}e^{\alpha l_t/2}-G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2}+G_{ma}e^{-\alpha l_t/2}}. \quad \text{(A3)}$$

Assume that $\beta l_t \ll 1$, then the frequency condition becomes

$$-\beta nl+\frac{\beta l_t}{2}\cdot\frac{G_{mb}e^{\alpha l_t/2}-G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2}+G_{ma}e^{-\alpha l_t/2}}=-\pi. \quad \text{(A4)}$$

The frequency is given by

$$\begin{aligned} f &\approx \frac{v_{\text{phase}}}{2}\left(nl-\frac{l_t}{2}\,\frac{G_{mb}e^{\alpha l_t/2}-G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2}+G_{ma}e^{-\alpha l_t/2}}\right)^{-1} \\ &\approx \frac{v_{\text{phase}}}{2nl}\left(1+\frac{l_t}{2nl}\,\frac{G_{mb}e^{\alpha l_t/2}-G_{ma}e^{-\alpha l_t/2}}{G_{mb}e^{\alpha l_t/2}+G_{ma}e^{-\alpha l_t/2}}\right). \end{aligned} \quad \text{(A5)}$$

If we further assume $\alpha l_t \ll 1$, (A5) can be simplified as

$$f \approx \frac{v_{\text{phase}}}{2nl}\left(1+\frac{G_{mb}-G_{ma}}{G_{mb}+G_{ma}}\cdot\frac{l_t}{2nl}\right). \quad \text{(A6)}$$

Acknowledgment

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