# A Rail-To-Rail Input Receiver Employing Successive Regeneration and Adaptive Cancellation of Intermodulation Products

Edward A. Keehr and Ali Hajimiri

California Institute of Technology, Pasadena, CA 91125

*Abstract* — **A direct conversion receiver is demonstrated which operates in the presence of a rail-to-rail (+12.4dBm) out-of-band blocker and a -16.3dBm blocker, where the ICP1 is +12.5dBm and the uncorrected extrapolated IIP3 is +33.5dBm. IM distortion is adaptively cancelled via feedforward loops which are digitally expanded to reproduce higher order nonlinear reference terms. Cancellation improves input-referred total IM distortion by over 24dB, resulting in an extrapolated IIP3 of +45.3dBm.**

*Index Terms* — **Adaptive equalization, feedforward cancellation, mixed-signal linearization, nonlinear circuits, RF receivers, wireless communications.**

## I. INTRODUCTION

Throughout the history of radio, receivers and their blocks have been considered to exist within the realm of small-signal circuit design. Metrics such as ICP1 were meant to denote boundaries on the regions of operation and typically limited the maximum signal handling of the receiver input to less than 1V. In this work, we propose a method to overcome these limitations and implement a radio receiver that operates in the large-signal regime.

## II. SYSTEM CONCEPTS

The concept by which the proposed receiver accomplishes large signal operation is an extension of that presented in [1]. Such a receiver would need to handle the presence of many higher-order intermodulation (IM) products generated from a large input signal. The dominant IM products are regenerated at RF in an alternate nonlinear receiver path, downconverted, digitized, and finally used to cancel IM products in the nominally linear (main) receiver path via adaptive filtering. Shown in Fig. 1, the proposed receiver contains two nonlinear receiver paths, corresponding to even and odd order IM products. Once downconverted and digitized, the even and odd order IM products can be successively multiplied in the digital domain to regenerate higher order IM products.

For example, IM2 products can be squared to generate an approximation to IM4 products. IM2 and IM3 products can be multiplied to generate an approximation to IM5 products.
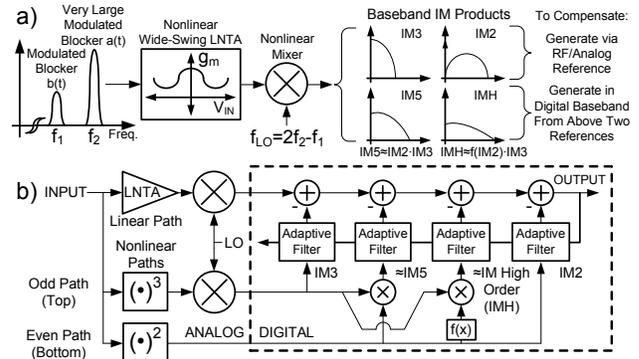


Fig. 1. Successive regeneration and adaptive feedforward cancellation of IM products at baseband implemented in this work. a) Concept. b) Simplified system block diagram.

This approximation approaches an equality when one of the blocker signals is much larger than all of the rest. As illustrated in Fig. 1, two blocker signals with complex envelopes $a(t)=a_I(t)+ja_Q(t)$ and $b(t)=b_I(t)+jb_Q(t)$ generate a number of different baseband IM products. Dropping the *(t)* for brevity, the baseband nonlinear terms can be derived:

$$IM\,2 \propto a_I^2 + a_Q^2 + b_I^2 + b_Q^2 \tag{1}$$

$$IM\,3_I \propto a_I^2 b_I + 2a_I a_Q b_Q - a_Q^2 b_I \tag{2}$$

$$IM\,3_Q \propto -a_I^2 b_Q + 2a_I a_Q b_I + a_Q^2 b_Q \tag{3}$$

The IM4 and IM5 terms in the linear path are:

$$IM\,4 \propto IM\,2^2 + 2(a_I^2 + a_Q^2)(b_I^2 + b_Q^2) \tag{4}$$

$$IM\,5_I \propto IM\,3_I((a_I^2 + a_Q^2) + \tfrac{3}{2}(b_I^2 + b_Q^2)) \tag{5}$$

$$IM\,5_Q \propto IM\,3_Q((a_I^2 + a_Q^2) + \tfrac{3}{2}(b_I^2 + b_Q^2)) \tag{6}$$

While the IM4 and IM5 reference terms are:

$$IM\,4_{REF} \propto IM\,2^2 \tag{7}$$

$$IM\,5_{I,REF} \propto IM\,3_I\,IM\,2 \tag{8}$$

$$IM\,5_{Q,REF} \propto IM\,3_Q\,IM\,2 \tag{9}$$

It can be seen that as the ratio $|a(t)|/|b(t)| \rightarrow \infty$, the reference terms approach the linear path corruptive terms and at this point large cancellation ratios can be achieved.

Some strong nonlinearities may not be well-represented by a truncated polynomial basis of intermodulation products. In this case, the IM2 terms may be modified by a fixed look-up table (LUT) representing a static function $f(x)$ prior to multiplication with IM3 terms.

Although the proposed receiver only achieves large cancellation ratios for large ratios of $|a(t)|/|b(t)|$, it is important to note that this condition is precisely the same as that of many important nonlinear blocking problems. For example, in FDD communications systems with relaxed PA/LNA isolation, the TX leakage appears as the dominant blocker to the receiver. Implantable medical sensors that receive power wirelessly may also need to demodulate a small data signal in the presence of a dominant power transfer signal [2]. In addition, radar systems can benefit from being able to handle a single very large intentional jamming signal.

## III. RF/ANALOG RECEIVER ARCHITECTURE AND CIRCUITS

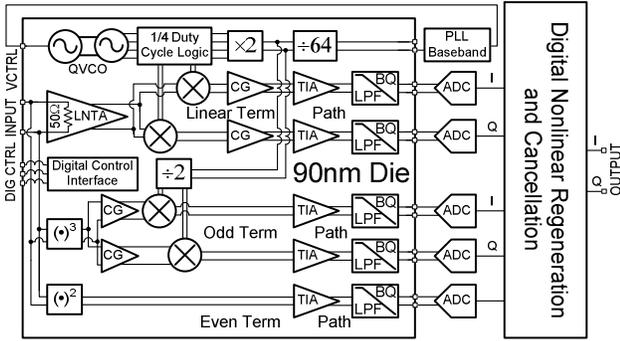### A. Linear Path Receiver Architecture



Fig. 2. Proposed receiver architecture.

Figure 2 shows the architecture of the complete receiver and block diagram of the RF front end. In order to maximize the large-signal handling capability of the receiver, the input signal is immediately converted into current by a low-noise transconductance amplifier (LNTA). This current is then directly converted by a set of quadrature passive mixers to baseband, where it is filtered by large capacitors. In order to isolate the I and Q downconversion chains with minimal voltage swing at the LNTA output, a ¼-phase passive mixer scheme was used.

The noise generated by the transimpedance amplifier (TIA) in a passive mixer system is a well-known problem in cases such as this, where the impedance looking back up into the passive mixer is low. In order to provide a high

input impedance to the TIA, it is preceded by a common-gate (CG) buffer, thereby lowering its effective noise contribution. A 2nd-order active RC biquad (BQ) was utilized to both buffer the TIA and to complete a 3rd-order Chebychev low-pass anti-aliasing filter.

The VCO oscillates at the LO frequency in order to minimize the out-of-band phase noise floor for a given power dissipation. This is an atypical choice due to the fact that it promotes LO-RF and RF-LO coupling, increasing DC offset and decreasing IIP2, respectively. However, in this architecture DC offset is compensated by adding a differential static current to the first OTA virtual ground in the BQ. IM2 products are ultimately cancelled using the scheme described in Section II.

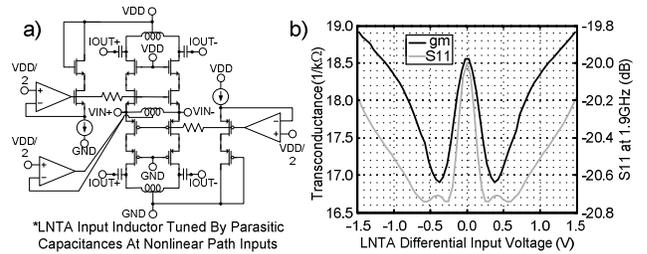### B. Linear Path Receiver Circuits



Fig. 3a. Simplified LNTA schematic showing biasing OTAs.
Fig. 3b. Static LNTA simulations: differential $g_m$ and $S_{11}$ as a function of differential input voltage, for Vdd=1.5V.

A differential rail-to-rail input receiver accommodates a signal at its input whose amplitude is nearly equal to the supply voltage before reaching ICP1. To accomplish this task, a push-pull CG-LNTA is introduced in Fig. 3a. The transconductance (and hence input impedance) remains relatively constant over a rail-to-rail input, as shown in Fig. 3b, guaranteeing that the absolute magnitude of odd-order IM products generated for large signals also remains roughly constant. However, because this transconductance function is not well-approximated by a truncated polynomial basis, the digital back-end must use LUTs representing exponential functions of the form $f(x)$, $g(x) = e^{-|k|x}$ to compensate for IM products produced in the LNA.
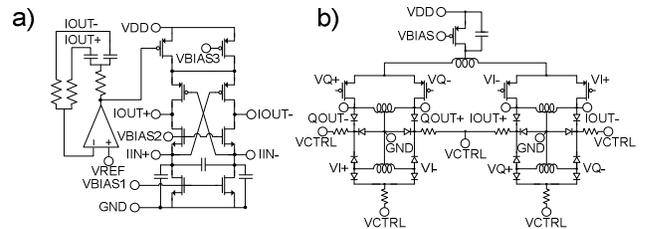


Fig. 4a. TIA CMOS common gate buffer schematic.
Fig. 4b. VCO schematic.

The current gain of the CG buffer preceding the TIA is nearly doubled by using a cross-coupled CMOS architecture, shown in Fig. 4a, in which the CG-device current is re-used in a pair of PMOS common-source amplifiers. The buffer's large center capacitor of 335pF filters out large downconverted blocker signals. Reciprocal mixing noise due to the very large blocker and VCO phase noise is addressed via the use of the Q-doubling dual-LC tank 90° phase-shift QVCO shown in Fig. 4b. As described in [3], the dual tanks provide additional filtering of out-of-band phase noise.

### C. Nonlinear Path Receiver Architecture and Circuits

In contrast to the architecture presented in [1], the nonlinear path inputs are derived directly from the receiver input, as this is the only point in the receiver at which some version of the RF input is commonly available as a voltage of appreciable magnitude. The odd path IM term generator utilizes a multistage architecture as in [4] but with a CMOS input stage in order to increase the dynamic range for a given current. The even path IM term generator consists of a buffered canonical squaring transconductor that feeds directly into a TIA.
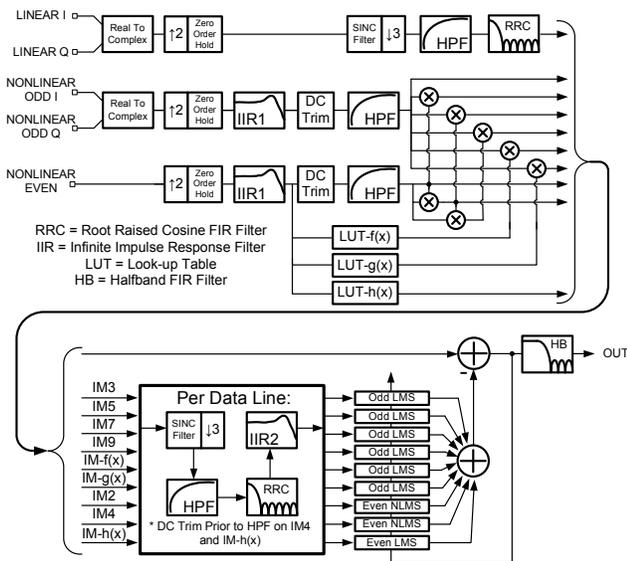


Fig. 5.    Digital back end architecture.

### IV. DIGITAL BACK END

The analog outputs of the receiver are captured by 12 bit discrete ADCs running at 25MHz. For this proof-of-concept demonstration, the digital back end (DBE) is implemented in a fixed-point software model, with its architecture shown in Fig. 5. The nonlinear path inputs are

upsampled and filtered prior to successive nonlinear reference generation to ensure that unwanted higher-order nonlinear terms do not alias into the signal band. This filtering also compensates for the small amount of group delay distortion present in the nonlinear path baseband filtering. After this process is complete, an approximate digital model of the analog linear path baseband filter removes undesired residue from these operations and helps to better match the linear and nonlinear paths.

The remaining difference between the linear and nonlinear path transfer functions is fine-tuned via LMS adaptive equalizers modified to compensate for I/Q mismatch [1]. Quantized-NLMS adaptive equalizers [1] modified to divide by the square root of the norm were placed on the IM2 and IM4 lines to reduce gradient noise amplification for large signal levels. A function $h(x)=tanh(k \cdot x)$ in the even order path was found to improve cancellation performance. The exponential functions $f(x)$ and $g(x)$, along with $h(x)$, are implemented with 256-element LUTs. The complete nonlinear path circuitry utilizes 39 and 342 16-bit multipliers running at 50MHz and 16.66MHz, respectively. Based on the results of [5] and assuming that the multipliers dominate the power consumption, the extra digital circuitry and adaptive filters would consume about 12mA and 41.5mA under a 1.3V supply for the even and odd nonlinear paths, respectively. In practice, these quantities would be dramatically reduced by time-averaging, as correction is only required under infrequent blocking conditions.

### V. MEASUREMENT RESULTS



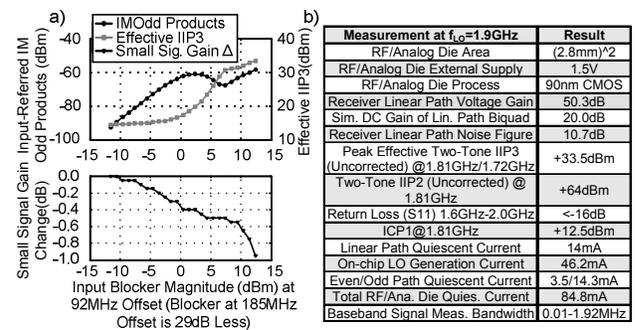| Measurement at $f_{LO}$=1.9GHz | Result |
|---|---|
| RF/Analog Die Area | (2.8mm)^2 |
| RF/Analog Die External Supply | 1.5V |
| RF/Analog Die Process | 90nm CMOS |
| Receiver Linear Path Voltage Gain | 50.3dB |
| Sim. DC Gain of Lin. Path Biquad | 20.0dB |
| Receiver Linear Path Noise Figure | 10.7dB |
| Peak Effective Two-Tone IIP3 (Uncorrected) @1.81GHz/1.72GHz | +33.5dBm |
| Two-Tone IIP2 (Uncorrected) @ 1.81GHz | +64dBm |
| Return Loss (S11) 1.6GHz-2.0GHz | <-16dB |
| ICP1@1.81GHz | +12.5dBm |
| Linear Path Quiescent Current | 14mA |
| On-chip LO Generation Current | 46.2mA |
| Even/Odd Path Quiescent Current | 3.5/14.3mA |
| Total RF/Ana. Die Quies. Current | 84.8mA |
| Baseband Signal Meas. Bandwidth | 0.01-1.92MHz |

Fig. 6a.    Two-CW tone IIP3 test: measured input referred error, effective IIP3, and ICP1 of standalone RF/Analog die.
Fig. 6b.    Baseline receiver performance metrics.

The non-monotonic nature of the LNTA nonlinearity is apparent in the results of the two-tone measurement shown in Fig. 6a. In this case, a large CW blocker at 92MHz LO frequency offset is swept with a smaller blocker at 185MHz offset while the LO is set to run at

1.9GHz. As predicted in Section IIIb, although the small signal gain of the receiver is negligibly reduced, the magnitude of the IM products at the output remains roughly constant. By extrapolating at each point of the sweep, an effective IIP3 metric can be obtained, reaching a peak of +33.5dBm for a rail-to-rail blocker at the input.
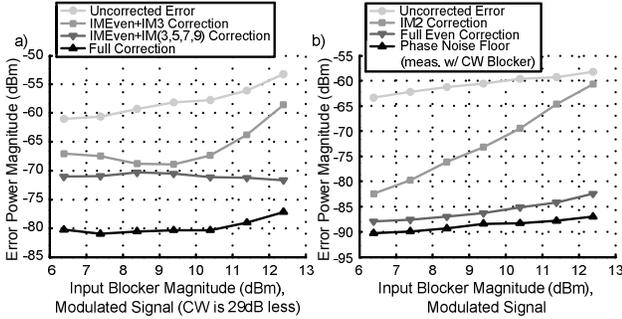


Fig. 7. Measured input-referred error with various degrees of cancellation. a) Even and odd order cancellation for two-signal blocking. b) Even order cancellation for large QPSK-modulated blocker and phase noise floor (measured with a CW blocker).

The linearity performance of the receiver is also tested under modulated blocking conditions by applying a large QPSK signal at 2MSPS along with a smaller CW blocker at LO offsets of 92 MHz and 184 MHz, respectively. The measured cancellation performance for different levels of applied correction is shown in Fig. 7. At the worst-case full-correction value in Fig. 7a, an extrapolated IIP3 metric of +45.3dBm is obtained after de-embedding residual even-order products. The correction performance for peak blocking as a function of QPSK modulation bandwidth is shown in Fig. 8a, while the convergence behavior of the adaptive algorithm is shown in Fig. 8b.
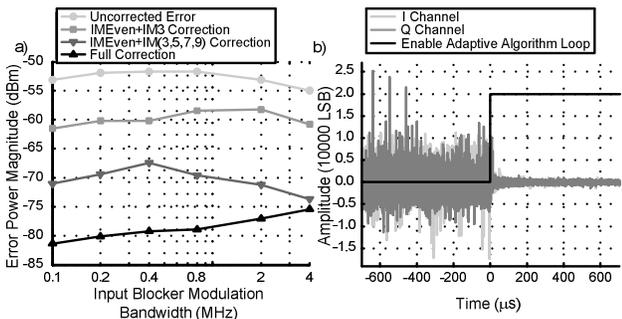


Fig. 8. a) Measured input-referred error as function of modulation bandwidth for +12.4dBm QPSK blocker / -16.3dBm CW blocker. b) Convergence behavior of full adaptive algorithm for +11.4dBm 2MSPS QPSK blocker / -16.3dBm CW blocker.

The RF/Analog die is shown in Fig. 9. The chip is fully ESD protected and is controlled by a digital interface.

## VI. CONCLUSION

A large-signal handling direct conversion receiver has been demonstrated in a 90nm RF CMOS technology. It achieves an out-of-band ICP1 of +12.5dBm and a peak uncorrected IIP3 of +33.5dBm. Adaptive feedforward cancellation of modulated IM products yields over an order of magnitude improvement in input-referred error.
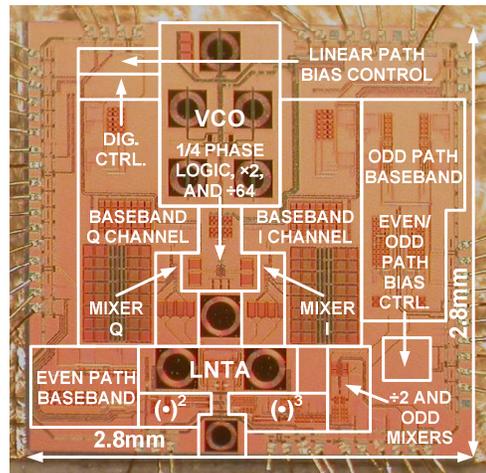
Fig. 9.    RF/Analog chip die photo.

## REFERENCES

[1] E. A. Keehr and A. Hajimiri, "Equalization of Third-Order Intermodulation Products in Wideband Direct Conversion Receivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2853-2867, Dec. 2008.

[2] W. Liu, M. Sivaprakasam, G. Wang, M. Zhou, J. Granacki, J. Lacoss, and J. Wills, "Implantable Biomimetic Microeletronic Systems Design," *IEEE Engineering in Medicine and Biology Magazine*, pp. 66-74, Sept. 2005

[3] A. M. ElSayed and M. I. Elmasry, "Low-Phase-Noise *LC* Quadrature VCO Using Coupled Tank Resonators in a Ring Structure," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 701-705, Apr. 2001.

[4] E. A. Keehr and A. Hajimiri, "Analysis of Internally Bandlimited Multistage Cubic-Term Generators for RF Receivers," *IEEE Trans. Circuits and Systems - I*, vol. 56, no. 8, pp. 1758-1771, Aug. 2009.

[5] S.K. Hsu, S.K. Mathew, M. A. Anders, B. R. Zeydel, V. G. Oklobdzija, R. K. Krishnamurthy, S. Y. Borkar, "A 110 GOPS/W 16-bit multiplier and reconfigurable PLA loop in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 256-264, Jan. 2006.