Design of a Novel Low-Power 4th-Order 1.7GHz CMOS Frequency Synthesizer for DCS-1800

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Abstract – A low-power fully-integrated type-2 4th-order 1.7GHz CMOS frequency synthesizer for DCS-1800 application is designed and simulated in a 0.25µm process technology. The frequency switching is achieved using a novel architecture exploiting a direct digital synthesis (DDS) device as the frequency reference. The new topology significantly lowers the undesired sideband power due to divider ratio switching by directly shifting the frequency of the DDS reference. The frequency synthesizer (excluding the DDS device) dissipates only 9mW of power from a 2V power supply. It employs a fast-switching novel charge pump circuit and a low-noise fully-integrated differential LC voltage controlled oscillator using on-chip spiral inductors and accumulation-mode capacitors to meet the requirements of a DCS-1800 system. A detailed analysis of the phase noise in the 4th-order loop is presented.

I. Introduction

Due to recent advances in analog integrated circuits, direct digital synthesizers (DDS) have become faster and more easily accessible [1]. They produce a low-noise output with small undesired sideband power. Therefore, they can be used as the reference frequency for a phase-locked loop directly controlling the output frequency. This is possible since a DDS device uses a sine look-up table and a digital to analog converter to achieve output frequency control to parts in billion [2].

Using a direct digital synthesizer as the reference in a phase-locked loop allows us to use a fixed frequency division ratio in both transmit and receive modes of operation and eliminates the need to change the division ratio continuously to achieve an intermediate output frequency. Therefore, there is no need to perform complex operations such as dithering or delta-sigma noise shaping in frequency division chain to minimize the spurious power. This new frequency synthesizer architecture, depicted in Fig. 1, totally eliminates the close-in sidebands due to constant switching of the frequency division ratio common in fractional-*N* frequency synthesizers. Although general purpose DDS devices are power hungry, a special purpose DDS can be used in the architecture proposed in Fig. 1.

II. System Level Modeling of the Loop

Due to the switching-mode operation of the charge pump circuit, the frequency synthesizer should be modeled as a discrete-time system. Although it is possible to perform a discrete time analysis of the loop in *Z*-domain, more insight can be achieved by using a continuous time approximation. If the loop bandwidth is much less than the input frequency, we can assume, that the state of the PLL changes by a small amount during each input cycle. Using the "average" values of the discrete-time parameters, our frequency synthesis loop can be approximately modeled using the system level representation of Fig. 2. Because of its linear behavior, we can model the phase-frequency detector (PFD) and the charge pump circuit as the cascade of a summing node and a gain stage. A phase error of $\phi_e=\phi_{ref}-\phi_{div}$ results in an average charge pump current $I_e=I.\phi_e/(2\pi)$. The current times the input impedance Z of the loop filter gives the voltage on the input node of the filter. Further, there is an extra pole contributed by the 4th-order loop filter that can be modeled by the transfer function $T(s)$. Therefore the VCO control voltage is related to the phase difference at the input of the PFD through the product of $Z(s)$ and $T(s)$.

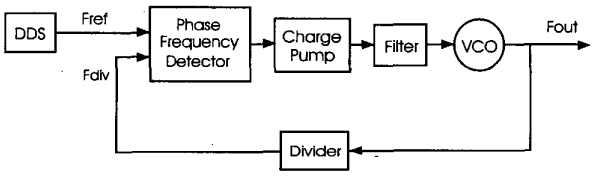

Fig. 1. Block diagram of the frequency synthesizer.

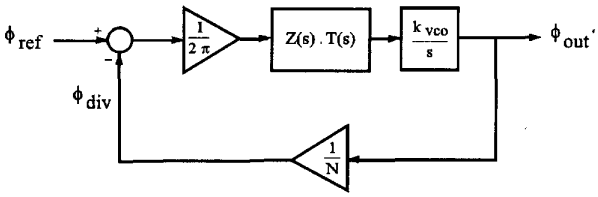

Fig. 2. System level model of the PLL

III. Building Blocks

a.) Direct Digital Synthesizer (DDS)

Although the DDS device was not implemented in our design, the expected power consumption of a DDS optimized for the proposed synthesizer using standard digital CMOS process technology, is less than 20mW. This estimate is based on the power consumption and specifications of general purpose single-chip DDS devices commercially available [2].

b.) Phase-Frequency Detector (PFD)

The phase frequency detector (PFD) schematic is shown in Fig. 3. It generates up and down outputs that have a certain minimum width, even when the phase difference is zero to eliminate the dead-zone in the phase-voltage transfer characteristic of the phase

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detector. This allows the loop to track small changes in the reference while the loop is in lock [3].

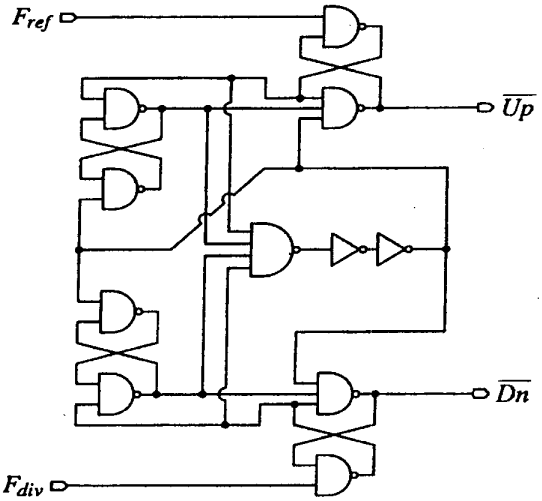

Fig. 3. Phase-frequency detector without dead zone.

c.) Charge Pump

A simplified schematic of the charge pump is shown in Fig. 4. The upper and lower branches of the charge pump are both driven differentially to achieve better matching between the switching times and allow for a current steering scheme formed by the input differential pair M_1-M_2, current mirror load M_3 and the output current source M_4. A similar circuit is used to discharge the filter capacitors and to increase the output frequency of the VCO. A longer duration of the **down** pulse results in a net charge being deposited on the loop filter capacitor which will in turn decrease the oscillation frequency and *vise versa* for a longer **up** pulse duration. The output of the phase frequency detector is single-ended and has to be converted to differential to drive the differential pairs. This is achieved by driving charge pump inputs by a complementary clock generated by Shoji's delay-balanced chain [4], which consists of two inverter chains with two and three inverter stages to match delays over process variations.

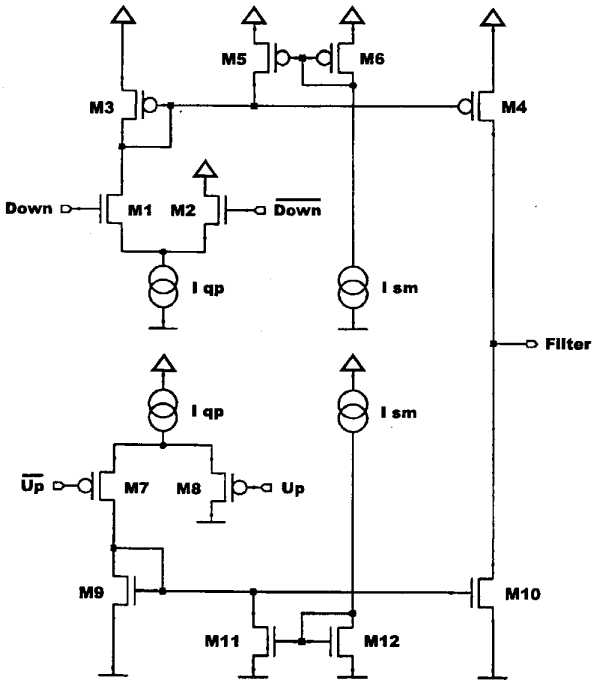

Fig. 4. Simplified schematic of the charge pump circuit.

In the absence of the bleed current sources formed by M_5 and M_6, the switching time of the mirror branch will be determined by the current-dependent time constant of the diode-connected transistors M_3. This will slow down the operation of the charge pump and degrade the output waveform. To mitigate this problem, a small bleed current branch is added to expedite the switching of the current mirror and pull up the gate of M_3 and M_4. When the down signal is high, the current I_{qp} is steered through M_1. The difference $I=I_{qp}-I_{sm}$ flows in M_3 and is mirrored to the output device M_4. When the down signal is low, the current in M_3 goes to zero quickly.

This charge pump topology is capable of generating well-controlled short current pulses compared to other charge pump topologies at the expense of some quiescent power dissipation due to current sources I_{qp} and I_{sm}. This is certainly well justified as the pulse matching directly affects the spurious performance of the frequency synthesizer.

d.) Loop Filter

Fig.5. shows the schematic of the 4th-order loop filter used. The higher order reduces the total capacitance which occupies most of the chip area and also lowers the reference spurious sidebands in the output. The filter was designed for the receive path (divider ratio N=4*53=212). A passive filter was chosen to avoid phase noise degradation due to device $1/f$ noise.

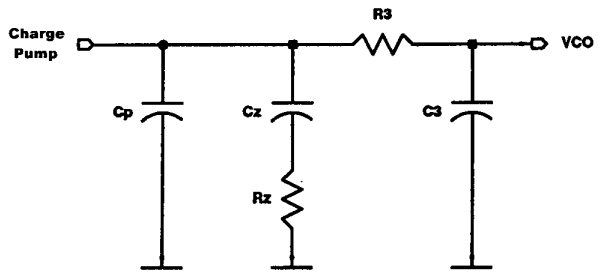

Fig. 5. Loop filter

e.) Frequency Divider Chain

The frequency divider consists of a prescaler circuit and a programmable counter. The prescaler consists of 2 Master-Slave flip-flops to divide by 4. Two D-Latches similar to those in Fig. 6. are cascaded to form a master-slave flip-flop for the prescaler.

The lower tree differential pair, M_1-M_2 steers the current between the amplification and regeneration branches. M_7 and M_8 act as load for both pairs. When CLK+ is high, the differential pair M_3-M_4 amplifies the input, but when it switches to low, the

regenerative pair latches the input data. The prescaler is followed by a counter which can divide by 45 or 53 (so it can be used for both transmit and receive paths), consists of 6 differential RS-flip flops and some logic to reset them and to form a nearly symmetric input signal for the phase-frequency detector with a high/low ratio of 22/23 or 26/27.

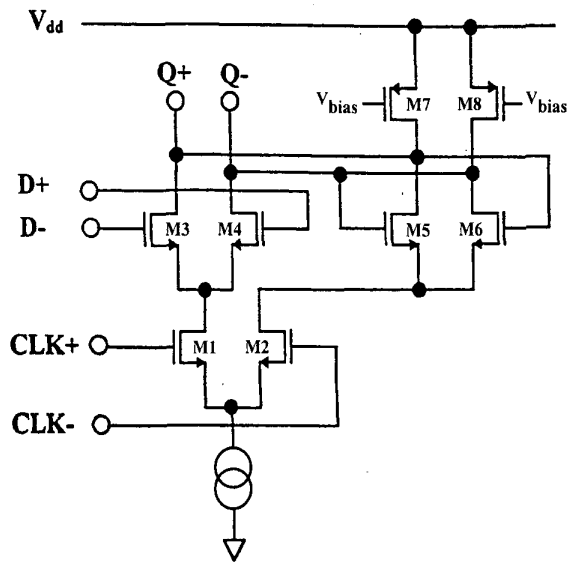

Fig. 6. D-Latch in prescaler circuit

f.) Voltage Controlled Oscillator

The VCO is a fully-integrated differential cross-coupled inductance-capacitance (LC) voltage controlled oscillator. The LC-tank consists of an on-chip spiral inductor and uses accumulation-mode varactors for tuning. Patterned ground shields (PGS) are employed to increase the quality factor of the spiral inductor. The tuning characteristic is quite linear and shows a k_{vco}=3.05x10^9 rad/V at 1.7GHz. A phase noise of −118.5dBc/Hz at 600kHz offset from the 1.7GHz carrier is predicted dissipating only 6mW of power in a 0.25μm process technology. The open-loop phase noise of the oscillator was simulated with SpectreRF and is shown in Fig. 7 as the dotted line.

IV. Phase Noise Performance

To calculate the total phase noise at the output of the system, the effect of various noise sources has to be examined. The phase noise contributions of the frequency divider is small and is therefore neglected in the following calculation. Because of the high order of the loop, this noise source is significantly suppressed at frequencies larger than the loop bandwidth. Phase noise due to R_z is calculated to be

$$\mathcal{L}_{Rz}(s)=\frac{4k_bTR_z}{2\pi}\cdot\frac{1}{2}\cdot\left[\frac{P_1(s)}{P_1(s)+R_z+\frac{1}{sC_z}}\right]^2\cdot\left[\frac{T(s)\cdot\frac{kvco}{s}}{1+Z(s)\cdot T(s)\cdot\frac{kvco\cdot I}{2\pi Ns}}\right]^2$$

The first term represents the power spectral density of R_z in terms of $\Delta\omega$, and the factor ½ is to calculate the double sideband power spectrum. To get the systems output phase noise, this has to be multiplied by the square of the transfer function from the noise source to the output. $P_1(s)$ is the impedance of $(R_3+C_3)//Cp$. The phase noise due to R_3 can be calculated in the same fashion to be:

$$\mathcal{L}_{R3}(s)=\frac{4k_bTR_3}{2\pi}\cdot\frac{1}{2}\cdot\left[\frac{R_3+\frac{1}{sC_3}}{P_2(s)+R_3+\frac{1}{sC_3}}\right]^2\cdot\left[\frac{T(s)\cdot\frac{kvco}{s}}{1+Z(s)\cdot T(s)\cdot\frac{kvco\cdot I}{2\pi Ns}}\right]^2$$

with $P_2(s)$ as impedance of $(R_z+C_z)//C_p$. The noise of a single MOS transistor is approximately given by

$$\frac{i_n^2}{\Delta\omega}=\frac{4k_bT\gamma}{2\pi}\cdot\mu\cdot C_{ox}\frac{w}{l}(V_{GS}-V_T)$$

where γ is the excess noise factor and is around 2 for a short channel device. By adding the uncorrelated noise sources in the transistors of the charge pump, we can calculate the resulting phase noise contribution to be:

$$\mathcal{L}_{CP}(s)=\sum\left(\frac{i_n^2}{\Delta\omega}\right)\cdot\Delta t\cdot f_{ref}\cdot\frac{1}{2}\cdot\left[\frac{Z(s)\cdot T(s)\cdot\frac{kvco}{s}}{1+Z(s)\cdot T(s)\cdot\frac{kvco\cdot I}{2\pi Ns}}\right]^2$$

where Δt is the pulse width of the **up** and **down** signals in locked condition, which is about 0.5ns in our design. $\Delta t\cdot f_{ref}$ is the fraction of time during which the charge pump is active.
The resulting closed loop phase noise due to the VCO is:

$$\mathcal{L}_{VCO}(s)=\left(\frac{\phi_n^2}{\Delta\omega}\right)_{VCO}\cdot\left[\frac{1}{1+Z(s)\cdot T(s)\cdot\frac{kvco\cdot I}{2\pi Ns}}\right]^2$$

and the noise from the DDS device has to be multiplied by the

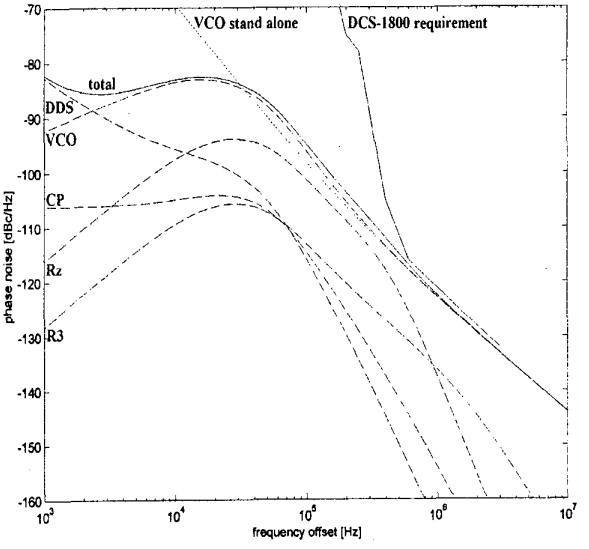

Fig.7. Output phase noise due to various sources

square of the forward transfer function. Note that the phase noise data from [2] is used in Fig.7. The sum of all these uncorrelated noise sources gives the total phase noise at the output, which is shown in Fig. 7.

The filter components were chosen to meet the phase noise requirements for DCS-1800 system, *i.e.*, -116dBc/Hz@600kHz and -132dBc/Hz@3MHz offset from the carrier. Phase noise at 600kHz offset is dominated by the VCO and the filter resistors. But lower resistors require larger capacitors to get a stable system. Since the loop filter capacitors occupy most of the chip area, they should be small to reduce manufacturing costs in mass production. The loop filter components have been chosen to satisfy these contradictory requirements as described in the next section.

V. Loop Parameters

The design of a PLL involves trade-offs between stability, locking time, chip area, phase noise, spurious response, loop bandwidth and power consumption. Design variables in this PLL are the loop order, the divider ratio N, the charge pump current I, and the values of the resistors and the capacitors in the filter. The following are the values in the final design:

C_z=9nF	C_p=450pF	C_3=450pF	
R_3=400Ω	R_z=1.6kΩ	I=75μA	N=212

The die area for the loop filter capacitors is about 1.5mm^2. The DDS output varies from 7.824MHz to 8.176MHz (step size: 943.4Hz) which leads to the required VCO output from 1658.6MHz to 1733.6MHz (step size: 200kHz) and the loop bandwidth is 52kHz.

VI. Simulations

Fig. 8. shows the simulated VCO control voltage when a frequency step is applied to the reference source. The frequency error becomes smaller than 20kHz after about 150μs (locking time), which is

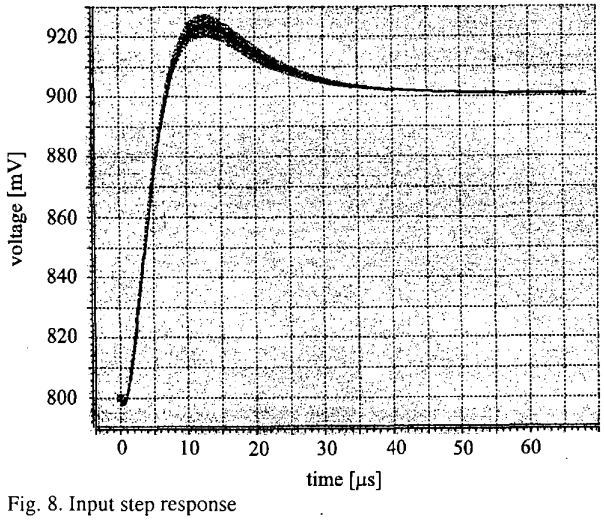

Fig. 8. Input step response

significantly smaller than the available time slot of 577μs in DCS-1800.

Due to the finite length of closed-loop simulations performed in SPICE (70μs), the frequency domain spectrum obtained by the FFT (Fast Fourier Transformation) analysis has a numerical noise floor of about –70dBc. Fig. 9 shows the spectrum obtained this way. As can be seen there are no spurious sidebands above –70dBc and therefore the spurious response is better than –70dBc mainly due to the novel balanced charge pump circuit.

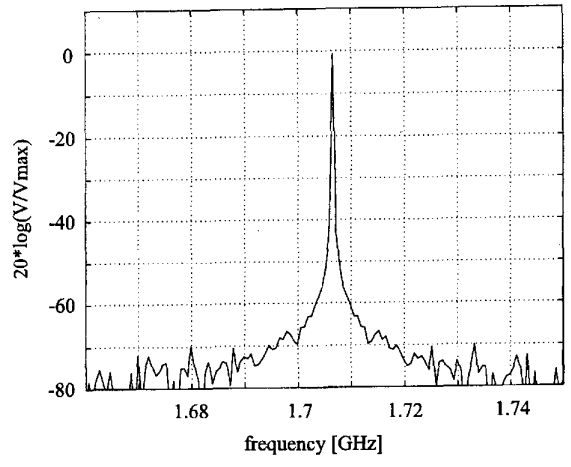

Fig. 9. Simulated output spectrum of the frequency synthesizer

VII. Conclusion

A low-power fully-integrated type-2 4th-order 1.7GHz CMOS frequency synthesizer for DCS-1800 application is design in a 0.25μm process technology. Frequency switching is achieved using a novel frequency synthesis loop exploiting a direct digital synthesizer and a PLL. A novel charge pump circuit is used to minimize the undesired sideband power. The frequency synthesis loop dissipates only 9mW of power from a 2V power supply.

Acknowledgments

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