

A 10GHz CMOS Distributed Voltage Controlled Oscillator¹

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Abstract

A 10 GHz CMOS distributed voltage controlled oscillator (DVCO) is designed in a 0.35 μm BiCMOS process technology using only CMOS transistors. The oscillator achieves a tuning range of 12% (9.3 GHz to 10.5 GHz) and a phase noise of -114 dBc/Hz at 1 MHz offset from a carrier frequency of 10.2 GHz. The VCO uses two different simultaneous tuning techniques which allow for a coarse and fine tuning of frequency in a frequency synthesizer. The oscillator provides an output power of -7 dBm without any buffering, drawing 14mA of dc current from a 2.5V power supply.

Introduction

Recently, CMOS has emerged as a promising low-cost alternative to compound semiconductor or silicon bipolar technology for integration of microwave front-end circuits. Unlike traditional approaches, CMOS makes it possible to integrate the microwave front-end and digital back-end on the same chip and provides a system-on-a-chip solution at microwave frequencies.

Although it is possible to design LC oscillators on a silicon substrate up to 10 GHz, it becomes excessively hard to achieve a wide tuning range and good phase noise as the frequency of operation approaches f_{max} of transistors [1]. This is mainly due to the trade-off between the self-resonance frequency and the quality factor, Q , of the inductors and varactors. This trade-off becomes prohibitive as the operation frequency increases.

This limitation has made it more attractive to pursue alternative approaches, such as distributed oscillators. Distributed amplifiers have been studied for over 50 years [2][3][4]. Skvor, *et al* proposed to build a VCO by operating a distributed amplifier in the *reverse* gain mode, using the output from the idle drain load as the feedback output [5]. A 4 GHz distributed oscillator was demonstrated using four discrete pHEMTs and microstrip lines on a printed circuit board (PCB) [6]. In 1999, Kleveland, *et al* showed an integrated (with off-chip termination and bias) distributed oscillator operating at 17 GHz without any tuning capability using a 0.18 μm CMOS technology [7]. The forward gain mode instead of reverse gain mode was used to demonstrate that CMOS is usable for oscillator applications at microwave frequencies.

Despite these advances, tuning remains a problem since distributed VCOs (DVCOs) are used at frequencies close to the device f_T , where there is not enough gain to lose in tuning circuitry. Consequently, the addition of extra integrated varactors with low Q is not a favorable option due to their high loss which further deteriorates with frequency. Nor can the reverse mode tuning scheme of [5] be used due to the limited

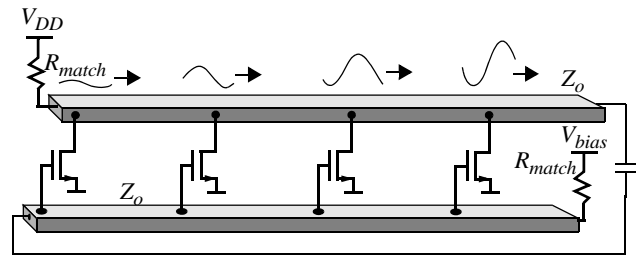


Figure 1. Basic distributed oscillator with isolated drain and gate bias.

transistor gain in CMOS technologies. Therefore, a new tuning scheme must be devised.

In this paper, we first discuss the basic principle and design issues of DVCOs. Then, the tuning techniques are discussed. Special attention will be paid to the layout and topology considerations. Finally, measurement results are shown.

Design of DVCO

A) Design of Basic Distributed Oscillators

An integrated distributed oscillator (Fig.1) operates in the forward-gain mode of a distributed amplifier. The forward (to the right in the figure) wave on the gate line is amplified by each transistor and appears on the drain line. The signal on the drain line travels forward in synchronization with the traveling wave on the gate line, and each transistor with transconductance, g_m , adds power constructively to the signal at each tapping point on the drain line. Thus the forward path can have an overall gain larger than unity while the gain of each transistor, approximately $g_m Z_0/2$, may be less than one. The output of the drain line is then fed back to the input of the gate line. (It is assumed that both lines have characteristic impedance Z_0). The forward traveling wave on the gate line and the backward (to the left in the figure) wave on the drain line are absorbed by the matched terminations, R_{match} .

To maximize the gain of each transistor, Z_0 must be maximized. The highest characteristic impedance can be achieved by using coplanar striplines with minimum conductor width of 3 μm for the signal line and a ground line of 8 μm . The spacing between the ground and signal lines is 10 μm , which results in a Z_0 of 70 ohms. Transistor loading reduces this impedance to 40 ohms. The 3.6 mm-long gate and drain lines are modeled with SPICE using a lumped lossy transmission line model with a total of 200 LRC sections.

B) Gate-Line Tuning

The frequency of a distributed oscillator is controlled by the time delay of its transmission lines. This delay can be changed in several different ways. One approach is to adjust the delay of the line by changing its capacitive loading. Since it is not possible to use explicit varactors due to their low Q , it is desirable to use the intrinsic capacitances of the transistors for tuning.

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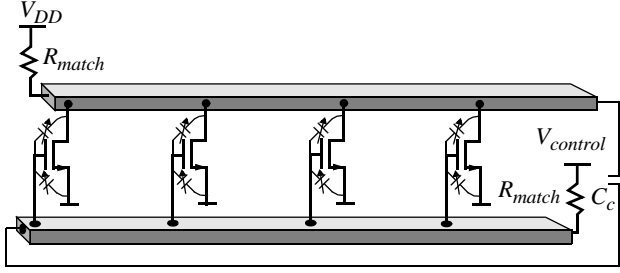


Figure 2. Gate-line bias tuning of a DVCO.

Tuning can be achieved by adjusting the dc bias of the gate-line as shown in Fig. 2. This is made possible by introduction of an ac coupling capacitor, C_c , between the drain and gate lines. With this modification, it is possible to change the nonlinear capacitances of transistors (such as C_{gs} and C_{gd}) as well as their transconductances, g_m , by changing gate bias. Simulation results indicate that C_{gd} has the largest effect on the tuning range.

C) Current-Steering Delay-Balanced Tuning

An alternative way of changing time delay is to vary the line length. Although the physical length cannot be changed, the effective electrical length can be varied as shown in Fig. 3. Each gain section consists of two gain transistors, M_1 and M_2 , connected between the gate and drain lines. Both transistors share the same tap point on the gate line. However, their drains are connected to the drain line at two different points. The transistors are biased using current sources I_1 and I_2 , and their sources are ac grounded using two bypass capacitors to maximize their gain. The effective electrical length of the drain line can be changed by varying the ratio of I_1 and I_2 . The difference between the minimum and maximum effective length of the drain line is controlled by the distance between the drain taps.

Tuning can be achieved by distributing the current between M_1 and M_2 with different ratios, and thus performing a vector sum of the output signals with different phases. Therefore, the effective total length of the transmission lines lies between the maximum and minimum, and the oscillation frequency can be tuned continuously. The tuning range is determined by the ratio of the distance between the drain tap points of M_1 and M_2 in each section to the total length of the transmission lines. We will refer to this technique as *current steering tuning* [8].

The problem with current-steering is delay mismatch. The drain line voltage can lead or lag the gate voltage in phase depending on the ratio of I_1 and I_2 . This phase mismatch between the gate and drain line affects the oscillator's phase condition and makes it harder for the oscillator to maintain 360 degrees of phase shift around the loop. In other words, it degrades the synchronization of the gate and drain lines. If not resolved, this phase mismatch degrades the phase noise at both ends of tuning range or can even stop the oscillation.

To remedy this problem, the delay mismatch between the gate and drain lines must be minimized. This can be done using the complementary configuration shown in Fig. 4. It is

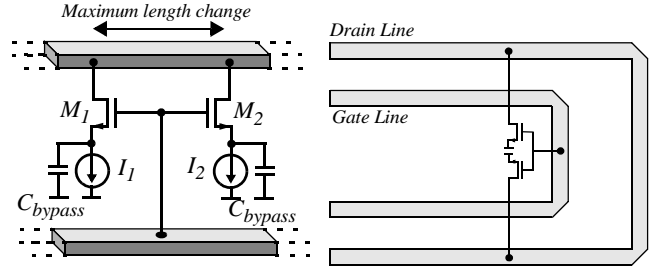


Figure 3. Varying effective length of transmission lines.

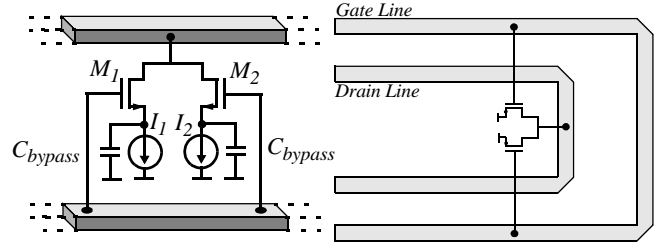
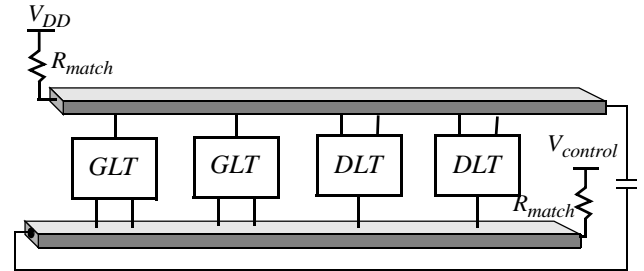
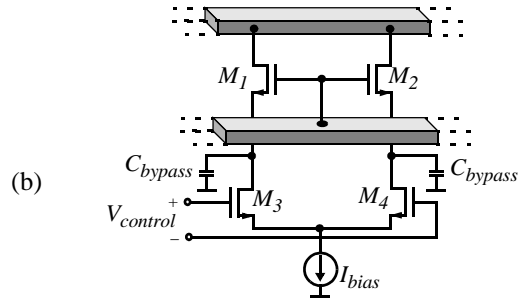


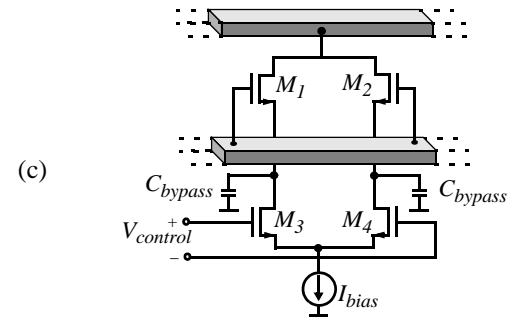
Figure 4. Complementary configuration for delay balancing.



(a)



(b)



(c)

Figure 5. Current-steering delay-balanced tuning: (a) block diagram of a DVCO; (b) section DLT; (c) section GLT.

different from the former one in that the gain transistors share the same drain tap point but are separated on the gate line by the same distance as the separation on the drain line of Fig. 3. A pair of these complementary sections (Fig. 3 and 4) can be used to cancel the delay mismatch. We will refer to this delay balancing technique as *current-steering delay-balanced tuning*.

Special attention should be paid to the layout of these structures as an extra piece of wire can simply act as another transmission line and introduce excess, unbalanced and unnecessary electrical length. Therefore, these delay-balanced structures should be placed at the “U-turns” of the transmission lines as shown in Figures 3 and 4.

The complete DVCO uses a pair of each structure as shown in Fig. 5a. It comprises of two gate-line-tuning (GLT) sections (Fig. 3 and 5b) and two drain-line-tuning (DLT) sections (Fig. 3 and 5c). In each section, I_1 and I_2 are replaced with the current source I_{bias} and two current steering transistors M_3 and M_4 . The differential control voltage steers the tail current between M_1 and M_2 . The channel lengths of transistors M_3 and M_4 should be chosen longer than the minimum channel lengths to allow for a larger and more uniform range of the differential control voltage, $V_{control}$. Longer channel length also reduces the channel noise of these devices which improves the phase noise of the oscillator.

D) Layout Issues

Since the circuit operates at microwave frequencies and any conductive line can act as a transmission line, special attention should be paid to the layout. First, the gate and drain lines should be parallel to maintain synchronization of signals and their spacing chosen to lower interference. However, due to the feedback path in the oscillator, a crossing where one transmission line goes underneath the other is inevitable. This crossing is implemented using both *metal1* and *metal2* lines to minimize the loss and compensate for the thickness difference between the top layer and the lower metal layers. Enough vias are introduced at the crossing point to minimize the resistance. Also, there are reverse-biased PN junctions (laminations) underneath the entire transmission line structure to terminate Eddy currents and lower the loss. In each section, the two gain transistors have identical distances from the tapping points on the transmission lines in order not to introduce unbalanced excess delay as shown in Fig. 3 and 4. The dc bias lines pass underneath and are perpendicular to the transmission lines to minimize the capacitive loading on the lines.

Experimental Results

The 10 GHz DVCO is fabricated in Conexant's 0.35 μm BiCMOS technology [9] using only CMOS transistors. The DVCO occupies an area of 1.4 mm x 1 mm, including the pad. It is noteworthy that CMOS transistors in a BiCMOS process are known to have inferior f_T s compared to transistors of comparable size in pure CMOS technologies.

In our test setup, the chip is glued to a PCB with conductive adhesive. The dc pads are wire-bonded to the PCB as shown

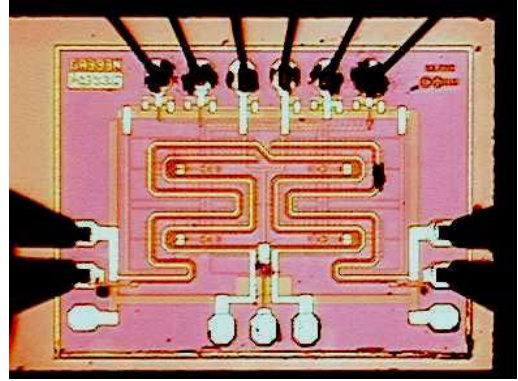


Figure 6. Chip photo.

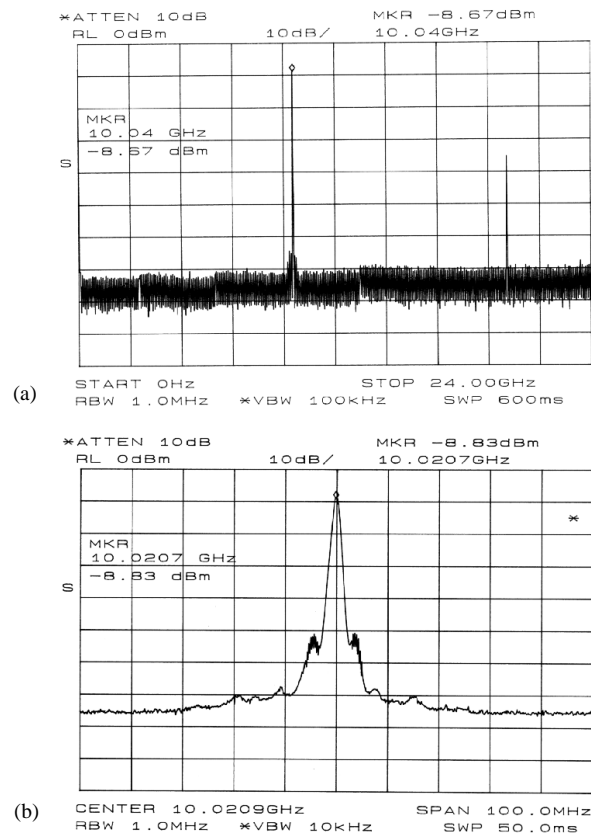


Figure 7. Power spectrum: (a) harmonics; (b) detail.

in the die photo of Fig.6. A microwave probe station in conjunction with microwave coplanar probes are used to probe the RF pads on the other three sides. The probes are connected to the measurement equipment and biasing circuitry through coaxial cables. An HP 8563E spectrum analyzer is used to measure the oscillation frequency and the output power. The insertion loss from the probes to the spectrum analyzer is 4.3dB. Therefore, any measured power on the analyzer should be adjusted for this extra loss.

The measured power spectrum is shown in Fig.7, which should be adjusted for the 4.3dB loss in the setup. The output frequency of the oscillator is 10.0 GHz and the output power

is -4.5 dBm. Deterministic modulation sidebands are observed in the output spectrum. Further tests and experiments revealed that they are induced by the radio broadcast signals absorbed by the probe setup, which modulates the DVCO, and hence are not inherent to the DVCO itself.

Fig. 8 shows a tuning range of 12% (9.3–10.5 GHz) with a total drain current of 14 mA for the gate-line tuning. The measured tuning range of the current-steering delay-balanced tuning technique is 2.5% (10.19–10.44 GHz) as shown in Fig. 9. This dual tuning capability allows a simultaneous coarse and fine tuning in a frequency synthesizer which can improve the capture range.

The measured output power from the gate and drain termination points vs. total drain current are compared in Fig.10. These measurements are good indicators of the oscillator's internal voltage levels.

Conclusion

A 10 GHz CMOS DVCO tunable in the range of 9.3–10.5 GHz is demonstrated. It utilizes two tuning techniques, namely, gate-line tuning and current-steering delay-balance tuning. The DVCO is implemented in a 0.35 μm BiCMOS technology using only CMOS transistors, showing a phase noise of -114 dBc/Hz at a 1MHz offset from a 10.2 GHz carrier, drawing 14 mA of current from a 2.5V supply.

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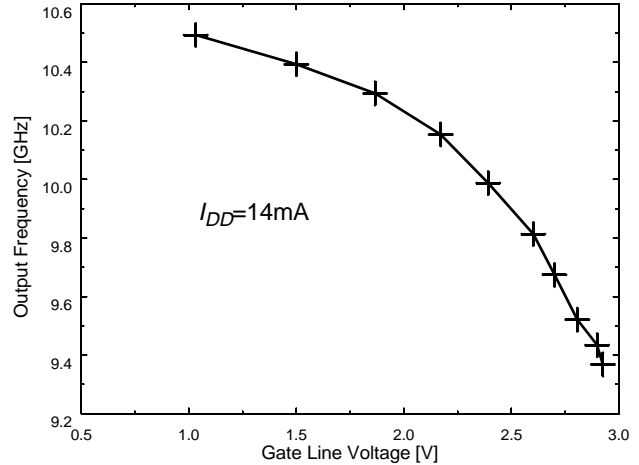


Figure 8. Gate-line bias tuning range.

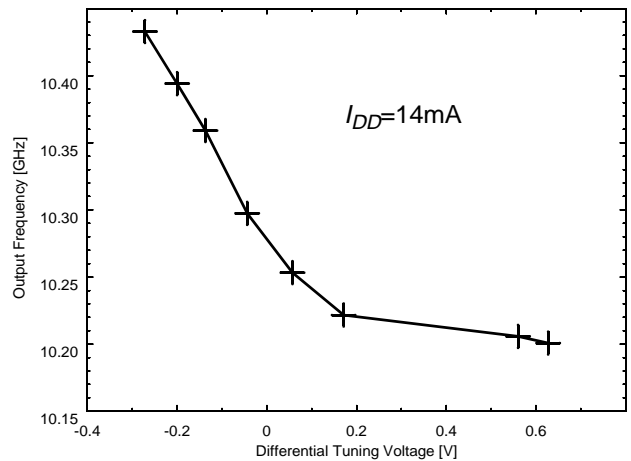


Figure 9. Current-steering delay-balanced tuning range.

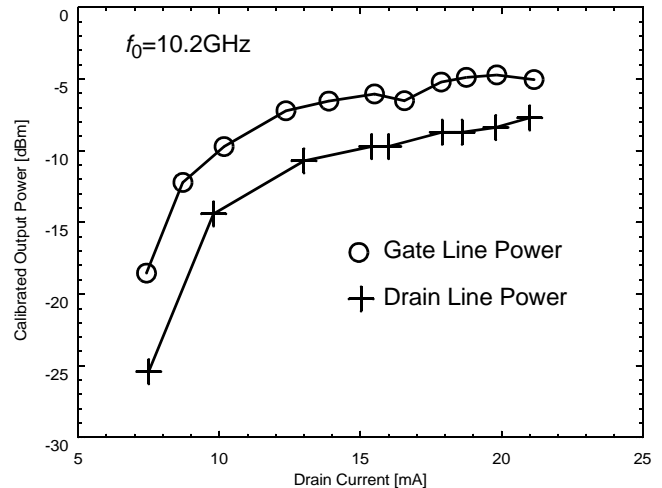


Figure 10. Power consumption vs. output power.

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