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A NOVEL TUNING TECHNIQUE FOR DISTRIBUTED VOLTAGE CONTROLLED OSCILLATORS

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ABSTRACT

A novel current-steering delay-balanced tuning technique for distributed voltage controlled oscillators (DVCO) is demonstrated. This tuning technique is used to design a DVCO operating at 10 GHz in a 0.35 μm CMOS technology. The DVCO is continuously tunable between 9.9 and 10.3 GHz. Special attention is paid to the layout issues for the high frequency design.

1. INTRODUCTION

Voltage controlled oscillators (VCO) are essential building blocks in communication systems. Advances in wireless communications and broadband networks create demands for VCOs at microwave frequencies. On the high-speed digital communication front, multi-gigahertz clock-and-data recovery loops require low-jitter high-frequency VCOs to achieve a low bit-error rate. Even next generation microprocessors need multi-gigahertz on-chip frequency synthesizers.

Traditionally, integrated VCOs at microwave frequencies were implemented using compound semiconductor (GaAs or InP) or silicon bipolar technology. However, CMOS is emerging as a promising low-cost alternative capable of integrating the microwave front-end with the digital-signal-processing back-end. It therefore provides a possible system-on-a-chip solution at microwave frequencies.

It is difficult to design an LC-tank VCO on silicon substrate using CMOS process at frequencies close to the cut-off frequency (f_T) of the transistors due to the small gain of devices. The low Q of integrated inductors and varactors exacerbate the situation for operation at frequencies above C-band. Therefore, the idea of a distributed oscillator is gaining momentum in CMOS RFICs.

Distributed oscillators originate from distributed amplifiers, which have been studied for over 50 years [1-4]. In 1992, Skvor *et al.* proposed to make a VCO by operating a distributed amplifier in the reverse gain mode, using the output from the idle drain load as the feedback output [5]. A 4 GHz distributed oscillator was demonstrated using four discrete pHEMTs and microstrip lines on a printed circuit board [6]. In 1999, Kleveland *et al.* showed an integrated (with off-chip termination and bias) distributed oscillator at 17 GHz without any tuning capability in a 0.18 μm technology [7]. The forward gain mode instead of reverse gain mode was used. Their results demonstrated that CMOS is usable for oscillator applications at microwave frequencies.

Despite these advances, tuning remains a problem in integrated distributed oscillators. Since distributed oscillators usually operate at frequencies close to the device f_T, there is not enough gain to lose in tuning. Consequently, the low Q integrated varactors can hardly be used due to their high loss. Nor can the tuning scheme in [6] be applied since it cannot provide enough gain in CMOS technology. Therefore, a new tuning scheme must be developed.

In this paper, we first discuss the basic principle and design issues of DVCOs. Then a novel tuning scheme will be presented and SPICE simulation results will be shown. Finally, we will deal with layout and topology considerations.

2. DESIGN

2.1 Design of Basic Distributed Oscillators

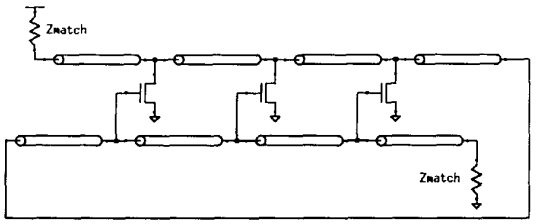

Figure 1. Distributed oscillator.

An integrated distributed oscillator operates in the forward-gain mode of a distributed amplifier (Fig. 1). The forward (to the right in the figure) wave on the gate line is amplified by each transistor. Amplified waves travel forward on the drain line in synchronization with the wave on the gate line and add constructively at each tap point on the drain line. The sum from the output of the drain line is then fed back to the input of the gate line. The forward wave on the gate line and the backward (to the left in the figure) wave on the drain line are absorbed by the matched terminations.

Coplanar striplines (Fig. 2) are used in order to maximize the characteristic impedance (Z_0), which is proportional to the open-loop gain and thus the oscillation amplitude.

The design specifications are oscillation frequency and amplitude. The design variables are geometry (width, spacing,

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and length) of transmission lines, number of sections, termination, transistor size, and bias current.

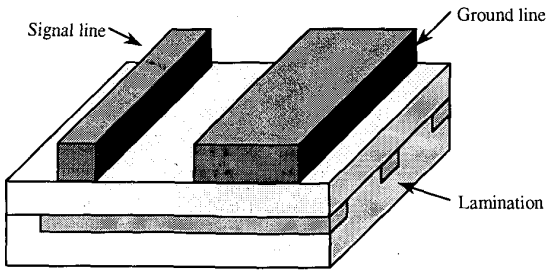

Figure 2. Coplanar stripline.

2.2 Tuning

Intuitively, a distributed oscillator can be tuned by varying the time delay of the transmission line sections. A conceptually easy way is to load the transmission lines with varactors so as to change their effective delay (Fig. 3). It can also help to balance the phase constants of the gate and drain lines. However, the quality factor, Q, of available varactors in CMOS technology is rather low at frequencies of interests, so that the oscillation can hardly start.

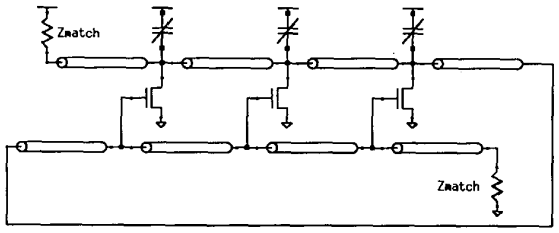

Figure 3. Tuning a distributed oscillator by varactors.

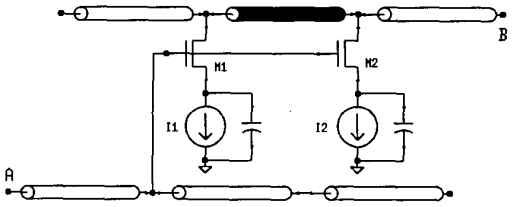

Figure 4. Varying effective length of transmission lines.

An alternative approach is to vary the length of the transmission lines to tune the distributed oscillator. Since the physical length cannot be changed, we choose to change the effective length by changing the transconductance of active transistors. As can be seen in Figure 4, each gain section comprises of two gain transistors (M_1, M_2) which are coupled between the gate and drain lines. These two transistors are separated by an additional transmission line segment (highlighted) on the drain line, with both gates connected to the same point on the gate line. The sources of M_1 and M_2 are ac grounded by two bypass capacitors, while dc biased by the current sources. By varying the currents, the total effective length of the transmission line is varied between its minimum and maximum.

For instance, when I_1 is maximum and I_2 is zero, only M_1 contributes to amplification. Therefore, the effective length of the transmission lines reaches its maximum value, which is longer than the minimum by the length of the highlighted segment between M_1 and M_2. A voltage change at node **A** will take the longest time to reach node **B**. This corresponds to the lowest oscillation frequency. On the other hand, when I_1 is zero and I_2 is maximum, the effective length of the transmission lines is at its minimum value, and the transmission from **A** to **B** is the fastest. Then the highest oscillation frequency is obtained.

Tuning can be achieved by distributing the current with different ratio between the two sets of transistors, and thus adding the output signals from the gain transistors in different phases. Therefore, the effective total length of the transmission lines lies between the maximum and minimum, and the oscillation frequency can be tuned continuously. The tuning range is determined by the ratio of the length of the transmission line segment between M_1 and M_2 in each section to the total length of the transmission lines, and therefore can be adjusted based on the application. We will refer to this technique as **Current Steering Tuning**.

The problem with current steering is delay mismatch. The traveling wave on the gate and drain lines will experience a phase mismatch, which depends on the relative current in M_1 and M_2. Also, the loading effect due to the transistor capacitance is more severe on the gate line than the drain line, since the gate capacitance of both gain transistors are connected to the same tapping point on the gate line while the drain capacitances are separated. The introduced phase mismatch degrades the oscillation amplitude or can even stop the oscillation. In order to balance the delay, a complementary configuration is devised (Fig. 5). It is different from the former one in that the gain transistors are separated by an additional transmission line segment on the gate line while driving the same node on the drain line. A pair of these complementary sections can be used to cancel the delay mismatch to the first order. We will refer to this delay balancing technique as **Current-Steering Delay-Balanced Tuning**.

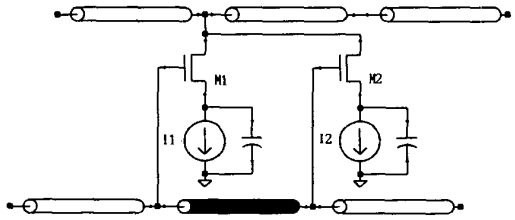

Figure 5. Complementary configuration for delay balancing.

The complete structure of a four-section DVCO with this technique is shown in Fig. 6a. It comprises of two gate-line-tuning (GLT) sections (Fig. 6b) and two drain-line-tuning (DLT) sections (Fig. 6c) to compensate the delay mismatch. For the convenience of layout, the four sections are in the sequence of GLT-GLT-DLT-DLT. In each section, I_1 and I_2 are replaced with the current source M_5 and two current steering transistors (M_3, M_4). The differential control voltage steers the tail current between M_1 and M_2. Bypass capacitors Cs_1 and Cs_2 guarantee that sources of M_1 and M_2 are ac grounded for maximum gain at the frequency of oscillation. They also suppress potential low frequency common-mode oscillations by lowering the gain at low frequencies.

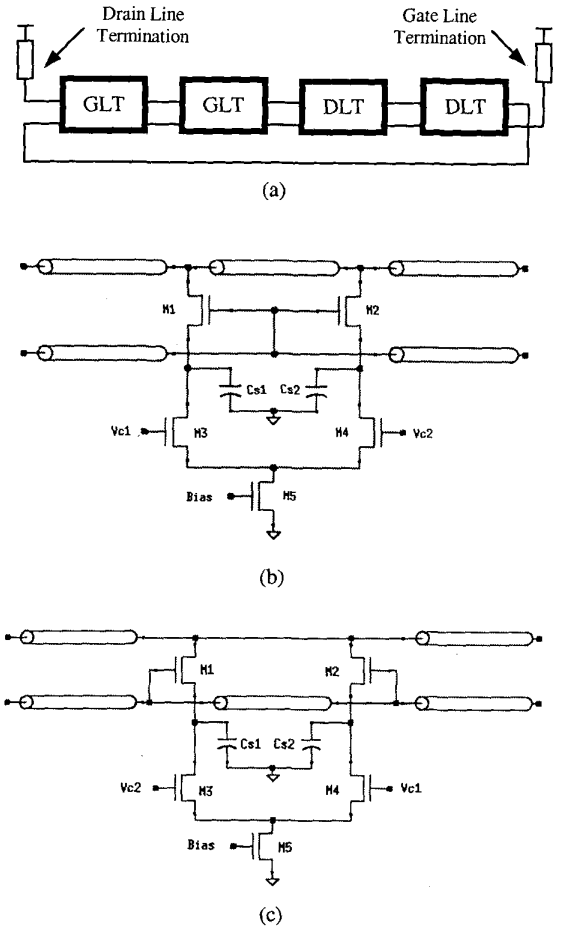

Figure 6. Current-steering delay-balanced tuning: (a) block diagram of a DVCO; (b) GLT; (c) DLT.

2.3 Simulation Results

The DVCOs are designed in Conexant's 0.35 μm BiCMOS technology using only CMOS transistors [8]. The top metal layer is 3 μm thick, and 4 μm above the substrate.

Circuit parameters from full-wave electromagnetic simulations [9] and lossy transmission line models in HSPICE are used to simulate coplanar striplines with a width of 3 μm (ground line 8 μm) and spacing of 10 μm (Fig. 2).

Figure 7a shows the startup characteristics of the designed four-stage CMOS DVCO. The simulated output spectrum in steady state can be seen in Figure 7b showing the power in the harmonics. The DVCO has a center frequency of 10 GHz with tuning span between 9.9 and 10.3 GHz (Fig. 7c).

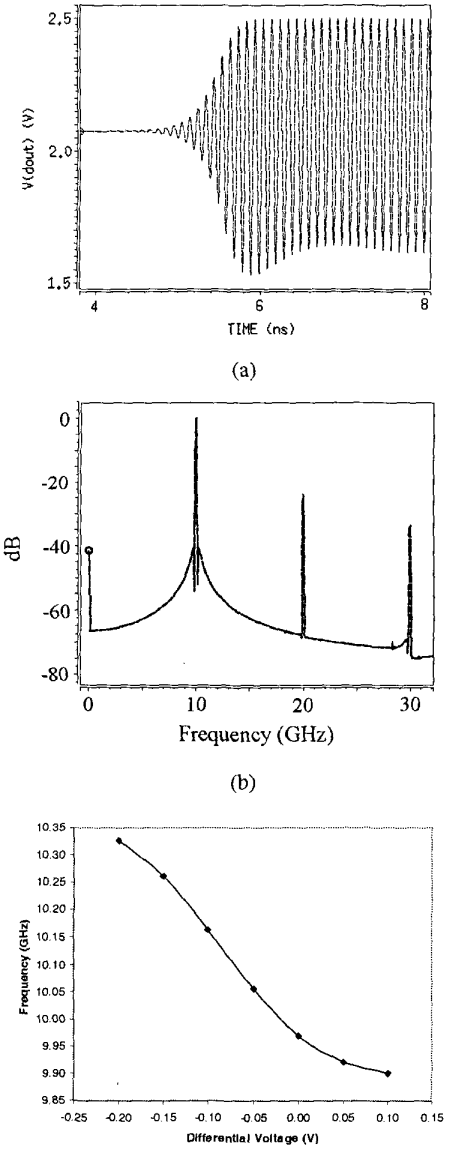

Figure 7. Simulation results: (a) output waveform; (b) FFT spectrum; (b) tuning range.

2.4 Layout

Due to very high frequency operation and sensitivity to effective length of the transmission lines, special attention should be paid to the layout. A few points are highlighted here:

- The gate line and drain line are in parallel to maintain synchronization of signals on the two lines. There should also be enough spacing between different coplanar striplines to prevent interference. However, since there is a feedback loop in the whole transmission line structure, a crossing where one transmission line goes underneath the other is inevitable.
- There are reverse-biased PN junctions (laminations) underneath the transmission lines to terminate Eddy currents to lower the loss of the transmission lines.
- In each section, the two gain transistors have identical distance from the tapping points on the transmission lines in order not to introduce unbalanced excess delay.
- The dc bias lines are perpendicular to the transmission lines to minimize the capacitive loading on the transmission lines.
- The output and terminations are easily accessible from the pad frame. To be able to use microwave coplanar probes, there should be only one RF pad (totally three) on each side of the chip, and thus all dc pads should be on the same side, convenient for wire-bonding.

The layout is made as symmetrical as possible. Figure 8 and Figure 9 show the floorplan and layout of the complete DVCO, respectively. The DVCO occupies an area of 1.4 mm x 1 mm (including the pad frame).

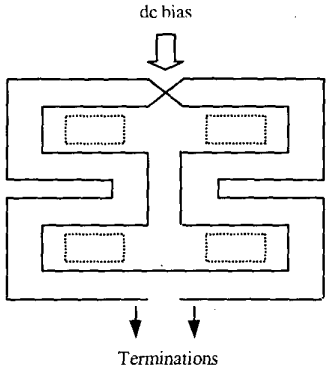

Figure 8. Floorplan of the DVCO.

3. CONCLUSION

A novel current-steering delay-balanced tuning technique for integrated DVCOs is proposed. A 10 GHz DVCO tunable in the range of 9.9 – 10.3 GHz using this tuning technique is demonstrated. The circuit is simulated in HSPICE and implemented in a 0.35 μm CMOS technology. Special attention is paid to the layout issues for high frequency operation.

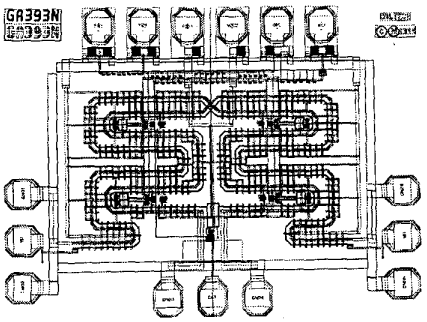

Figure 9. Layout of the DVCO.

4. ACKNOWLEDGEMENT

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