Analysis and Design of Silicon Bipolar Distributed Oscillators

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Abstract

A systematic approach to design of silicon bipolar distributed oscillators and VCOs is presented. The operation of distributed oscillators is analyzed and the general condition for oscillation is derived, resulting in analytical expressions for the frequency and amplitude of distributed oscillators. Special attention is paid to transmission line modeling that largely determines the performance of distributed oscillators. A distributed VCO operating at 12GHz dissipating 13mW of power is demonstrated. The VCO has a tuning range of 26% with a phase noise of -104dBc/Hz at 1MHz offset from the carrier. A second design shows a 17GHz bipolar distributed oscillator, which dissipates 9mW of power.

Introduction

Originated from distributed amplifiers[1][2], distributed oscillators show great prospects in the applications of silicon RFIC over the frequency range of 10-30 GHz due to their capability to operate at frequencies close to the intrinsic cut-off frequency of devices. A 4 GHz distributed oscillator using discrete pHEMTs was demonstrated by Skvor, *et al* [3][4]. Kleveland, *et al* showed a 17 GHz integrated distributed oscillator using a 0.18 μm CMOS technology[5]. Recently developed tuning techniques for distributed oscillators [6] make it possible to use them as voltage controlled oscillators (VCOs) in frequency synthesizers and clock recovery circuits. Despite these developments, a systematic and analytical approach to the design of distributed voltage controlled oscillators (DVCO) is still lacking.

In the next section, the basic operation of the distributed oscillator will be briefly introduced, followed by a detailed analysis of the oscillation condition, leading to general expressions for the amplitude and frequency of the oscillator. Next, the design and modeling of the coplanar transmission lines for a 12 GHz distributed oscillator will be presented, allowing us to calculate the frequency and amplitude analytically. Finally, experimental results for the 12 GHz distributed VCO and a 17 GHz distributed oscillator will be given.

Design of DVCO

A) Analysis of Distributed Oscillators

An integrated distributed oscillator (Fig.1) operates in the forward-gain mode of a distributed amplifier. The forward (to the right in the figure) wave on the base line is amplified by each transistor and appears on the collector line. The travelling wave on the collector line travels to the right in synchronization with the traveling wave on the base line. Each transistor adds power in phase to the signal at each tapping point on the collector line. Thus, the forward path can have an overall gain larger than unity while the gain of each transistor may be less than one. To sustain oscillations, the output of the collector line (node **2**) is fed back to the input of the base line (node **1**). The forward traveling wave on the base line and the backward (traveling to the left) wave on the collector line are absorbed by terminations matched to loaded characteristic impedance of the base line, Z_b', and collector line, Z_c', respectively.

To obtain a general condition for oscillation, the feedback loop is broken at nodes **1** and **2** (Fig. 2). In steady state, the gain from **1** to **2** should be 1. For a large coupling capacitor, the nodes **1** and **2** should have identical ac voltages. In the most general case, the load impedance of the base and collector lines are not equal, so it is important to have the correct source and load impedance at nodes **1** and **2** to consider loading effects, as shown in Fig. 2.

The voltage at the *i*th tap of the base line is related to the base line's segment length, l_b, and complex transmission line propagation constant, γ_b, through

$$v_{bi} = v_1 e^{-(i-1)\gamma_b l_b} \quad \textbf{(1)}$$

where v_1 is the voltage at node **1**. This is assuming that the base line is terminated to the loaded characteristic impedance of the base line, given by[1]

$$Z_b' \approx \sqrt{\frac{j\omega L_b + R_b}{j\omega\left(C_b + \frac{c_\pi}{l_b}\right) + G_b}}, \quad \textbf{(2)}$$

on the right. L_b, R_b, C_b, G_b are the series inductance and resistance, and parallel capacitance and conductance of the base transmission line per unit length, respectively. c_π is the small signal base-emitter capacitance of the bipolar transistors. Assuming that the collector line is terminated to its loaded characteristic impedance,

$$Z_c' \approx \sqrt{\frac{j\omega L_c + R_c}{j\omega\left(C_c + \frac{c_{out}}{l_c}\right) + G_c}}, \quad \textbf{(3)}$$

on the left, the incident wave going out of the collector of each transistor sees an impedance of $Z_c'/2$. L_c, R_c, C_c, G_c are the series inductance and resistance, and parallel capacitance and conductance of the base transmission line per unit length, respectively, and c_{out} is the total output capacitance of the bipolar transistors. Note that the impedance seen by the incident wave is the characteristic impedance of the transmission line. The generated incident wave at the *i*th collector tap traveling to the right is therefore given by:

$$E_{ci} = -G_m \frac{Z_c'}{2} v_{bi} = -G_m \frac{Z_c'}{2} v_1 e^{-(i-1)\gamma_b l_b} \quad \textbf{(4)}$$

where G_m is the large signal tranconductance of each transistor as defined in [7]. These generated waves travel through

1. This is assuming that the number of transistors on the line is large, so their input and output capacitances may be considered distributed.

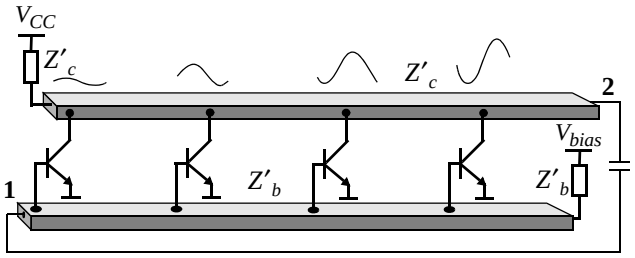

Figure 1. Basic distributed oscillator structure

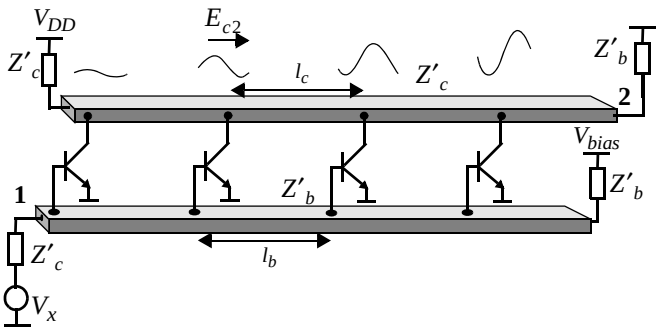

Figure 2. Open-loop equivalent model.

different lengths of transmission line to get to the output node. Therefore, the total incident wave at node **2** is given by superposition, *i.e.*,

$$E_{i2} = E_{c1}e^{-n\gamma_c l_c} + E_{c2}e^{-(n-1)\gamma_c l_c} + \ldots + E_{cn}e^{-\gamma_c l_c} = \sum_{i=1}^{n} E_{ci}e^{-(n-i+1)\gamma_c l_c} \quad \textbf{(5)}$$

Part of this incident wave will be reflected due to the impedance mismatch at node **2** as the collector line is connected to the base line which generally has a different loaded characteristic impedance. The reflected wave, E_{r2}, is related to the incident wave, E_{i2}, through the reflection coefficient, *i.e.*,

$$\Gamma_2 \equiv \frac{E_{r2}}{E_{i2}} = \frac{Z'_b - Z'_c}{Z'_c + Z'_b} \quad \textbf{(6)}$$

The voltage at node **2** will thus be given by

$$v_2 = E_{i2} + E_{r2} = E_{i2} \cdot \frac{2Z'_b}{Z'_b + Z'_c} \quad \textbf{(7)}$$

Using (4), (5) and (7), v_2 can be expressed in terms of v_1. Noting that for steady-state oscillations, $v_1 = v_2$ as they represent the same ac node in closed loop system, the following general oscillation condition is obtained:[2]

$$G_m \cdot (Z_b \parallel Z_c) \cdot \frac{e^{-(n+1)\gamma_c l_c} - e^{-(n+1)\gamma_b l_b}}{e^{-\gamma_c l_c} - e^{-\gamma_b l_b}} = -1 \quad \textbf{(8)}$$

This condition determines both the amplitude and the frequency of the oscillation.

To gain more insight into (8), let us consider the special case where the product of the complex propagation constants and section lengths are equal for both the collector and base lines, *i.e.*, $\gamma_c l_c = \gamma_b l_b$. This can be achieved by having different lengths and widths for the collector and base lines in the design. The oscillation condition of (8) reduces to

$$G_m \cdot (Z'_b \parallel Z'_c) \cdot n \cdot e^{-n\alpha l} \cdot e^{-jn\beta l} = -1 \quad \textbf{(9)}$$

where $\gamma = \alpha + j\beta$. The imaginary part of (9) should be -1. Assuming purely real characteristic impedance for the base and collector lines and l=l_b=l_c, we should have $nl\beta = \pi$. Noting that $\beta = 2\pi f / v_{group}$, where v_{group} is the wave group velocity in the line, the oscillation frequency is:

2. Using the identity $a^{n+1} - b^{n+1} = (a-b)(a^n + a^{n-1}b + \ldots + b^n)$

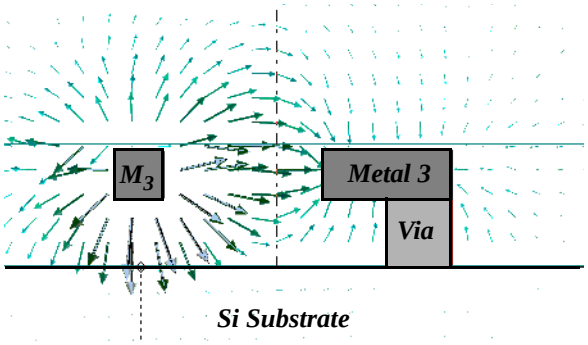

Figure 3. Electric field distribution from HFSS simulation

$$f_o = \frac{v_{group}}{2nl} \quad \textbf{(10)}$$

This expression makes intuitive sense as the denominator is twice the distance the wave has to travel through the oscillator to come back to the same place. The reason for the factor of two is the extra 180 degrees phase shift contributed by the transistor which halves the required distance.

The real part of (9) determines the amplitude by fixing G_m. Noting that for amplitudes, V_{amp}, large compared to kT/q, $G_m \approx 2I_C / V_{amp}$ [8], the oscillation amplitude is given by

$$V_{amp} = \frac{2I_C}{G_m} = 2nI_C(Z_b \parallel Z_c)e^{-\alpha nl} \quad \textbf{(11)}$$

where $e^{-\alpha nl}$ represents the loss in the transmission line. It is noteworthy that (11) reduces to the expression for the amplitude of a lumped oscillator for n=1 [8].

B) Transmission Line Modeling

Silicon is a very lossy substrate compared to III-V semiconductors and therefore special attention should be paid to the modeling of the transmission lines. Modeling can be done at three different levels: full-blown 3D electromagnetic (E&M) simulation, quasi-TEM transmission line modeling, and lumped RLC ladders. 3D E&M simulation is the most accurate and the most time-consuming. Quasi-TEM transmission line modeling may be preferred due to existence of analytical expressions. Finally lumped RLC ladder modeling can be easily integrated into circuit simulation, but are the least accurate.

In this design, the coplanar stripline has a conductor thickness of 3μm, a width of 3μm and a 4.2μm vertical spacing to

the substrate. The ground line is 8 μm wide and is placed 10μm away from the signal line. Fig. 3 shows the cross-section of this structure and the electric field distribution simulated by HFSS [9].

HFSS simulations result in a unloaded characteristic impedance of $Z = 73.7\Omega - j0.84\Omega$ and a propagation constant of $\gamma_{unload} = 51.3 + j514[neper/m]$, which translate to a series inductance of $L = 503nH/m$, a parallel capacitance of $C = 92.4pF/m$, a series resistance of $R = 4.22k\Omega/m$ and a parallel conductance $G = 0.616S/m$.Using these parameters in conjunction with transistor parameters (*e.g.* c_π, r_π, etc.), the following loaded parameters were obtained for the base and collector lines:

$$Z'_c = 66.5\Omega - j0.57\Omega$$
$$Z'_b = 28.4\Omega - j1.1\Omega$$

Since the loaded characteristic impedances of the base and collector lines are very different, the most general condition given by (8) should be used to calculate the frequency and amplitude of the oscillation. An internal voltage amplitude of 0.22V and a frequency of 12.7GHz are predicted.

C) Layout Issues

Layout is also a critical issue in the design of DVCOs. A few important considerations are highlighted here: due to the feedback path in the oscillator, a crossing where one transmission line goes underneath the other is inevitable. This crossing is implemented using both *metal*1 and *metal*2 lines to minimize the loss and compensate for the thickness difference between the top layer and the lower metal layers. Enough vias are introduced at the crossing point to minimize the resistance. In each section, the two gain transistors have identical distances from the tapping points on the transmission lines in order not to introduce unbalanced excess delay. The dc bias lines pass underneath and are perpendicular to the transmission lines to minimize the capacitive loading on the lines.

Measurement Results and Conclusion

The bipolar DVCOs are fabricated in a 0.35μm BiCMOS technology. The 12 GHz VCO occupies an area of 1.2 mm x 1 mm, and the 17 GHz distributed oscillator uses 1mm x 0.8 mm of die area (Fig. 4).

The parasitic losses of a package is avoided by wire-bonding the dc pads to the PCB. A microwave probe station in conjunction with microwave coplanar probes are used to probe the RF pads on the other three sides. An HP 8563E spectrum analyzer is used to measure the oscillation frequency and output power. The insertion loss of the setup from the probe to the spectrum analyzer is 6.3 dB and 12.4 dB at 12 GHz and 17 GHz, respectively. Therefore, all the measured power shown should be adjusted accordingly.

The measured power spectrum and phase noise spectrum of the 12 GHz VCO are shown in Fig. 5 and Fig. 6. A phase noise of -104 dBc/Hz at 1 MHz offset from a 11.7 GHz carrier is achieved on only 6 mA bias current from a 2.2 V dc supply. This power dissipation is comparable to low power

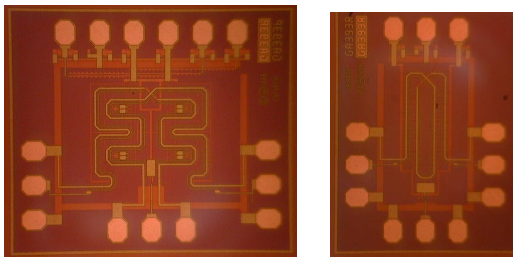

Figure 4. Chip photo: 12 GHz (left), 17 GHz (right)

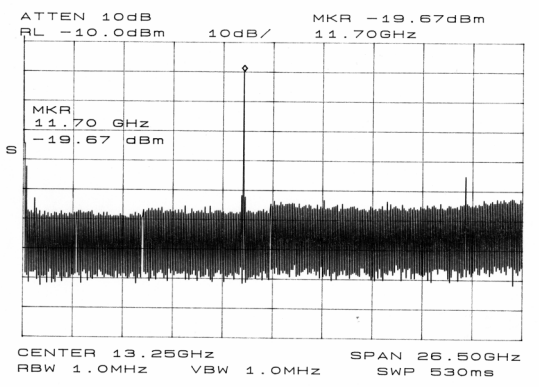

Fig. 5 Power Spectrum of 12 GHz DVCO

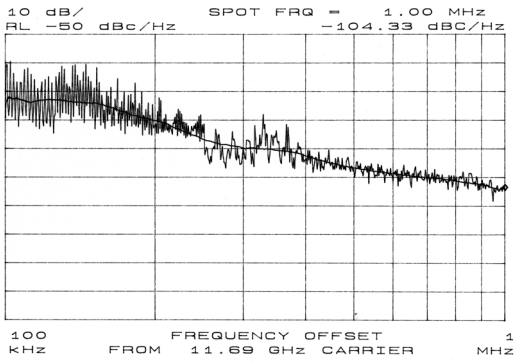

Figure 6. Phase Noise of 12 GHz DVCO

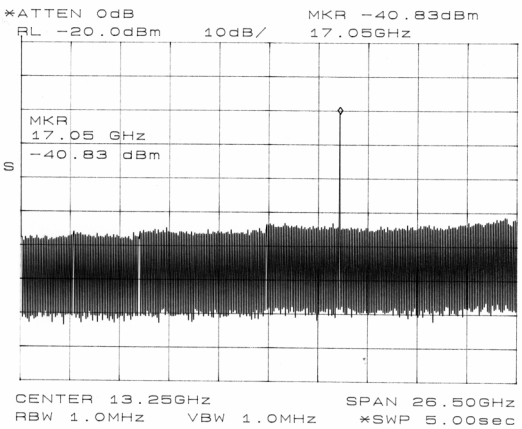

Figure 7. Power Spectrum of 17 GHz DVCO

lumped VCOs operating at lower frequencies. A better phase noise can be achieved simply by increasing the bias current.

Collector line tuning achieves a remarkable tuning range of 26% (9.6 - 12.45 GHz) as shown in Fig. 9. Also a differential current-steering delay-balanced tuning technique, which has been used in CMOS implementation [6], achieves 7.4% (11.68 - 12.57 GHz) tuning range (Fig. 10). This dual differential and single-ended tuning capability allows a simultaneous coarse and fine tuning in a frequency synthesizer which is very useful for improving the capture range in a phase-locked loop.

The power spectrum and phase noise spectrum of the 17 GHz differential VCO are shown in Fig. 7 and Fig. 8. A phase noise of -84 dBc/Hz at 1 MHz offset from a 17 GHz carrier with a total collector current of 9 mA from a 1 V supply is observed. Although not intended to be tunable, it can be tuned over a span of 160 MHz (17.03 - 17.19 GHz) (Fig. 11) by varying the bias current.

Conclusion

In this paper, a systematic approach to analysis of distributed oscillators has been presented. The general oscillation condition has been derived, leading to analytical expressions for the amplitude and frequency. The design of a 12 GHz silicon bipolar distributed VCO has been discussed. It achieves 26% tuning range with a phase noise of -104 dBc/Hz at 1 MHz offset from the carrier. A 17 GHz silicon bipolar distributed oscillator is also demonstrated.

Acknowledgment

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6. References

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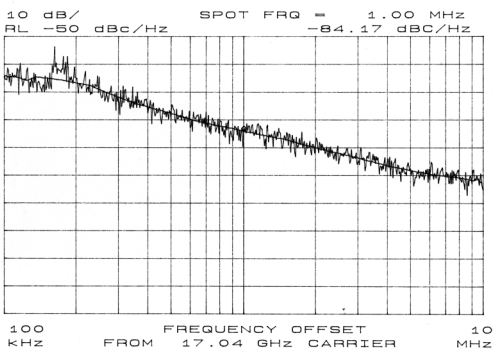

Figure 8. Phase Noise of 17 GHz DVCO

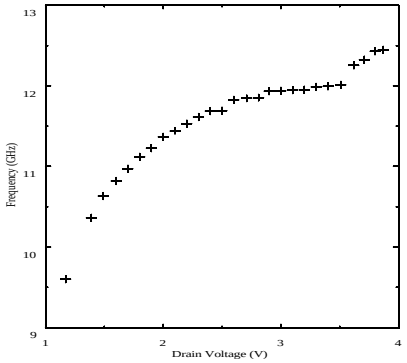

Figure 9. Drain bias tuning in 12 GHz DVCO

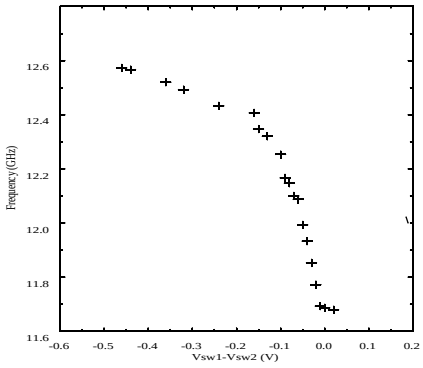

Figure 10. Current-steering delay-balanced tuning in 12 GHz DVCO

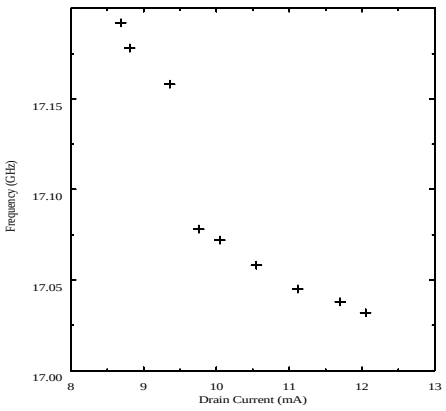

Figure 11 Bias current tuning in 17 GHz DVCO