Concurrent Dual-Band CMOS Low Noise Amplifiers and Receiver Architectures

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Abstract

A new *concurrent* dual-band receiver architecture is introduced that is capable of *simultaneous* operation at two different frequency bands. The concurrent operation results in higher bandwidth, lower total power dissipation and less sensitivity to channel variations. The architecture uses a novel *concurrent* dual-band low noise amplifier (LNA), combined with an elaborate frequency conversion scheme to reject the image bands. A general methodology for the design of concurrent LNAs is provided that makes it possible to achieve simultaneous narrowband gain and matching at multiple frequencies. The methodology is demonstrated by implementing an integrated dual-band concurrent LNA using $0.35\mu m$ CMOS transistors. The LNA provides narrow-band gain and matching at 2.45GHz and 5.25GHz bands, simultaneously. It drains 4mA of current and achieves voltage gains of 14dB and 15.5dB, input return losses of 25dB and 15dB, and noise figures of 2.3dB and 4.5dB at these two bands, respectively.

Introduction

Standard receiver architectures, such as superheterodyne and direct conversion, accomplish high selectivity and sensitivity by narrow-band operation at a single RF frequency. These modes of operation limit the system's available bandwidth and robustness to channel variations and thus its functionality. On the other hand, wideband modes of operation are more sensitive to out-of-band signals due to transistor non-linearity, which can introduce severe bottlenecks in system performance.

The diverse range of modern wireless applications necessitates communication systems with more bandwidth and flexibility. More recently, dual-band transceivers have been introduced to increase the functionality of such communication systems by switching between two different bands and receive *one band at a time*[5][8]. While switching between bands improves receiver's versatility (*e.g.*, in dual-band cellular phones), it is not sufficient in the case of a multi-functionality transceiver (*e.g.*, a cellular phone with a GPS receiver and a bluetooth interface). Using conventional receiver architectures, simultaneous operation at different frequencies can only be achieved by building multiple independent signal paths with an inevitable increase in the cost, footprint and power dissipation.

In this work, a new *concurrent* dual-band receiver architecture is introduced that is capable of *simultaneous* operation at two different frequencies without dissipating twice as much power or a significant increase in cost and footprint. This concurrent operation can be used to extend the available bandwidth, provide new functionality and/or add diversity to battle channel fading. The concurrent operation is realized through an elaborate frequency conversion scheme, in conjunction with a novel concurrent dual-band low noise amplifier (LNA). These new concurrent multi-band LNAs provide simultaneous narrow-band gain and matching at multiple frequency bands.

The next section briefly describes the proposed receiver architecture and demonstrates the central role of the concurrent LNAs in the receiver. A general methodology for the design of concurrent multi-band LNAs will follow, leading to a particular CMOS implementation of a concurrent dual-band LNA. Finally, the measurement results are presented and discussed.

Receiver Architecture

In this section, we will demonstrate the design process leading to the fully-integrated concurrent dual-band receiver architecture. The objective is to devise a receiver that can simultaneously receive the signal at two different frequency bands with maximum reuse of power and building blocks.

The first gain stage in a concurrent dual-band receiver is its LNA. Traditional single-band LNAs use a single or cascode transistor stage to provide wideband transconductance and combine it with proper passive resonant circuitry at the input and output to shape the frequency response and achieve gain and matching at the single band of interest [1]. A very important observation here is that the transconductance of the active device is still wideband and can be used to provide gain and matching at other frequencies of interest without any penalty in power dissipation. This observation leads to a compact and efficient front-end for a concurrent dual-band receiver which consists of a dual-band antenna [2][3], followed by a monolithic dual-band filter [4] and a concurrent dual-band LNA that provides simultaneous gain and matching at two bands, as shown on the left-hand side of Fig. 1. A detailed approach to the design of such multi-band LNAs will be described in the subsequent sections.

The frequency of the first local oscillator (LO) that appears after the LNA and performs the first down conversion determines the image frequency(ies) and plays an important role in the performance of the system. For a *non-concurrent* receiver, it has been proposed to choose the first LO frequency halfway between the two frequency bands and select the band of interest by choosing the appropriate sideband produced by an image-separation mixer [5]. Although this method is sufficient for the non-concurrent approaches, it will suffer from some serious shortcomings if used *for a concurrent receiver,* where the LNA amplifies the signal in both of the desired bands. This is because one band is the image of the other and there is no attenuation of the image by either the antenna or the filter. The situation is exacerbated by the LNA gain in the image band. In this scenario, one is solely relying on the image rejection of the single sideband receiver, which is limited by the phase and amplitude mismatch of the quadrature LOs and the signal paths, and is insufficient in a concurrent receiver.

An alternative approach that does not suffer from the above problem and, in fact, significantly improves the image rejection is to use an offset LO as shown in Fig. 2. The LO frequency is offset from the midpoint of the two bands (f_A and f_B) in such a
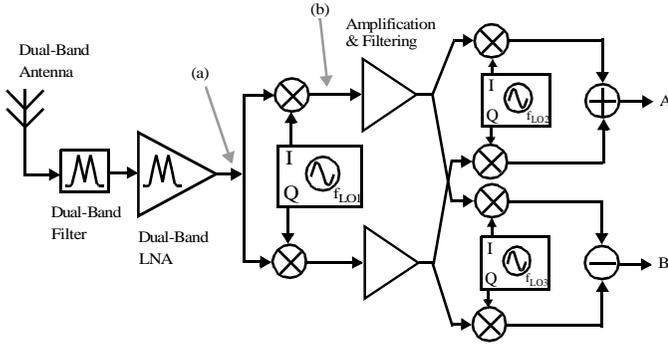
Fig. 1: An architecture for concurrent dual-band receiver.

Fig. 2: Frequency domain signal evolution in the concurrent receiver

way that the image of the first band at f_A falls at the notch of the front-end transfer function at f_{IA}. The attenuation at the notch frequency is determined by the compounded attenuation of the dual-band antenna, filter, and LNA. Similarly, the image of the second band at f_B will fall outside the pass-band of the front-end at f_{IB} and will be attenuated, accordingly. Using a quadrature first LO makes the stage fit to act as the first half of any single-sideband image reject architecture, such as Weaver [6]. Since the receiver has to demodulate two bands concurrently and independently, two separate paths *must* be used eventually. Each path comprises of the second half of the image reject architecture, as shown Fig. 1 which provide further image rejection. This architecture eliminates an extra antenna, a front-end filter, an LNA, and a pair of front-end mixers, which in turn result in power, footprint and area savings. At the same time large image rejection in excess of that of the single-sideband receiver is achieved through diligent frequency planning.

Concurrent Multi-Band LNAs

This section is dedicated to a generic approach to the design of a general class of integrated concurrent multi-band LNAs as one of the essential building blocks of concurrent dual-band receivers discussed earlier. It is crucial to note the fundamental difference between this approach and the existing ones. In conventional dual-band LNAs, either one of the two single-band LNAs is selected according to the instantaneous band of operation [7][8], or two single-band LNAs are designed to work in parallel using two separate input matching circuitry and two separate resonant loads[5]. The former approach is non-concurrent, while the latter consumes twice as much power. The other existing approach is to use a wideband amplifier in the front-end. Unfortunately, in a wideband LNA, strong unwanted blockers are amplified together with the desired frequency bands and significantly degrade the receiver sensitivity. In this work, concurrent multiband LNAs are proposed as an alternative to alleviate these problems.

In a single-band LNA, passive circuits are used to shape the wideband transconductance of the active device in the frequency domain to achieve gain and matching at the frequency of interest. This concept can be generalized to multiple frequency bands noting that the intrinsic transconductance of the active device is inherently wideband and can be used at multiple frequencies simultaneously.
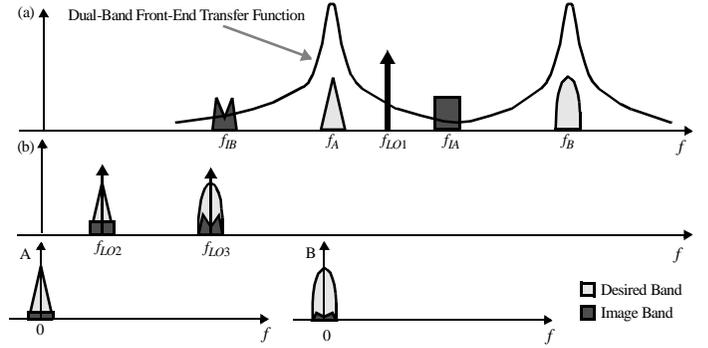
Fig. 3 shows the general case of a transistor with arbitrary gate impedance, Z_g, gate-source impedance, Z_{gs}, source impedance Z_s, gate-drain impedance Z_{gd}, and load impedance Z_L. The impedances shown in Fig. 3 also include transistor's inherent reactance components($e.g.$, C_{gs}). The effect of Z_{gd} is neglected in the subsequent derivation of expressions for noise, gain and matching parameters at different frequencies. It is possible to carry out a complete analysis which is beyond the scope of this paper [9].

Ignoring the noise contribution of passive elements, the total noise of this stage can be represented by its input equivalent voltage and current noise:

$$i_n = \frac{i_{nd}}{g_m Z_{gs}} + i_{ng}$$

$$e_n = \frac{Z_{gs} + Z_s + Z_g}{g_m Z_{gs}} \cdot i_{nd} + (Z_s + Z_g) \cdot i_{ng}$$

(1)

where i_{nd} and i_{ng} are the drain and gate noise currents (collector and base noise currents in a bipolar implementation), and g_m is the transconductance of the transistor.

To obtain more insight into the design trade-offs, we ignore the gate noise (that usually contributes less than 0.2dB to the *NF*), in the expression for the noise factor, *F*, that is given by:

$$F = 1 + \frac{\overline{|i_n + Y_s e_n|^2}}{\overline{i_s}^2}$$

$$\approx 1 + \frac{\gamma g_{d0}}{Y_s} \cdot \frac{1}{g_m^2 |Z_{gs}|^2} \cdot |1 + Y_s(Z_{gs} + Z_s + Z_g)|^2$$

(2)

where g_{d0} is the zero-bias drain-source channel conductance, Y_s is the reference source admittance ($e.g.$, Y_s=1/50Ω) for the noise figure, *NF*, i_s is the noise current associated with this source admittance, and γ is the excess noise factor for the MOS transistor ranging from 2/3 for long-channel devices to more than 2 for short-channel devices [10].

Several useful design implications can be obtained from (2). First of all, this equation agrees with the well-accepted notion that *NF* can be reduced using a larger g_m (more power dissipation). It also shows that an increase in Z_{gs} improves the *NF*, that accounts for the improvement in noise figure for transistors with smaller channel length and C_{gs}. The last term in (2) plays
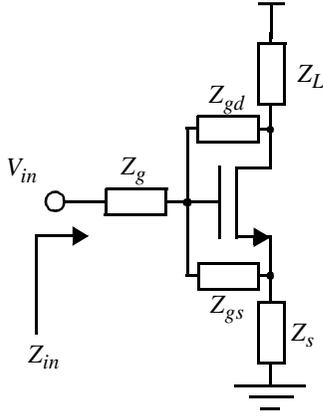
Fig. 3: General model for single-transistor amplifier

Fig. 4: Concurrent dual-band CMOS LNA (biasing not shown)

the most important role in the design of concurrent multiband LNAs. Since passive components cannot produce any negative real part, the last term reaches its minimum when $Z_{gs} + Z_s + Z_g = 0$ at the frequency(ies) of interest. Thus, the minimum NF will be achieved for these frequency(ies).

Another important feature of an LNA is its input impedance matching for maximum power transfer. Neglecting Z_{gd}, the input impedance of the amplifier in Fig. 3 is given by:

$$Z_{in} = Z_{gs} + Z_s + Z_g + g_m Z_s Z_{gs} \qquad (3)$$

To achieve simultaneous noise and power match at the input, (2) and (3) should simultaneously satisfy the minimum NF and input matching condition at all frequencies of interest, *i.e.*,

$$\begin{cases} Z_{gs} + Z_s + Z_g = 0 \\ g_m Z_s Z_{gs} = R_{in} = 50\Omega \end{cases} \forall \omega_{in-band} \qquad (4)$$

In addition to these conditions, it is crucial to maximize Z_{gs} and g_m to minimize NF as much as the power budget allows.

To demonstrate the validity of these expressions, consider the special case of a single band LNA inductive source degeneration similar to that of [1], where (4) reduces to:

$$\begin{cases} (L_g + L_s)C_{gs}\omega^2 = 1 \\ \dfrac{g_m L_s}{C_{gs}} = R_{in} = 50\Omega \end{cases} \qquad (5)$$

in accordance with [1].

The general design criteria given by (4) can be used to generate a large number of different topologies for concurrent multi-band LNAs. The following section presents an example of such.

A Concurrent Dual-Band CMOS LNA

A large number of passive networks satisfy the design criteria of (4). In order to minimize the NF, one should maximize Z_{gs}, as previously mentioned. One way to obtain a reasonably large Z_{gs}, is to use a transistor with minimum channel length and no extra passive element between the gate and the source. The second condition of (4) can be satisfied using a single on-chip source degenerative inductor. To fulfill the first condition of (4) at both frequencies, a parallel LC network in series with the
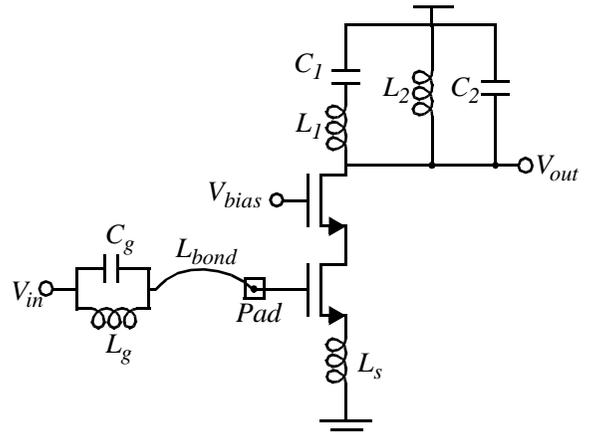
inevitable inductance of the bonding wire and package lead is used as shown in Fig. 4. The parallel LC of Z_g resonates with $Z_{gs}+Z_s$ at both frequency bands of interest.

In order to achieve narrow-band gain at bands of interest, the drain load network should exhibit high impedance only at those frequencies. This can be done by adding a series LC branch in parallel with the parallel LC tank of a single-band LNA, as shown in Fig. 4. Each series LC branch introduces a zero in the gain transfer function of the LNA at its series resonant frequency. The frequencies of the zeros determine the frequency of the notches in the transfer function, which are used to greatly enhance the image rejection of the receiver, as discussed earlier and shown in Fig. 2.

Measurement Results

This section presents the measurement results of a concurrent dual-band CMOS LNA operating at 2.45GHz and 5.25GHz frequency bands for indoor wireless communications. The design is based on the topology of Fig. 4, which is one example of the general concept of the concurrent multi-band LNA. It is implemented in a 0.35μm BiCMOS technology using only CMOS transistors. The input parallel resonator is made using a 0.9pF porcelain multilayer capacitor and a 2.7nH chip inductor.

Fig. 5 shows the measured voltage gain, A_v, and input reflection coefficient, S_{11}, of the amplifier up to 10GHz. It achieves narrow-band voltage gains of 14dB and 15.5dB, input return losses of 25dB and 15dB, and noise figures of 2.3dB and 4.5dB at 2.45GHz and 5.25GHz, respectively. It drains 4mA of current from a 2.5V supply voltage. The notch due to the LNA is about 40dB deeper than the peaks which directly translated to the same amount of improvement in image rejection. Due to the large difference between the notch and pass-band frequencies, no elaborate tracking loops such as those proposed in [11] are necessary. The single-ended nature of the LNA makes external Baluns unnecessary. Measurements of 6 different chips with 3 different boards and off-chip components show strong repeatability *without* using the commonly-used sliding capacitor input matching adjustment.

An LNA's linearity is often measured by intermodulation and compression point tests and represented by IP3, for 3rd order non-linearity, and CP1 for 1dB compression point. We refer to these in-band IP3 and CP1, as IP3$_{inband}$ and CP1$_{inband}$. How-

ever, in a multi-band system, more non-linearity measures should be considered. In-band signals from different desired bands (*e.g.*, 2.50GHz and 5.15GHz) can mix due to amplifier's non-linearity, causing in-band undesired signals (*e.g.*, 3x2.50 - 1x5.15 = 2.35 due to 4th order non-linearity), as shown in Fig. 6. We show this cross-band IPn, as IP$n_{crossband}$, where n is the order of non-linearity. A similar cross-band compression measure can be defined as the signal power in band *A* that causes a 1dB drop in the small signal gain in band *B* and vice versa, which will be denoted as CP1$_{A>B}$.

The concurrent dual-band LNA demonstrates an input-referred in-band IP3 of 0dBm and 5.6dBm, and in-band CP1 of -8.5dBm and -1.5dBm at 2.45GHz and 5.25GHz bands, respectively. The measured input referred IP4$_{crossband}$ is 7.5dBm. The LNA exhibits an CP1$_{2.4>5.2}$ of -11.5dBm and an CP1$_{5.2>2.4}$ of -5.7dBm.

The following table summarizes the measured performance of the fabricated concurrent dual-band LNA shown in Fig. 7. The chip occupies an area of 0.8x0.8 mm^2 including pads and ESDs. The *NF*, S_{11} and power dissipation are better than previously published non-concurrent and/or single-band CMOS LNAs.
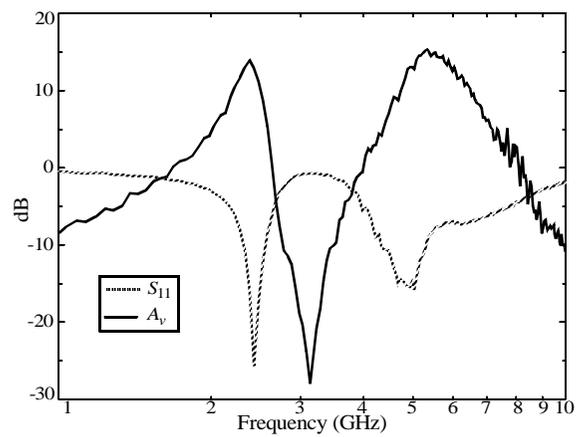

Fig. 5: Measured voltage-gain and S_{11} in dual-band CMOS LNA
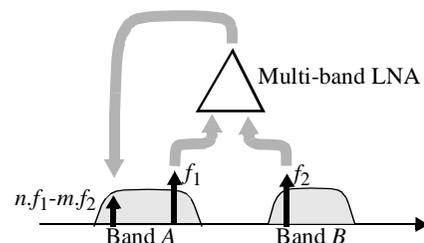
Fig. 6: Illustration of crossband intermodulation.

Frequency	2.45GHz ± 50MHz	5.25GHz ± 100MHz
Voltage Gain	14 dB	15.5 dB
S_{11}	-25 dB	-15 dB
NF	2.3 dB	4.5 dB
Input IP3$_{in-band}$	0.0 dBm	5.6 dBm
Input CP1$_{in-band}$	-8.5 dBm	-1.5 dBm
Input CP1$_{A>B}$	CP1$_{2.4>5.2}$= -11.5 dBm	CP1$_{5.2>2.4}$= -5.7 dBm
Input IP4$_{cross\_band}$	7.5 dBm	
DC Current	4mA	
Supply Voltage	2.5V	
Active Device	0.35μm CMOS transistors	

Conclusions

A new concurrent dual-band receiver architecture capable of simultaneous operation at two different frequency bands is introduced. It uses a novel concurrent dual-band LNA, combined with an elaborate frequency conversion scheme to reject the out-of-band signals. This work provides a general methodology for the design of concurrent multiband LNAs to achieve simultaneous narrow-band gain and matching at multiple frequencies. The effectiveness of the proposed methodology is demonstrated through measurement results of a CMOS implementation of the integrated concurrent dual-band LNA that achieves a superior *NF*, S_{11}, and power dissipation over previously published non-concurrent and/or single-band LNAs.

Acknowledgments
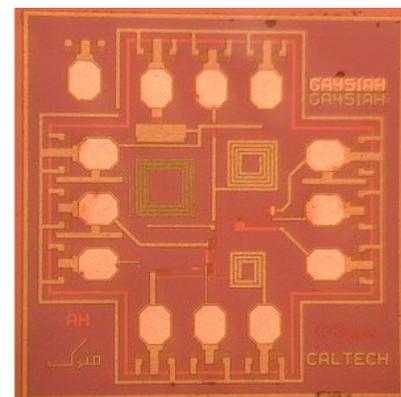
Fig. 7: Chip micrograph of dual-band CMOS LNA.

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