Closed-Loop Spurious Tone Reduction for Self-Healing Frequency Synthesizers

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***Abstract* — On-chip spurious tone detection and correction in an 8-12 GHz CMOS synthesizer is used to automatically reduce spurious output tones at different offset frequencies by up to 20dB. Using synchronous detection, sensitivity is limited by detection time only. The presented methods are generally applicable to frequency synthesizers and phased-locked loops in various applications.**

***Index Terms* — phase locked loop, frequency synthesizer, spurious tones, VCO reference spur, spur reduction techniques, spurious tone suppression, sampled loop filter**

I. Introduction

Spurious tones in phase-locked loop (PLL) synthesizers are undesirable for many reasons: in radio transmitters, spurs are transmitted alongside the RF carrier, interfering with users in adjacent channels. In radio receivers, spurs down-convert signals in adjacent radio channels to base-band, causing interference and degrading sensitivity. In clock-and data recovery circuits that use PLLs (e.g. [1]), spurs can cause increased bit-error rates in the recovered data due to edge-transition timing inaccuracies in the recovered clock. In fractional-N synthesizers, reference spurs in the oscillator output are dithered alongside the main tone, resulting in increased synthesizer noise.

Side-tone spurs in synthesizers are typically introduced through frequency-modulation (FM) of the carrier signal, and are more problematic than amplitude-modulated (AM) tones as gain limiting operations attenuate AM spurs. In PLLs, the voltage-controlled oscillator (VCO) is typically FM modulated by periodic disturbances of the control voltage due to the loop action. In practice, many techniques are employed to reduce the disturbance: use of sample-and-hold loop-filter [2], feedback-based methods to reduce charge-pump mismatch [3], methods reducing the VCO gain upon lock [4], and methods to adjust the timing of control voltage actuation with sub-sampling phase-detectors [5]. All of the above methods attempt to either minimize the control voltage ripple in an open-loop fashion or the resulting FM modulation. In this paper, we present a true closed-loop spurious reduction using sensing and actuation of the oscillator control voltage ripple to offset the effects of parasitic capacitance charge feed-through, process, device mismatch, and temperature sensitive variations directly.

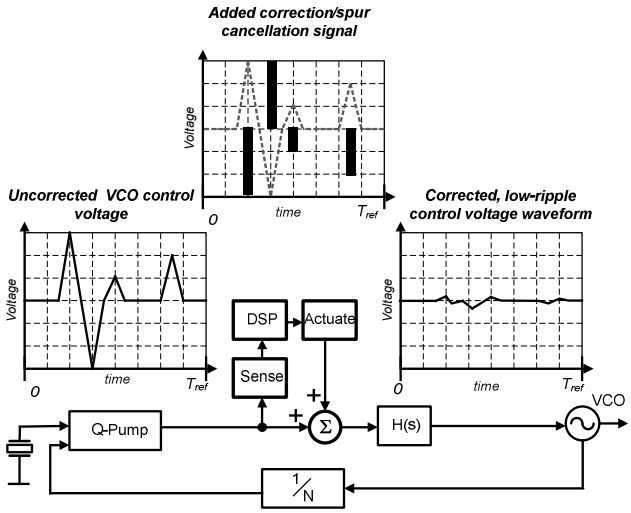

Fig. 1. – Closed-loop reduction of VCO control voltage ripple in the presented scheme: injected pulses approximate the inverse of the uncorrected control voltage, reducing overall spurious tone power, particularly in lower harmonic components that are difficult to filter.

II. Concept

Figure 1 illustrates our approach conceptually: the VCO control voltage signal is digitally sampled for processing in a DSP unit. For actuation, a periodic correction signal (error signal) is added to minimize the AC disturbance on the control voltage. Ideally, the correction signal is the true inverse of the original, analog control voltage disturbance such that the sum of the two signals is zero. However, to reduce power and area overhead in the correction signal generator, the correction signal is approximated using narrow, digitally generated pulses. In steady-state, both the detected as well as the generated error signal are synchronized to the reference signal and, hence, periodic. Therefore, the periodically injected pulse contains fundamental and harmonic components of the reference frequency, and N injected pulses of controllable amplitude and phase provide 2•N degrees of freedom to control the amplitudes and phases of the first N harmonics of the injected signal. The remaining difference contains mostly high-frequency components that are strongly attenuated by the loop filter.

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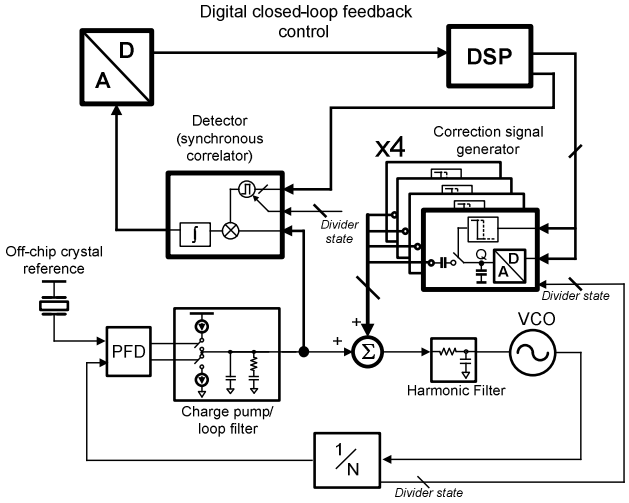

Fig. 2. Implemented system block diagram. A programmable, on-chip correlator and correction signal generator sense and actuate the AC control voltage disturbance. Off-chip digital signal processing closes the feedback loop.

To demonstrate close-loop reduction of spurious tones using the above concept, a PLL including a detector and a correction signal generation circuit has been implemented.

The details of the implementation as well as measured results are discussed in the remainder of this paper.

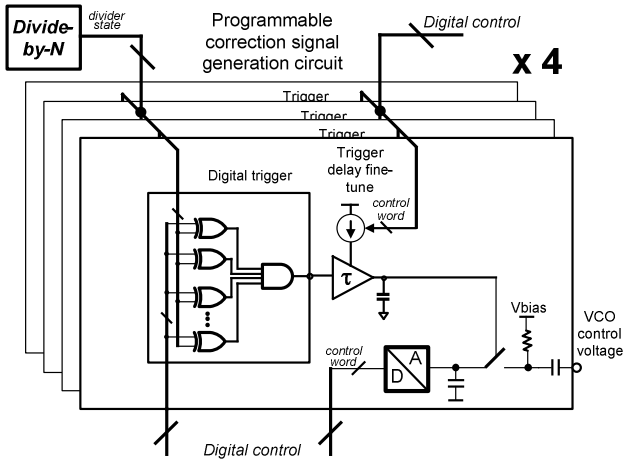

Fig. 3. Digitally controllable charge injection circuit. A periodic trigger signal is generated once during the reference clock cycle by comparing the divider state to a control word. Additional programmable delay allows fine-tunes the timing of the trigger signal. At the trigger, a programmable charge is injected into the VCO control voltage, causing a temporary, pulse-like disturbance of the control voltage. Four channels are implemented.

III. Implementation

A. System Block Overview

Figure 2 shows a block diagram of the complete synthesizer. The control voltage waveform sensing circuit is implemented as a sub-sampling correlator, and the time samples are used to reconstruct the control voltage signal. Details of the sensing and reduction

The implemented PLL core itself uses a 50MHz off-chip reference signal, and can be tuned from 7-12GHz. The overall PLL loop bandwidth is 800kHz-1.2Mhz, depending on the operation frequency. Including switched capacitor banks for coarse tuning control, the VCO gain k_{vco} is 2GHz/V typically for midrange control voltages. The divide-by-N circuit generates N distinguishable states used for providing timing information to generate programmable trigger signals in the detector and correction signal generator. The PLL loop is closed with a charge pump and 3rd order loop filter.

B. Error Signal Generation

The error signal generator (Figure 3) consists of four parallel, digitally controlled charge-pulse injection channels. For each channel, a programmable amount of charge can be injected into the control voltage node at a programmable time-instant during the reference clock cycle. The charge is injected into the control voltage node periodically by closing a switch once during a reference clock cycle. With four channels, four independently controllable injections can be made during each reference clock cycle. The trigger for the switch is generated by first comparing the divider state to a programmable known state, generating a trigger signal at a state transition point of the divider. A programmable, current-starved delay cell provides additional timing control. The four parallel channels can generate a waveform synchronous to the control voltage waveform, allowing up to eight degrees of freedom.

C. Control Voltage Waveform Detection

The control voltage waveform detector (Figure 4) uses synchronous correlation to sub-sample the periodic control voltage waveform at successive time-steps throughout the reference clock cycle. Using a subset of the N divider states as timing reference, timing edges synchronous to the control voltage disturbance are used to create correlation time windows. The control voltage is amplified and band-pass filtered to remove DC information and to filter high frequency components above 400MHz. With

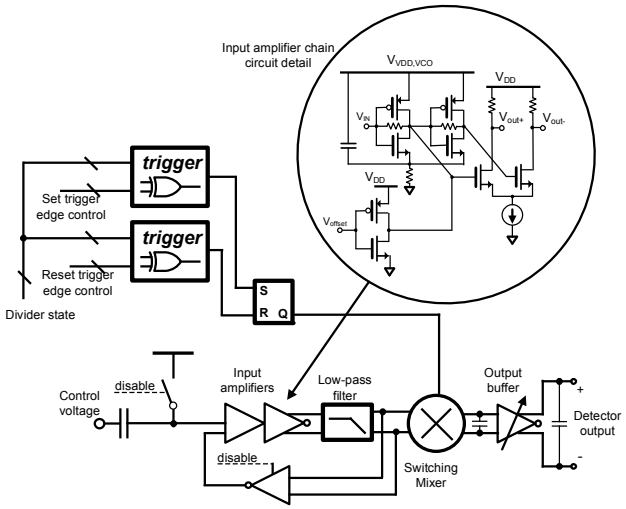

Fig. 4. Control voltage waveform detector (correlator). Correlation time-windows are selected by comparing the divider state with programmable edge control words. The mixer output is integrated on a capacitor. Circuit detail of the input amplifier chain is shown including DC offset correction input. The input amplifiers have a band-pass response to minimize aliasing.

twenty or more samples used, the Nyquist frequency is 500Mhz or above.

Because the detector operates synchronously, sensitivity is limited only by the integration time used at the output. In the implemented circuit, 1us integration time is sufficient to detect a 10uV input signal with a signal-to-noise ratio of 3:1 (corresponding to a -70dBc reference spur level at typical operating points). Better sensitivity can be achieved using larger times.

D. Digital Closed-Loop Control and Spurious Power

Let A_n denote the signal amplitude of the nth reference harmonic on the control voltage line, f_{vco} the VCO frequency, N the PLL division ratio and k_{vco} the VCO gain. For a single-frequency tone, the FM-modulation index corresponding to signal is given by

$$\beta_n = \frac{k_v \cdot A_n \cdot N}{n \cdot f_c}. \quad (1)$$

Assuming that $\beta_n << 1$ for all n, it can be shown that the total spurious power is approximately

$$\left(1 - J_0\left(\sqrt{\Sigma_n \beta_n^2}\right)\right)^2, \quad (2)$$

where J_0 is the zeroth-order Bessel function of the first kind. To minimize total spurious power, the sum of A_n/n squared for a suitable number of n harmonics should be minimized. With An for each n up to the Nyquist frequency obtained from the detector, an approximate total spur power can be calculated.

The loop is closed with a digital back-end using the following algorithm: for each offset signal channel, the delay of an injected test pulse is swept, and extrema in total spur power are detected. At the most significant extrema, a gradient descent using successive approximation is performed to determine the optimum injected pulse strength.

Besides the above described algorithm, alternative feedback algorithms are possible depending on the available digital signal processing power and memory.

Because the processes responsible for spur generation are parasitic in nature and change slowly in time (e.g. voltage, temperature, ageing), the required duty-cycle for sensing can be kept very low. The circuit can be corrected – or, in a sense, self-healed – prior to operation. This greatly minimizes power overhead for the detection circuit due to a low duty cycle. Furthermore, this allows our method to be applied to fractional-N synthesizers as well, as the synchronous spurs can be self-healed for each division modulus separately prior to operation.

IV. Measurement Results

The PLL is implemented in a low-power 65nm CMOS process. Test chip dimension are 1.4mm x 0.9mm, with 150um x 50um and 130u x 80u um used by the detection and correction signal circuits, respectively. Figure 5 shows a photograph of the test-chip. The PLL frequency output spans 7.4GHz to 12.4GHz using a 50MHz reference signal. The phase noise at 1MHz offset is about -100dBc, depending on the programmed frequency. Activation of the elimination circuit has no measureable impact on

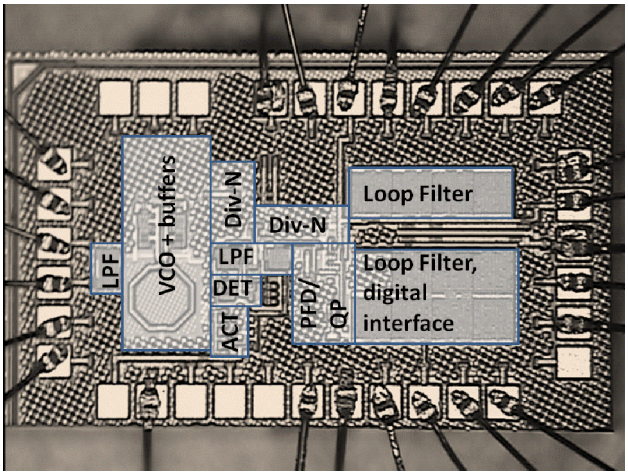

Fig. 5. Die photograph of the self-healing phase-locked loop circuit. The die measures 1.4mm by 0.9mm. DET – spur detector, ACT – correction signal generator; LPF – loop filter

TABLE I
FUNDAMENTAL SPURIOUS POWER

f_o [GHz]	**12.0**	**11.2**	**10.4**	**9.6**	**8.8**	**8.0**
nominal [dBc]	-44.2	-51.3	-51.8	-57.2	-55.5	-59.4
corrected [dBc]	-56.6	-63.1	-72.2	-70.7	-74.4	-62.1

broadband phase noise. The PLL consumes 138mW including 50Ω drivers for the VCO and the VCO-divide-by-2 outputs. Assuming an in-situ duty cycle of 0.1%, the detection circuit consumes 16uW when operated. The digital back-end can be run on a similar duty cycle. The elimination circuit core consumes approximately 5mW, with further reduction possible.

Figures 6 and 7 show typical output spectra before and after correction for operation at 10.4GHz and 12GHz respectively. Before correction, the dominant spurs have powers of -45dBc to -50dBc. When comparing with other designs, it should be noted from (1) that similar error amplitudes A_n on the control voltage line result in different modulation indexes and hence spur levels for different designs. After correction, the total spurious power is typically reduced by 6dB or more. Due to implementation issues only two of the four elimination channels were operable. The achieved spurious tone reduction is stable over significant times (hours and days) in the measurement set-up. Over frequency, the fundamental spur is typically reduced by 10dB (table I). The residuals spurious power is likely due to other spur generating mechanisms that are not detected on the control voltage.

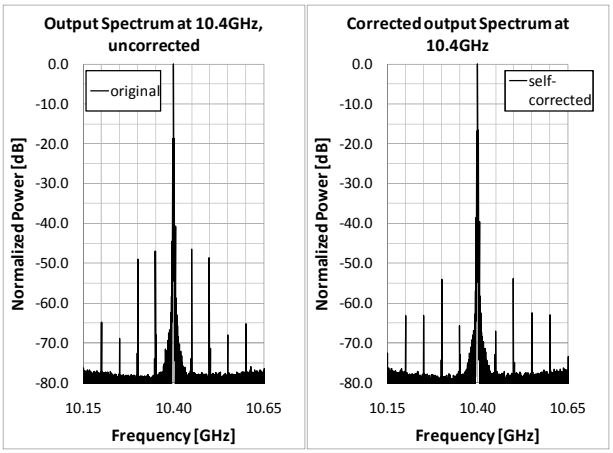

Fig. 6. VCO output spectrum before and after spurious tone correction for a VCO center frequency of 10.4 GHz. The VCO output is amplitude limited to remove amplitude modulated components. Total spurious power is reduced by 20dB.

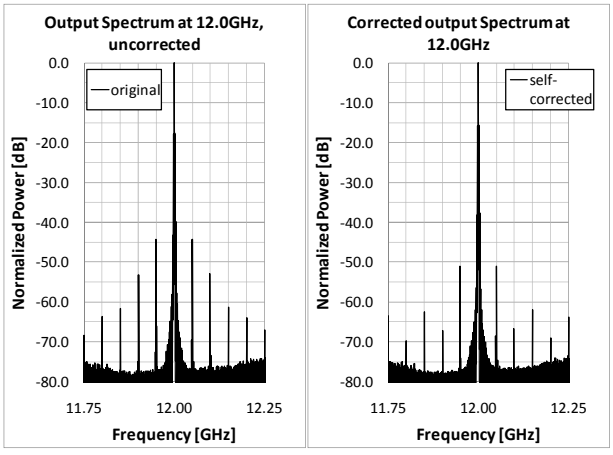

Fig. 7. Uncorrected (left) and corrected (right) output spectrum at 12GHz. The IC is packaged in a 28-pin PLCC. Total spurious power is reduced by 12dB.

V. CONCLUSION

A closed-loop, direct spurious tone detection and actuation method has been demonstrated. The scheme is applicable to a wide variety of synthesizer applications such as transmit and receive LO generation for both integer-N and fractional-N synthesizers. To the best of the author's knowledge, this is the first spur correction scheme employing direct detection and actuation of control voltage disturbance in frequency synthesizers.

ACKNOWLEDGEMENTS

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