An Integrated Traveling-wave Slot Radiator

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Abstract — A traveling-wave integrated slot radiator is designed using electromagnetic duality theory based off of the ring portion of a radial multi-port driven radiator to minimize the area required exclusively for the antenna. It is designed in 32 nm SOI CMOS and driven by a buffered quadrature VCO at 4 points to create the traveling wave that radiates out of the backside of the chip. It is measured to have a maximum EIRP of 6.0 dBm at 134.5 GHz with a total radiated power of -1.7 dBm while drawing 168 mW DC power.

Index Terms — antenna theory and design, CMOS integrated circuits, integrated radiators, millimeter-wave silicon RFICs, on-chip antennas.

I. INTRODUCTION

Electromagnetic radiation at mm-wave frequencies above 100 GHz can enable applications in active imaging for security or biological uses as well as being used for wide-bandwidth high data rate short-range data transfer. CMOS transistor scaling due to Moore’s law has increased the maximum possible oscillation frequency to these frequencies, but transferring mm-wave power above 100 GHz off chip is challenging due to the inductance and resonances associated with traditional wirebonds and flip-chip methods as the size of these elements approach and surpass the wavelength of the signal. Because the integrated circuit (IC) itself is on the same order of magnitude as the wavelength at these frequencies, integrating the drivers and antennas on the same substrate to create an integrated radiator has become feasible. Recent work has shown that reasonable efficiencies and power levels of integrated radiators can be achieved without the need for external dielectrics or lenses [1]–[3], decreasing the cost and volume requirements of such devices significantly.

One issue with integrating antennas on chip is the active area they consume. In modern silicon processes, the cost of the chip is determined by its area, and as the size of the antenna is often one of the dominate factors that determine the area, finding ways to reduce the footprint of the antenna is of great importance. In wire-based antennas such as dipoles, loops, or traveling-wave ring antennas, the ground plane of the chip must be pulled away from the antenna to prevent mirror currents that could cancel out the radiation, requiring large areas of the chip to be left empty. Even metal fill can greatly reduce the radiation efficiency of the antenna, and must either be excluded at a risk to yield, or accommodations to the design must be made to utilize a low fill level area such as an inductor layer that comes with additional design rules to maintain acceptable yields. One possible way to get around this area requirement is to create integrated slot antennas that do not require large open areas in the ground plane [4].

Electromagnetic duality theory [5], enables slot antennas to be designed and analyzed by introducing a fictitious magnetic current that flows through the slot, and then comparing that to a wire antenna that is created by inverting the entire antenna plane’s metal. The lines of the antenna now become slots, and the open space around the lines become metal. The E and H fields of the slot antenna are then replaced by the fields H and −E for the wire antenna, as shown in Figure 1. This means that a radiator can be designed using the design principles and intuition of wire antennas and then inverted to its slot dual, and all of the previously unused open space becomes a ground plane that can shield supporting circuitry, thus reducing the required area of the radiator.

Fig. 1. Electromagnetic duality theory is used to design slot-based antennas by inverting the metals on a plane, leading to E and H fields being replaced by H and −E. A dipole is the complement to a slot dipole, and a traveling-wave ring antenna is the complement to the traveling-wave slot ring antenna.

II. RADIATOR DESIGN

This radiator takes advantage of the benefits of multi-port driven (MPD) radiators [1], while also reducing the
required area of the antenna by using slot-based design. The antenna then also acts as a power combiner, eliminating a block that can cause loss when integrated on-chip.

Electromagnetic duality theory is used to create the radial slot MPD radiator. In this case, the antenna that we are going to invert is the ring of the radial MPD antenna [1]. This means that when inverted, the antenna becomes a slot ring as depicted in Figure 2, where there is an internal metal plane that is surrounded by a thin slot ring, which itself is surrounded by a large outer metal plane.

![Fig. 2. Depiction of the traveling-wave slot radiator, with driver circuitry at the core which produces quadrature signals that drive the slot ring at four points to create the traveling wave, producing radiation mainly through the backside of the silicon substrate.](image)

The slot ring is driven in quadrature at four separate points, as shown in Figure 2. This produces a traveling wave around the ring that generates a circularly polarized radiated field. Similar to the wire version of the MPD antenna, all of the driver circuitry can be located at the center of the radiator, and because the AC ground planes begin at the edge of the slot, they do not need to be pulled back to maintain effective radiation. This means that the area occupied exclusively by the antenna needs only to be the slot itself, and enough of the ground plane on either side to provide enough shielding to prevent any unwanted feedback paths. Due to the higher dielectric constant of the silicon substrate, the majority of the power initially goes down into the substrate, and thus the primary beam is formed coming out of the backside of the substrate.

The feeds for this antenna operate by using micro-strip transmission lines whose ground reference is the inner metal plane, and directly connecting the signal line of the T-line to the outer metal plane. The DC supply voltage for the driver circuitry is supplied through the antenna feeds through outer AC ground plane, while the DC ground is connected to the inner ground plane, and then taken out to the edge of the chip along a single line that is perpendicular to the slot as it crosses it to minimize the interaction with the antenna. This asymmetry will cause the radiation pattern to deviate from being circularly polarized to being somewhat elliptically polarized.

The antenna is simulated using 3D FEM simulator Ansoft HFSS to have a maximum gain of 3.0 dBi, with a radiation pattern shown in Figure 3 and a radiation efficiency of 39% using a standard 250μm thick 10 Ωcm substrate.

![Fig. 3. Simulated pattern of antenna gain for the slot ring antenna shows a maximum gain of 3.0 dBi, with a radiation efficiency of 39%.](image)

Figure 4 shows the circuit block diagram of the radiator. A quadrature voltage controlled oscillator (QVCO) is implemented at the center of the inner ground plane. The two differential output pairs, in phase (OSC₀ and OSC₁₈₀) and quadrature (OSC₉₀ and OSC₂₇₀), of the QVCO go through three stages of differential buffer amplifiers to provide the final outputs P₀, P₁₈₀, P₉₀, and P₂₇₀ to feed the antenna. Differential amplification allows the use of differential inductors for buffer stages providing virtual grounds on the inductors to reduce the amount of required bypass capacitance. In order to properly drive the antenna with correct phases, two of the output lines, P₉₀ and P₁₈₀, need to cross each other so that the correct sequence of P₀, P₉₀, P₁₈₀, and P₂₇₀ appears on the corresponding driving points of the antenna. To match the additional delay of P₉₀ and P₁₈₀, the other two feed lines, P₀ and P₂₇₀, are meandered to provide additional delay.

The QVCO consists of two cross-coupled oscillators which are coupled to each other through two mechanisms: Resistive coupling, Rₑ, and parallel transistor coupling, Mₑ, as shown in Figure 5. The resistive coupling ensures that the oscillator coupling is strong enough to allow quadrature mode oscillation but also supports two other modes, common-mode oscillation and in-phase differential oscillation. In order to force the two VCOs to oscillate in quadrature mode, parallel transistor coupling is added.
Fig. 4. Block diagram of the driver circuitry of the slot radiator. A quadrature VCO generates the four required phases to drive the antenna and three buffers amplify QVCO’s outputs to provide sufficient output power.

Although strong-enough parallel transistor coupling on its own results in quadrature oscillation, simultaneous use of the two coupling mechanisms lowers the required quadrature coupling strength thus allows us to use smaller transistors, with less coupling strength which lowers phase noise degradation due to strong quadrature coupling. In this design, $M_x$ is $30\mu m$ wide for the cross-coupled transistors and $M_c$ is $3\mu m$ wide for coupling transistors to provide sufficient quadrature coupling.

Fig. 5. Schematic of the QVCO incorporating resistive coupling as well as parallel transistor coupling simultaneously to ensure quadrature oscillation.

The three amplifier buffers are all cascode differential amplifiers and are sized to deliver enough power to the antenna driving points and also to allow proper impedance matching between the stages, Figure 6. All four transistors in each amplifier are of the same size; $M_1$ is $20\mu m$ wide for the first stage, $M_2$ is $40\mu m$ wide for the second stage, and $M_3$ is $60\mu m$ wide for the output stage. AC coupling capacitors are used between the stages.

Fig. 6. Schematics of the differential buffer chain including three cascode amplifiers sized appropriately for power amplification and impedance matching.

III. MEASUREMENTS

The chip was fabricated in a 32 nm SOI CMOS process with 11 copper metal layers and one aluminum top metal layer. The inner ground plane was implemented on m5 and m6, the outer ground in m8 and m9, and the transmission lines in the top copper. A $6\mu m$ wide fill exclusion was used around the slot and fill exclusion was also used under the inductors. It is mounted on transparent tape to enable backside radiation and wirebonded to a PCB, as shown in Figure 7.

The power is received by a 23 dB gain linearly polarized horn antenna 9 cm away from the chip. The antenna feeds an 11th harmonic mixer that feeds a signal generator. The measurement system was calibrated for absolute captured power using a calorimeter-based Erickson Power Meter. The PCB was mounted onto a two dimensional stepper motor to enable radiation pattern measurement as well as measurement of total radiated power.

Fig. 7. Measurement setup including 2-D stepper motor for radiation pattern measurements for both absolute power calibration (a) and using an 11th harmonic mixer that feeds a spectrum analyzer (b).
When located broadside to the chip, the receive antenna captured 1.55 mW combined from both orthogonal linear polarizations, which corresponds to a maximum measured EIRP of 6.0 dBm from its single radiating element. Integrating the entire radiated power of the half-space yields a -1.3 dBm radiated power from the backside beam. Figure 8 shows the measured calibrated spectrum of the broadside radiation. The chip consumes 168 mW of DC power from a 1.2 V source and occupies an area of 1.2 mm$^2$.

The axial ratio of the polarization in the broadside direction is measured to be 3.3 dB. The cause of deviation from circular polarization is likely due to the asymmetry of the line extending out over the slot to the ground bondpad, and possibly from small chips in the backside of the silicon substrate from dicing that could be causing unwanted reflections.

The stepper motors were also used to rotate the chip in two dimensions to measure the radiation pattern shown in Figure 9. In order to measure the entire power of the elliptical polarization, the motors were swept twice with the linearly polarized receive antenna oriented in both horizontal and vertical polarizations.

A comparison to other integrated radiators in silicon without external dielectrics or lenses is shown in Table I. The die photo of the slot radiator is shown in Figure 10. The blocks of the radiator are marked in the inset.

**TABLE I**

<table>
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<tr>
<th>Metric</th>
<th>This Work</th>
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<th>[2]</th>
<th>[3]</th>
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<tr>
<td>Rad. Power (dBm)</td>
<td>-1.3</td>
<td>-2.0</td>
<td>-2.4</td>
<td>n/a</td>
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<tr>
<td>Max. EIRP (dBm)</td>
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<td>4.6</td>
<td>-1.9</td>
<td>5.13</td>
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<tr>
<td>Frequency (GHz)</td>
<td>134.5</td>
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<td>191</td>
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<td>Num. of Elements</td>
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<td>1</td>
<td>4</td>
<td>4</td>
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<tr>
<td>EIRP/Element (dBm)</td>
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<td>4.6</td>
<td>-1.9</td>
<td>-0.87</td>
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<tr>
<td>DC Power (mW)</td>
<td>168</td>
<td>388</td>
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<td>Area (mm$^2$)</td>
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<td>3.5</td>
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<td>130 nm SiGe</td>
<td>65 nm CMOS</td>
<td>32 nm SOI CMOS</td>
</tr>
</tbody>
</table>

Fig. 8. Measured calibrated spectrum of the broadside radiation shows power captured to be -25.1 dBm, which corresponds to a 6.0 dBm EIRP.

Fig. 9. Measured antenna pattern in both elevation and azimuth planes.

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**REFERENCES**


