

19.5 A Versatile Multi-Modality Serial Link

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Serial data links are often designed targeting a specific transmission medium. High-speed links using different predetermined transmission media have been demonstrated in the past [1-3]. This, however, restricts user's ability to use an integrated link interface with other transmission media once the chip is fabricated. For example, traditional transceivers for copper interconnects typically transmit baseband data, which is incompatible with a free-space wireless channel that is bandpass in nature and often uses RF carriers. A multi-modality transceiver block compatible with different transmission media is highly desirable as it offers great versatility by allowing the exact same interface circuitry to be used with different transmission media. Such a versatile interface can relax the board and system design requirements and enable the reuse of the same transceiver core with different media, reducing the time and cost overhead of re-designing and re-manufacturing.

In this paper, we present a versatile multi-modality solution compatible with copper, plastic, and wireless media at data rates in excess of 20Gb/s. The exact same transceiver can transmit data over any of the three transmission media: conductive wireline, dielectric waveguide, and wireless, enabling a multi-modality highly-versatile interconnect solution, as shown in Fig. 19.5.1. Such multi-modality interconnect solution can transmit data on and even through a PCB, as well as between various boards and external devices using any combination of wireline conductive metal lines, dielectric waveguides, and wireless free-space or through the board using exactly the same circuitry.

To realize such a versatile interconnect, we use a spectrally-efficient multi-carrier frequency multiplexing/de-multiplexing approach (Fig. 19.5.2), which is robust to channel variations over wide bandwidth [4]. The versatile interconnect operating at millimeter-wave frequency is free from interfering to/from other devices operating at lower frequencies. One of the challenges in implementing a frequency multiplexing transceiver is the transition from on-chip to off-chip. Since it is highly desirable to use the smallest and simplest I/O, it is necessary to multiplex/de-multiplex multiple carriers onto/from a single pad to minimize the cost and complexity. Also the size of SoC itself is often determined by the number of I/O pads rather than the actual circuit area [5]. This challenge necessitates the development of low-loss, area efficient diplexer and de-diplexer circuits for frequency multiplexing transceiver. We use an impedance transformation technique for designing these circuits, which enables single-pad frequency multiplexing transceiver. Schematics of the diplexer and de-diplexer are shown in Fig. 19.5.3. The RX contains two receiver elements operating at different frequencies, whose inputs are connected through an impedance-transformation network. The impedance seen looking into one of the receiver elements from the connection point is designed to be close to 50Ω at its operation frequency (in-band) while it presents high impedance at the operation frequency of the other receiver element (out-of-band). In the 57GHz receiver element, the impedance looking from point A into the transistor side (Tr_1) is matched to 50Ω at the in-band, 57GHz. On the other hand, the impedance at the out-of-band, 80GHz, is designed in the inductive region. A transmission line (TL_1) is employed to rotate the out-of-band reflection coefficient in a clockwise direction on the Smith Chart to transform it into higher impedance while maintaining the in-band impedance close to 50Ω . After the transformation, as shown in the Smith Chart of Fig. 19.5.3, the impedance seen looking from point B into the 57GHz receiver element is around 50Ω at the in-band ($Z_{57G}(57G)$) while the one at the out-of-band ($Z_{57G}(80G)$) is $174+j11\Omega$. Similarly, in the 80GHz receiver element, the impedance looking from point B at the in-band (80GHz) is matched to 50Ω , and the one at the out-of-band is designed to be high impedance. In this way, the two

receiver elements can share a single common pad without strong influence on each other. The transmitter diplexer is also designed using this technique, thus two transmitter elements can share a single common pad to transmit signal. This impedance transformation-based diplexer/de-diplexer offers high frequency selectivity while occupying significantly less die area in comparison with a traditional frequency selection network.

Figure 19.5.4 shows the performance of TX and RX. The TX contains a diplexer, amplifiers, upconversion mixers, and VCOs, while the RX contains a de-diplexer, LNAs, downconversion mixers, VCOs, and BB amplifiers. The TX has conversion gains of 6.0dB and 5.9dB with output saturated powers of -7.2dBm and -2.6dBm in the 57GHz and 80GHz bands, respectively. The RX has conversion gains of 33.4dB and 19.6dB with input P_{1dB} of -41.0dBm and -25.3dBm at 57GHz and 80GHz, respectively. Evaluation of the effect of crosstalk interference from the other channel is an important consideration in a frequency multiplexing transceiver. This degradation is evaluated using crossband compression ($CP1_{A>B}$), which is the input power in one channel A that results in a 1dB reduction in the small-signal gain of the other channel B [6]. The RX exhibits $CP1_{80G>57G}$ of -9.6dBm and $CP1_{57G>80G}$ of 2.0dBm. TX and RX consume powers of 52mW and 85mW from 1.1V supply voltage, respectively.

The measurement set up of three demonstrated types of transmission modalities are shown in Fig. 19.5.5. The 57GHz and 80GHz carriers are ASK modulated by two independent PRBS's, simultaneously. These signals are multiplexed at the TX diplexer then transmitted through: a 25mm-long coplanar strip (CPS), 120mm-long plastic waveguide (PWG), or wirelessly over a 5mm air gap in free space. The CPS consists of two $250\mu\text{m}$ -wide copper lines separated by a $75\mu\text{m}$ gap with a 0.8mm dielectric on the top. The plastic waveguide has a cross-section of $1\times 2\text{mm}^2$ and is made of polystyrene. The developed chips are flip-chip mounted to a CPS or wire-bonded to couplers of a PWG or antennas. Transmitted signals are separated from each other at the RX de-diplexer and assessed using an oscilloscope or a BER tester. Measured eye diagrams and BER dependences on data rate are shown in Fig. 19.5.6. The transmitted data is synchronous and each channel shares the data rate evenly. Demonstrated versatile interconnects achieved $BER < 10^{-12}$ at data rates of 28Gb/s (limited by evaluation equipment for synchronous data) over a 25mm CPS. The data rates of 26Gb/s over a 120mm PWG and 20Gb/s over 5mm free space are also achieved, which are the highest reported results for their respective transmission medium [2-3]. Additionally data rate over 25mm CPS is measured with asynchronous PRBS's. This demonstration achieves $BER < 10^{-12}$ at data rates of 29.6Gb/s (18.6Gb/s in 57GHz + 11.0Gb/s in 80GHz). The crosstalk between two channels are estimated by calculation of cross-correlation between a baseband output waveform and the PRBS pattern. The crosstalk is -30dB in 57GHz data channel whose interference is from 80GHz data channel.

The demonstrated versatile multi-modality serial data link chips are fabricated in 40nm low-power logic CMOS technology. The micrograph of TX and RX chips are shown in Fig. 19.5.7. The active footprints including diplexer/de-diplexer are 0.16mm^2 and 0.26mm^2 for TX and RX chips, respectively.

References:

- [1] M. Chen, et al., "A 40Gb/s TX and RX Chip Set in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 146-147, Feb. 2011.
- [2] S. Fukuda, et al., "A 12.5+12.5Gb/s Full-Duplex Plastic Waveguide Interconnect," *ISSCC Dig. Tech. Papers*, pp. 150-151, Feb. 2011.
- [3] T. Takeya, et al., "A 12Gb/s Non-Contact Interface with Coupled Transmission Lines," *ISSCC Dig. Tech. Papers*, pp. 492-493, Feb. 2011.
- [4] John G. Proakis, *Digital Communications*, WCB/McGraw-Hill, 1995.
- [5] K. Kawasaki, et al., "A Millimeter-Wave Intra-Connect Solution," *ISSCC Dig. Tech. Papers*, pp. 414-415, Feb. 2010.
- [6] H. Hashemi and A. Hajimiri, "Concurrent Dual-Band CMOS Low Noise Amplifiers and Receiver Architectures," *Symp. VLSI Circuits*, pp.247-250, Jun. 2001.

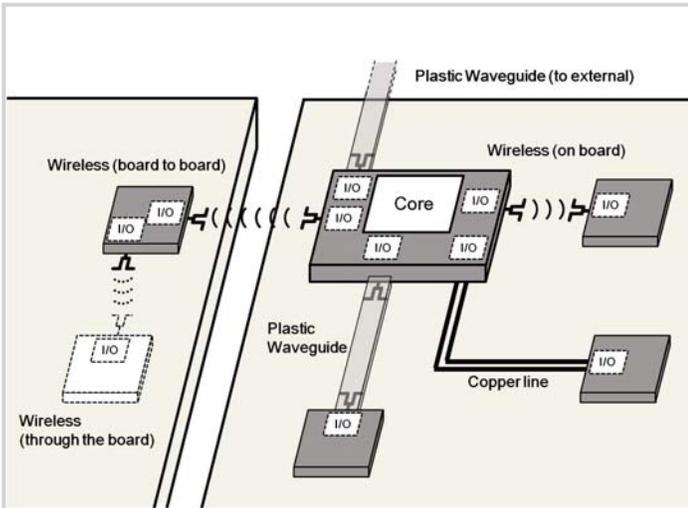


Figure 19.5.1: An application image of versatile multi-modality serial links.

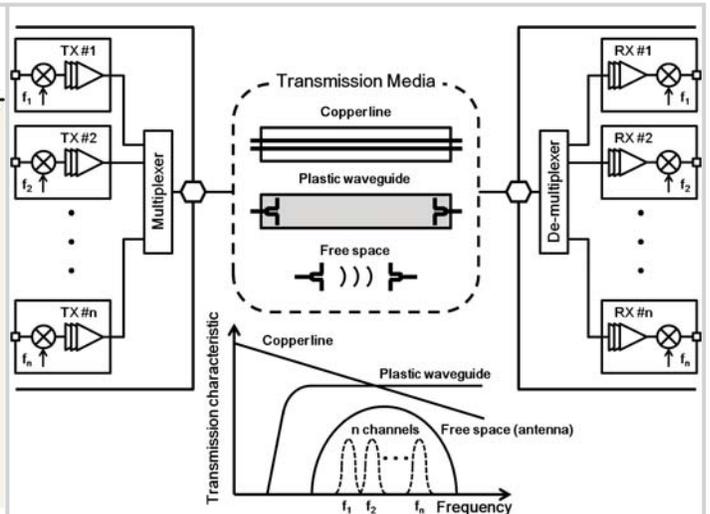


Figure 19.5.2: A frequency multiplexing system supporting three types of transmission media.

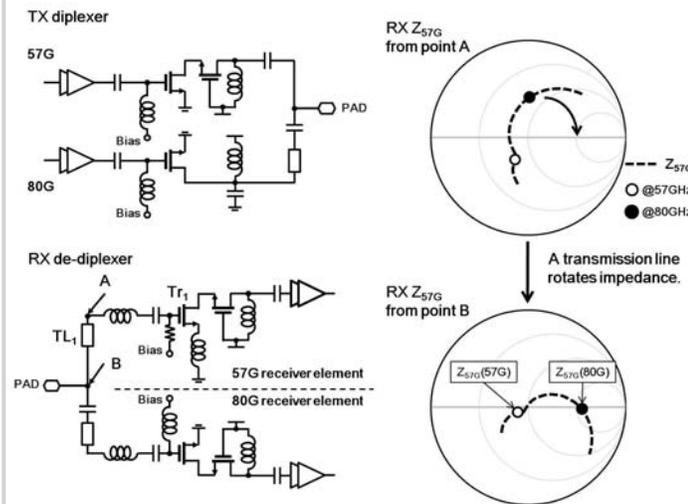


Figure 19.5.3: Schematics and impedance transformation of de-diplexer (simulation).

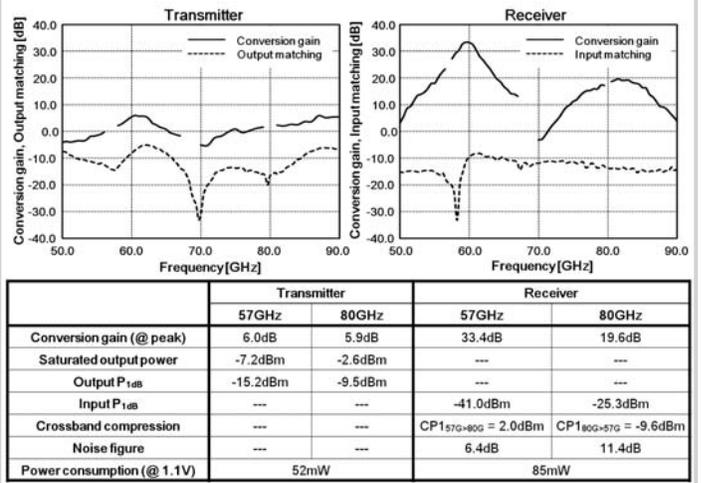


Figure 19.5.4: Measured performances of TX and RX.

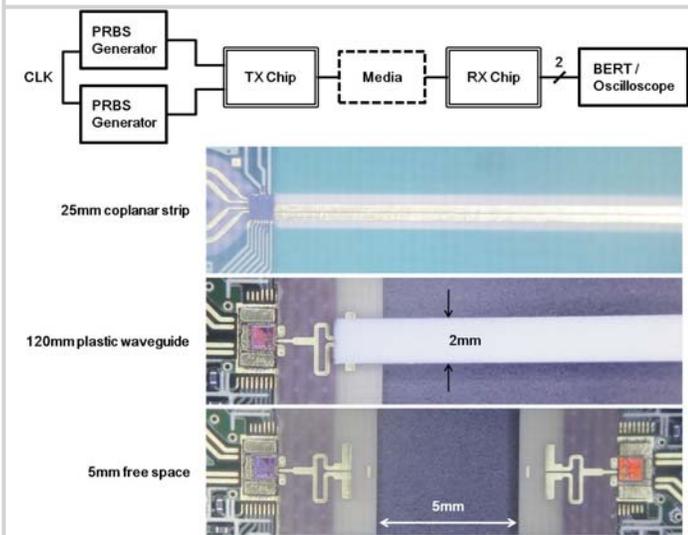


Figure 19.5.5: Measurement setup and photos of demonstrated transmission media.

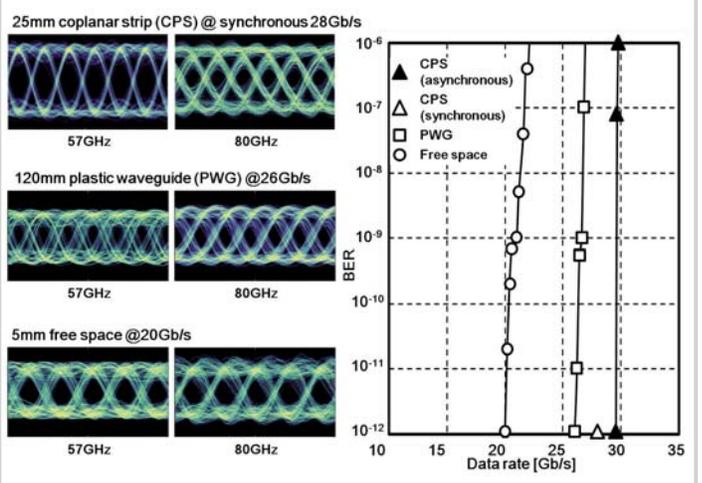


Figure 19.5.6: Measured eye diagrams and BER dependences on data rate for three transmission media.

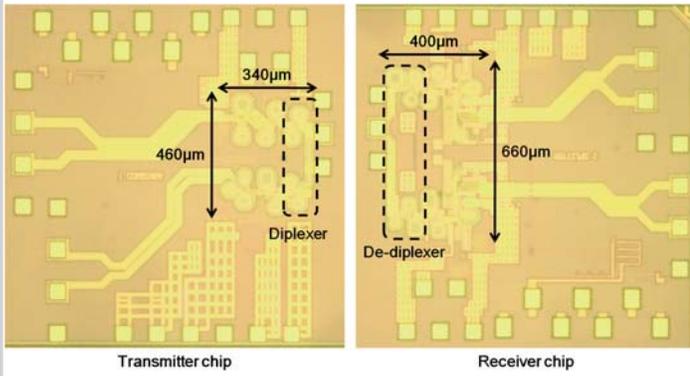


Figure 19.5.7: Die Micrographs.