Crosstalk-Induced Jitter Equalization

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***Abstract*-A novel jitter equalization circuit is presented that addresses crosstalk-induced jitter in high-speed communication links. A simplified model of electromagnetic coupling demonstrates the generation of crosstalk-induced jitter. This model suggests an equalizer that compensates for the data-induced electromagnetic coupling between adjacent links. Additionally, a data-dependent jitter equalizer that provides separate adjustments of rising and falling edge deviations is presented. The circuits are implemented using 130nm MOSFETs and operate at 5-10Gb/s. The results demonstrate reduced deterministic jitter and lower bit-error rate. At 10Gb/s, the crosstalk-induced jitter equalizer opens the eye at BER of 10^{-12} from 17ps to 45ps.**

I. Introduction

Signal integrity issues such as timing jitter are at the forefront of high-speed digital design. Keeping pace with the demand for aggregate data rates compels circuit designers to develop ever faster transceivers. Consequently, data rates are surpassing the bandwidth of transmission lines on legacy backplanes and, therefore, high-speed signals require appropriate compensation. Noise considerations dictate the choice of equalization technique.

To combat high-frequency attenuation, amplitude equalization can be introduced in the transmitter (pre-emphasis) or receiver (post-emphasis). Equalizer implementation is straightforward at the receiver, but high-frequency attenuation requires amplification of the signal and, therefore, the noise, limiting the signal-to-noise (SNR) [1]. Pre-emphasis compensates the signal prior to the addition of noise and is superior for compensating high-frequency attenuation. This approach, however, suffers drawbacks in environments with several unshielded serial data links. For instance, links in high-speed backplanes are situated in close proximity. Pre-emphasis of high-frequency signal components couples more electromagnetic energy into neighboring channels [2]. This coupling manifests as near-end crosstalk (NEXT) and far-end crosstalk (FEXT). Recent work has addressed crosstalk amplitude equalization issues between neighboring serial links [3]-[5]. However, no effort to date has been made to equalize the timing jitter resulting from crosstalk.

In this paper, the effect of crosstalk on data jitter is briefly summarized from [6]. The coupling between data transitions induces this jitter. Therefore, crosstalk-induced jitter (CIJ) is a type of bounded-uncorrelated jitter (BUJ), which is a subset of deterministic jitter (DJ) [7]. DJ reduces the horizontal opening of the data eye, degrading the bit error rate (BER). Serial links in backplanes demand low BER and jitter can ultimately limit the BER even after ISI is minimized. Reducing DJ is important to designing robust links with low BER.

We present general equalizer implementations for reducing the DJ impact of CIJ and data-dependent jitter (DDJ). The CIJ equalizer determines the electromagnetic modes of transitions and adjusts the delay of each transition. A DDJ equalizer with independent control of rising and falling edges reduces the total DJ. As these equalizers rely on dynamic adjustment of the transition time of the data signal, they do not suffer from the same SNR penalty as amplitude equalization. Finally, the performance of these jitter equalizers is presented in terms of eye opening and BER improvement.

II. Crosstalk-Induced Jitter

Crosstalk results from the interaction of electromagnetic fields generated by different data signals as shown in Fig. 1. In this figure, several high-speed differential serial links operate on the same substrate. While the coupling mechanism depends on the implementation, capacitive coupling is a useful approximation for high-impedance lines and provides insights into the generation of crosstalk-induced jitter both in backplanes and integrated circuits [9][10]. This approach can be generalized for crosstalk resulting from inductive and capacitive coupling [11]. Between the differential lines, a virtual ground exists since the transitions always maintain odd symmetry. Hence, the CIJ is dominated by the effect of one adjacent data signal.

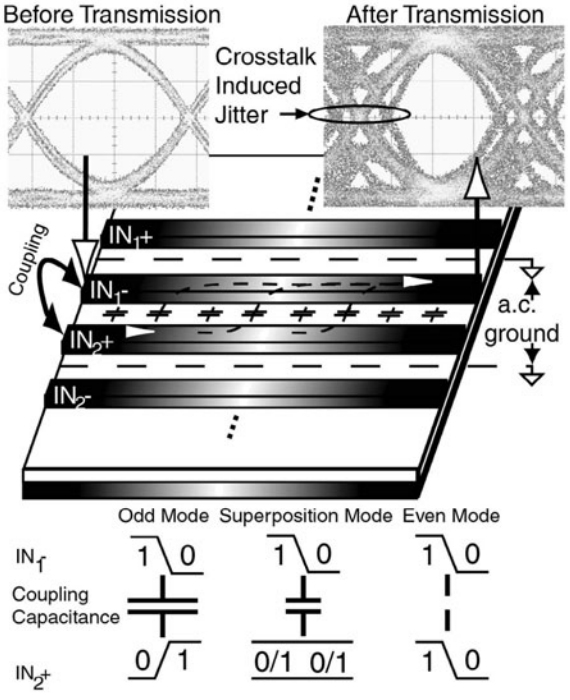

Fig. 1. The crosstalk jitter generated in the data eye due to the influence of a neighboring signal. Three possible modes can occur between transitions on neighboring lines.

Notably, the jitter on IN_1+ and IN_1- is generated by different neighbors. For simplicity, we study coupling between IN_1- and IN_2+. Coupling allows the adjacent signal to leak onto the transmission line according to the adjacent data sequence. Three transition combinations can occur as illustrated at the bottom of Fig. 1: odd, even, and superposition modes. Each modes is associated with a different coupling capacitance.

Typically, neighboring data transitions occur concurrently because the transmitters share a common clock. If we label IN_1- the victim signal and IN_2+ the aggressor signal, these signals can be represented as

$$r_1(t) = \sum_{n=-\infty}^{0} a_n g(t-nT) \quad \& \quad r_2(t) = \sum_{n=-\infty}^{0} b_n g(t-nT), \quad (1)$$

where a_n and b_n are independent data sequences and *g(t)* is the pulse response of the channel, which is assumed to be identical on both lines. The derivation in [6] calculates the arrival time, t_c, of the victim signal at the decision threshold, $v_{th} = r_1(t_c)$, when the aggressor signal is present. The CIJ is approximately

$$t_{c,\,CIJ} \approx -\tau_c \frac{(b_0 - b_{-1})}{(a_0 - a_{-1})}, \quad (2)$$

where τ_c is the time constant of the coupling capacitance and the line impedance. The denominator represents the transition in the victim data and the numerator represents the transition in the aggressor data. Note that (2) is only valid when a transition occurs on the victim data, *i.e.* $a_0 \neq a_{-1}$. Additionally, note that the shape of *g(t)* is not apparent in (2).

Based on the statistics of uncoded binary data, the coupling spreads the transition time of the victim data in (2) (and, symmetrically, the aggressor data) between three discrete values as shown in the eye in Fig. 1. The probability density function is

$$pdf_{CIJ}(t_c) = \frac{1}{4}\delta(t_c + \tau_c) + \frac{1}{2}\delta(t_c) + \frac{1}{4}\delta(t_c - \tau_c). \quad (3)$$

The middle, unaltered data transitions are twice as frequent because transitions with superposition mode occur twice as often as either the odd or even modes. This pdf describes the jitter and BER resulting from the influence of crosstalk.[1]

III. Crosstalk-Induced Jitter Equalization

The analysis of crosstalk-induced BUJ describes discrete transition deviations that occur for data sequences on neighboring channels. The separation of these peaks is related to the strength of the coupling between the two lines.

A general analog scheme for a CIJ equalizer is presented in Fig. 2. A symbol period time delay, *T*, is used to capture the data values before and after the transition. The summing device computes the difference between these data values to produce a three level signal corresponding to whether the current transition is a rising or falling edge. This result is multiplied by the result of the neighboring line to resolve the transition mode. The resulting tri-state signal indicates the electromagnetic mode of the transitions. For example, if both the victim and aggressor data lines have a rising (or falling) edge, the multiplication results in one, indicating the even mode. The tri-state value associated with the detection of this mode is weighted by an appropriate crosstalk equalization coefficient, which adjusts the time delay of the transition. This shifts timing deviations that occur in (3) to a consistent transition edge (i.e. the central transition). Notably, this adjustment can be implemented in either the transmitter as a pre-emphasis technique or the receiver before detection of the signal value. Additionally, the scheme in Fig. 3 can be expanded additional adjacent channels and include the effect of several neighbors.

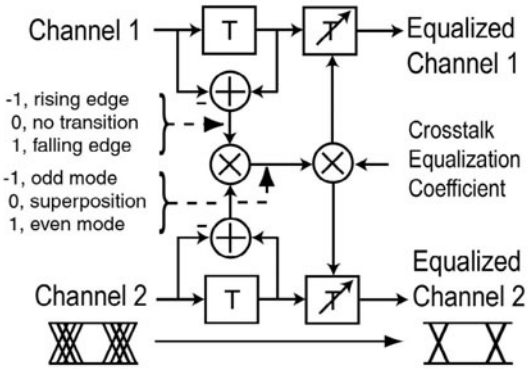

Fig. 2. Schematic of a two-channel crosstalk-induced jitter cancellation.

IV. Data-Dependent Jitter Equalization

The analysis presented in [8] describes the generation of DDJ in high-speed digital communications. Bandwidth-limitations and reflections result in data-dependent timing deviations. Often non-ideal offsets and device asymmetries create different transition rates for rising and falling edges and lead to duty-cycle distortion as well as DDJ that changes between the rising and falling edges. A low-power DDJ equalizer that can individually compensate the influence of duty-cycle variations is introduced.

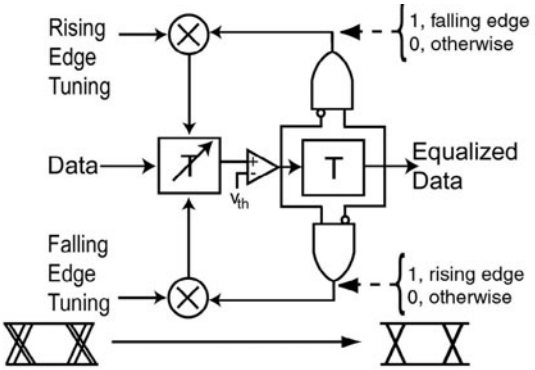

Fig. 3. Schematic for DDJ equalizer with independent rising and falling edge jitter.

1. Interestingly, the derivation of (2) does not assume a particular signalling scheme. A similar calculation of (3) for 4-PAM demonstrates additional crosstalk jitter due to the various combinations of transitions.

The detection of a prior rising or falling edges provides for compensation of the consecutive falling and rising edges, respectively. This scheme is shown in Fig. 3 and generalizes the circuit in [8]. The illustration demonstrates how an AND gate detects either a rising or falling edge after the data value is decided. Parallel adjustments are provided and combined in a variable time delay element.

V. Circuit Implementations

The circuit is implemented with 130nm MOSFETs. A chip microphotograph is provided in Fig. 4. The chip area measures 1mm x 1mm The actual area of the CIJ equalizer is 140µm x 100µm and the DDJ equalizer is 130µm x 80µm.

The circuit implementation consists of high-speed current-mode logic (CML) XOR and AND gates to detect transitions and compare the symmetry at 10Gb/s. While analog implementations of the circuits in Fig. 2 and Fig. 3 are possible, this logic gate approach is more robust to process variations and is sufficient for a proof-of-concept of the jitter equalizers.

For the CIJ equalizer, the gates generate logical values when the even or odd modes occur and are multiplied by a coefficient to adjust a variable time delay. For the DDJ equalizer, the CML gates generate logical values when the rising or falling edges occur and this logical value is weighted to adjusts the variable time delay.

The time delay elements are cross-coupled differential pairs that can adjust the delay quickly to satisfy the critical path timing for the equalizer circuits. Additionally, the time delays are tuned for the appropriate tap delay and bit rate.

The entire two channel circuit consumes 330mA from a 2V supply. From simulation, the crosstalk equalizer consumes 40mA and the DDJ equalizer draws 20mA per channel. The remaining current consumption supports the output buffering.

VI. Results

The chip is wirebonded to Rogers 5880 duroid with a brass mount. The CIJ and DDJ equalizers are tested separately.

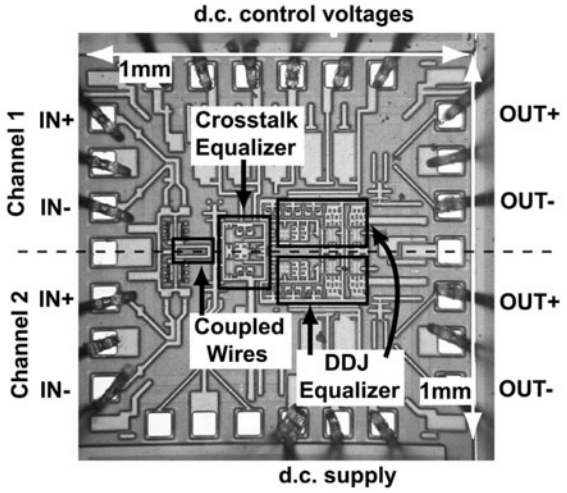

Fig. 4. Chip microphotograph of the XTC and DDJ equalizers.

To generate uncorrelated data sequences at 5-10 Gb/s, differential outputs of an Anritsu MP1763C pulse pattern generator (PPG) are delayed with respect to one another by 10 bits.[2] Two separate coupling paths are tested. For 10Gb/s testing, the two data paths are coupled through on-chip transmission lines with capacitive coupling of 3.35fF. For testing at 5Gb/s, the crosstalk was introduced through coupled microstrip lines on FR-4 board similar to [8] with capactive coupling of 400fF.

The first measurement collects jitter statistics around a threshold voltage from the data eye with and without CIJ equalization. The jitter standard deviation (J_σ)and peak-to-peak jitter (J_{pp}) reflect the BER performance. Histograms of the differential data eye are created from three thousand data points within a 400µV bounding box. In Fig. 5, the data eye demonstrates that J_σ reduces from 8.65ps to 6.31ps at 10Gb/s. J_{pp} reduces from 48.89ps to 34.22ps. Similar improvements are noted at 5Gb/s and recorded in Table I.

The second measurement sketches the bathtub curve for the eye opening with the Anritsu MP1764C error detector. The notable improvement of J_σ and J_{pp} is reflected by the larger eye opening in Fig. 6 after compensation. The BER measurement is degraded by the single-ended receiver in the MP1764C, which is sensitive to common-mode noise. A summary of these results at 5 and 10Gb/s is also shown in Table I. The BER curve measured before compensation shows an opening of 17ps at BER of 10^{-12} and 45ps after compensation. This indicates the substantial eye improvement possible due to the CIJ equalizer.

TABLE I.
Improvement of Crosstalk-Induced Jitter at 5 and 10Gb/s.

	J_σ	J_{pp}	BER = 10^{-12}
Before Equalization at 10Gb/s	8.65ps	48.89ps	17ps
After Equalization at 10Gb/s	6.31ps	34.22ps	45ps
Before Equalization at 5Gb/s	17ps	86ps	102ps
After Equalization at 5Gb/s	7.41ps	41.33ps	143ps

The DDJ equalizer is tested on a single channel of the circuit in Fig. 4. DDJ is introduced to the serial data through a buffer

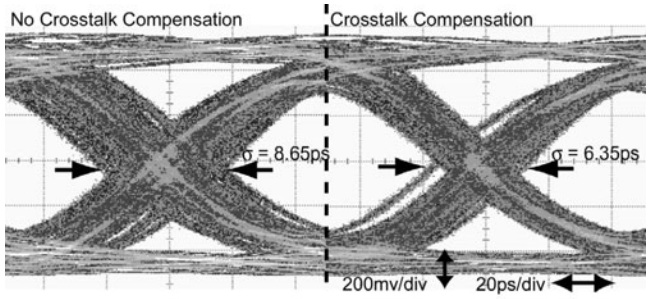

Fig. 5. Data eyes at 10Gb/s before and after equalization.

2. A 2^7-1 pseudo-random bit sequence is an example of a maximal length sequence, which has low (~zero) autocorrelation after one bit [1].

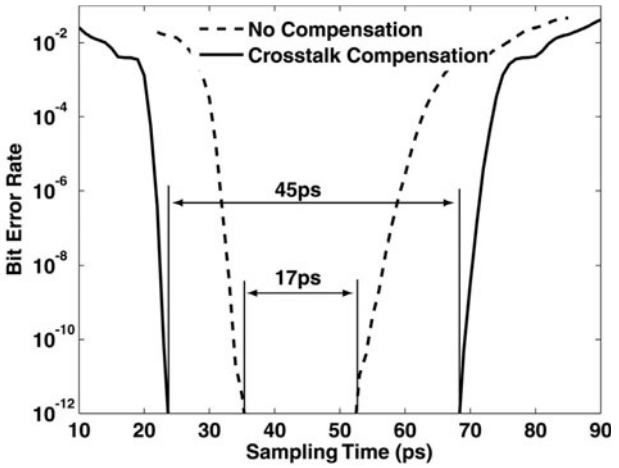

Fig. 6. Bathtub curve resulting before and after equalization.

loaded with large, trimmable capacitors. This testing solution is designed to ease the burden of using external 10GHz filters to demonstrate the performance improvement. As before, jitter statistics for the serial data are recorded from the differential data eye. The measurement results for the DDJ equalizer are shown in Fig. 7 and Table II at 10Gb/s. Four eyes are demonstrated in Fig. 7 to show the independent equalization of the rising and falling edges. The individual compensation of the rising and falling edges reduced J_σ by similar amounts. The compensation of the rising edge was slightly better since the rising edge seemed to suffer from more DJ than the falling edge. Consequently, J_{pp} was clearly improved entirely by rising edge equalization.

TABLE II.
IMPROVEMENT OF DATA-DEPENDENT JITTER AT 10GB/S

	J_σ	J_{pp}	BER = 10^{-12}
Before Equalization at 10Gb/s	9.35ps	49.78ps	30ps
After Falling Edge Equalization at 10Gb/s	7.37ps	40.9ps	41ps
After Rising Edge Equalization at 10Gb/s	7.14ps	34.22ps	43ps
After Rising and Falling Edge Equalization at 10Gb/s	4.6ps	34.7ps	52ps

Additionally, the BER bathtub curve is calculated directly through an error detector to verify the improvement of DDJ equalization. The BER demonstrates that equalizing the individual edges resulted in similar eye-opening. The equalization of both edges increased the eye opening that achieved BER of 10^{-12} from 30ps to 52ps.

CONCLUSION

Crosstalk-induced and data-dependent jitter equalizers are presented that compensate for deterministic jitter in high-speed serial communications links. The circuit implementations are simple and consume little power. The results demonstrate the reduction of crosstalk induced jitter and data-dependent jitter and, consequently, the overall BER of the serial link is significantly improved.

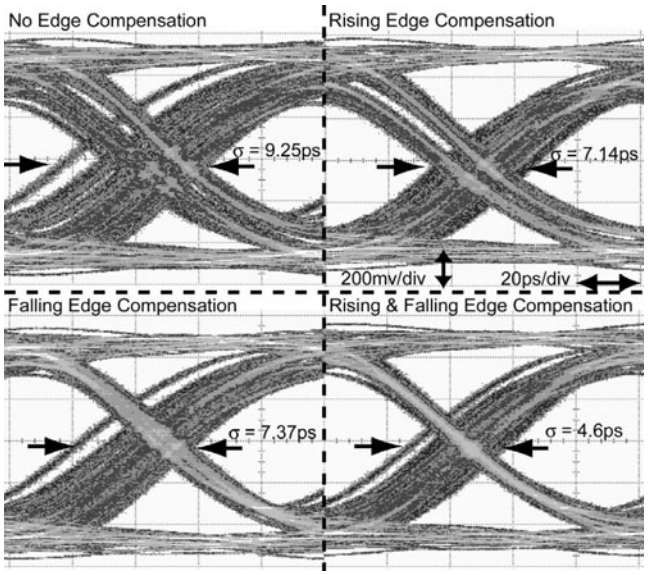

Fig. 7. Eye diagrams for DDJ compensation of different edges at 10Gb/s.

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REFERENCES

[1] J. Proakis, *Digital Communications*, NY, NY: McGraw Hill, 2001.
[2] J. Stonick *et al.,* "An Adaptive PAM-4 5-Gb/s Backplane Transceiver in 0.25um CMOS," *IEEE J. Solid-State Circuits,* vol. 38, pp. 436-443, Mar. 2003.
[3] J. Zerbe *et al.,* "A 2Gb/s/pin 4-PAM Parallel Bus Interface with Transmit Crosstalk Cancellation, Equalization, and Integrating Receivers." *IEEE Int. Solid-State Circuits Conference Digest.* Feb. 5-7 2001, pp. 66-67.
[4] C. Pelard *et al.,* "Realization of Multigigabit Channel Equalization and Crosstalk Cancellation Integrated Circuits." *IEEE J. Solid-State Circuits.* vol. 39, pp.1659-1669, Oct. 2004.
[5] Y. Hur *et al.*, "Equalization and Near-End Crosstalk (NEXT) Noise Cancellation for 20Gb/s 4-PAM Backplane Serial I/O Interconnects." *IEEE T. Microwave Theory & Techniques*, vol. 53, pp. 246-255, Jan. 2005.
[6] J. Buckwalter, B. Analui, and A. Hajimiri, "Data-Dependent Jitter and Crosstalk-Induced Bounded Uncorrelated Jitter in Copper Interconnects," *IEEE Int. Microwave Symposium Digest*, June 6-11 2004, pp. 1627-1630.
[7] International Committee for Information Technology Standardization (INCITS), Fibre Channel - Methodologies for Jitter and Signal Quality Specification- MJSQ, Technical Report REV 10.0, March 10, 2003.
[8] J. Buckwalter and A. Hajimiri, "A 10Gb/s Data-Dependent Jitter Equalizer," *Proc. IEEE Custom Integrated Circuit Conf.*, pp. 39-42, Oct. 2004.
[9] R. Ho, K. Mai, M. Horowitz. "The Future of Wires," *Proc. of the IEEE*, vol. 84, no. 9, pp. 490-504, April 2001.
[10] D. Pozar, *Microwave Engineering,* Reading, MA: Addison-Wesley, 1990.
[11] W. Dally and J. Poulton, *Digital Systems Engineering,* Cambridge, UK: Cambridge University Press, 1998.