A Breakdown Voltage Doubler for High Voltage Swing Drivers

Sam Mandegaran and Ali Hajimiri

Department of Electrical Engineering
California Institute of Technology, Pasadena, CA 91125, USA

Abstract

A novel breakdown voltage (BV) doubler is introduced that makes it possible to generate high output voltage swings using transistors with low breakdown voltages. The timing analysis of the stage is used to optimize its dynamic response. A 10Gb/s optical modulator driver with a differential output voltage swing of 8V on a 50Ω load was implemented in a SiGe BiCMOS process. It uses the BV-doubler topology to achieve output swings twice the collector-emitter breakdown voltage without stressing any single transistor.

Introduction

Recently, there has been a great deal of interest in silicon-based high-speed integrated circuits for optical fiber communications due to their cost advantage and integration prospects. While most of the building blocks in a fiber optics transceiver have been implemented and demonstrated in silicon at 10Gb/s and above, the optical modulator electrical driver has been primarily done in compound semiconductors. This is mainly due to breakdown limitations of silicon transistors and large required voltage swings of today's high-speed optical modulators. However, the process technology disparity between the driver and the rest of the transceiver results in additional cost and performance penalties. This paper introduces a new breakdown voltage (BV) doubler topology that overcomes the breakdown limitations of the SiGe transistors by design and enables high-speed broadband drivers with a large voltage swing in silicon.

Existing electro-absorption and Mach-Zehnder optical modulators require a large voltage swing to achieve a high extinction ratio, *i.e.*, to switch the light on and off effectively. Such a large voltage swing poses a challenge for silicon-based transistors (SiGe HBT or Si CMOS) whose breakdown voltages are constantly dropping with continuous scaling for higher speed. While there have been reports of driver circuits in SiGe for optical applications [1]-[3], all these circuits drop the entire voltage swing across single transistors and thus cannot exceed the collector-emitter breakdown voltages and are hence limited to a voltage swing of around 3V. This paper offers a novel BV doubler topology that can generate output voltage swings twice the transistor breakdown voltages, without exceeding the nominal operation conditions of the active devices.

Circuit Concept

A) Transistor Breakdown Voltages

There are several breakdown voltages that are often reported for bipolar junction transistors (BJT). The collector-emitter breakdown voltage, BV_{cer}, is the main limiting factor in the design of a high-voltage driver. This breakdown voltage is a function of the total base resistance, R_B, to the ac ground. The most commonly reported value is the collector-emitter breakdown voltage when the base is open, *i.e.*, $R_B = \infty$, often shown as BV_{ceo}. It is noteworthy that BV_{ceo} is the lower bound of the collector-emitter breakdown voltage of the transistor. This affects the design process, as the base is driven with a lower source impedance, this breakdown voltage will increase. For instance, in the process used to implement the driver in this paper, BV_{ceo} =1.8V compared to BV_{cer} >3.0V for R_B <100Ω. This property has been exploited in the designs of [1]-[4].

Reported high-speed drivers use some form of a current switch at the output stage. When a single active device withstands the entire output voltage swing [1]-[4], BV_{cer} sets the limit on the maximum output voltage.

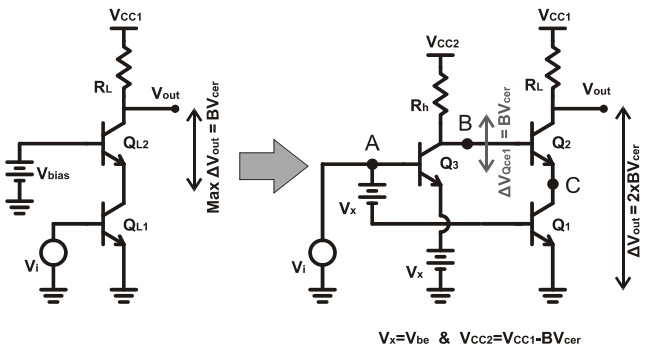

Figure 1: Evolution of the BV Doubler

B) Driven Cascode Topology (BV Doubler)

In principle, the output voltage swing can be broken down among several transistors in a cascode configuration to alleviate the breakdown voltage limitations of the transistors. However, in a standard cascode configuration, the base of the upper transistor is biased at a constant voltage, as shown in

Fig. 1a. Thus, its emitter voltage will remain relatively constant due to the logarithmic dependence of V_{BE} on I_C. For a fixed base voltage, most of the output voltage swing will still appear across the upper transistor, rendering this approach ineffective.

On the other hand, if the base of the upper transistor is also moved with the same polarity as the output, the emitter of the upper transistor will follow it at a similar rate since the upper transistor behaves as an emitter-follower for the base drive, as shown in Fig 1b. This will effectively divide the voltage swing between the top (Q_2) and bottom (Q_1) transistors in both on and off states, as well as during the transitions. Ideally, we would like to divide the output swing equally between the two transistors. This, in turn, implies that the base of Q_2 should move with half the voltage swing of its collector (V_{out}) for equal voltage division between the upper and lower transistors.

In our design, we set a conservative maximum V_{CE} limit of 2.5V and a minimum of 0.5V to avoid excessive base charge storage and its associated speed degradation. Hence, each transistor experiences a voltage swing of approximately 2V leading to a single-ended output voltage swing of 4V. The 2V limit on V_{CE} is much lower than that used in earlier works reported in [1]-[4] resulting in a more reliable design in our case.

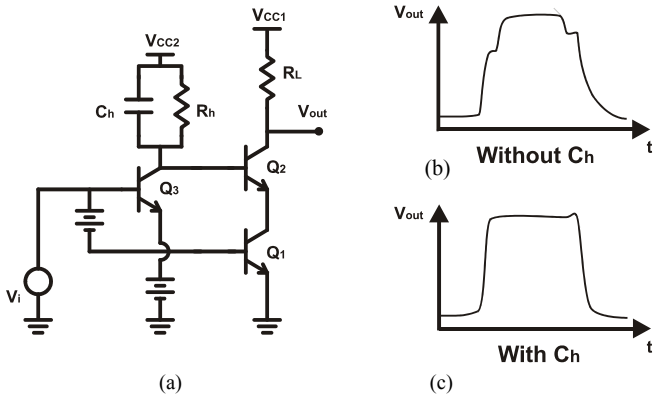

Figure 2: Single-ended equivalent of the output stage of the driver

C) Timing

While the basic concept introduced in Fig 1b is valid, the relative timing of the two signal paths plays an important role in the integrity of the output waveform, as shown in Fig. 2. The main path to output via Q_1 and Q_2 is slightly slower than auxiliary path through Q_3 and Q_2, as will be discussed in the next section. If no effort is made to compensate this timing mismatch, each path will induce changes on the output at different times, resulting in a distorted output voltage, as shown in Fig. 2b. This effect can be compensated by slowing the auxiliary path via introduction of an additional timing adjustment capacitor, C_h, on the collector of Q_3. By choosing the right value of C_h, the delays of the two paths can be equalized, resulting in a nice waveform at the output, as shown in Fig. 2c.

D) Differential Implementation

The actual circuit is implemented as a fully differential stage, as depicted in Fig. 3 and 4. Several emitter followers precede the main driver stage to lower the source impedances and provide the appropriate dc levels to both main and auxiliary paths. Additional resistors and diodes are used in the collectors of these emitter followers to avoid excessive V_{ce} and potential breakdown problems. The output driver consists of a main differential cascode path and an auxiliary differential path with timing adjustment capacitors C_h on each side. The resistor R_D lowers the common-mode dc level seen by the auxiliary path while it has no effect on the differential signal as node **D** is virtual ground. Capacitor C_D is used to lower the common-mode impedance on node **D** to suppress even mode variations.

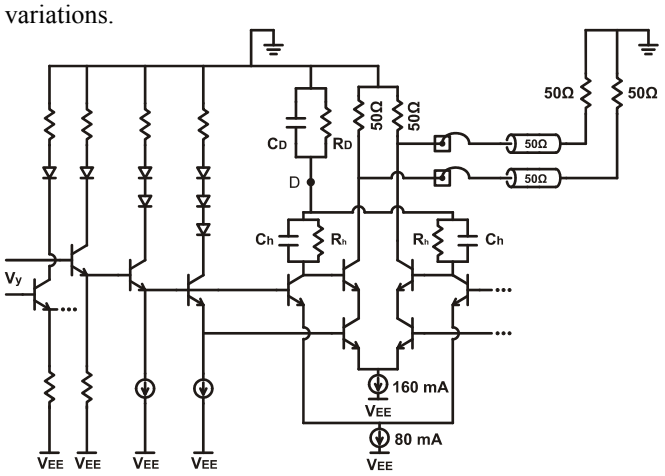

Figure 3: Output stage of the driver

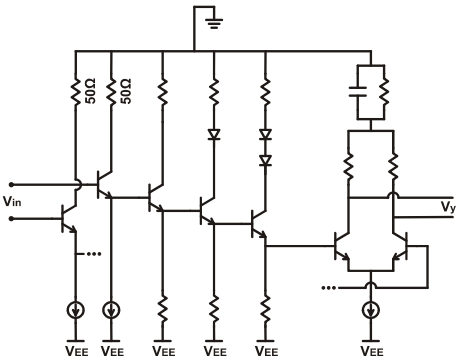

Figure 4: Pre-driver

Analysis

In this section, we perform a small signal analysis of the output stage dynamics. Fig. 5 is a simplified half-circuit small-signal equivalent of the output stage. The forward signal path consists of two parallel paths with different dynamics. The main path consists of an emitter follower buffer whose dynamics is non-dominant, followed by the common-emitter transistor, Q_1, and the common-base

transistor, Q_2, driving the output node. It has an inverting small-signal dc gain of:

$$A_1 = -g_{m1}R_L \tag{1}$$

where g_{m1} is the transconductance of Q_1 and R_L is the output load resistance. The non-inverting small-signal dc gain of the auxiliary path is given by:

$$A_2 = g_{m3}R_h \cdot \frac{g_{m2}R_L}{1+g_{m2}r_{o1}} \cong \frac{g_{m3}R_hR_L}{r_{o1}} \tag{2}$$

where g_{m3} and g_{m2} are the transconductances of Q_3 and Q_2, respectively, and r_{o1} is the output resistance of Q_1. This path consists of a common emitter stage with a gain of $-g_{m3}\cdot R_h$ and another highly degenerate common-emitter with a gain of $-R_L/r_{o1}$. The dc gain from the input to the collector of Q_3, $-g_{m3}\cdot R_h$, is approximately one-half of A_1 to guarantee equal division of the voltage swing at the output, as discussed in the previous section.

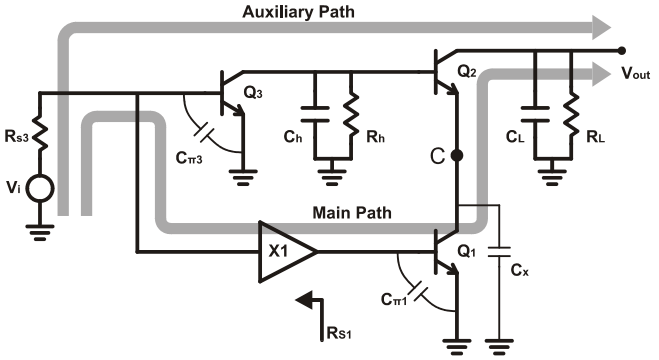

Figure 5: Half-circuit small-signal equivalent of the output stage

The dynamics of the main path is dominated by the pole at the input of Q_1, $p_{\pi 1}$, approximately given by:

$$p_{\pi 1} \cong \frac{-1}{C_{\pi 1}[(R_{S1}+r_{b1})\|r_{\pi 1}]} \approx \frac{-1}{C_{\pi 1}(R_{S1}+r_{b1})} \tag{3}$$

where R_{s1} is the output resistance of the buffer driving the base, and r_{b1} is the physical base resistance of Q_1. Since $r_{\pi 1}$ is much greater than $R_{s1} + r_{b1}$, it has a small effect on the pole frequency and it can be ignored. The auxiliary path has a slightly more complex dynamics. There is a pole at the input of Q_3, $p_{\pi 3}$, which is given by:

$$p_{\pi 3} \cong \frac{-1}{C_{\pi 3}[(R_{S3}+r_{b3})\|r_{\pi 3}]} \approx \frac{-1}{C_{\pi 3}(R_{S3}+r_{b3})} \tag{4}$$

where R_{s3} is the source resistance of the emitter follower driving Q_3 and r_{b3} is its physical base resistance.[1] The timing capacitance, C_h, introduces another pole, p_h, which is:

$$p_h \cong \frac{-1}{R_hC_h} \tag{5}$$

[1] $C_{\pi 3}$ primarily affects the auxiliary path since r_{b3} is greater than R_{S3}.

Additionally, the total parasitic capacitance on node **C**, C_x, generates a non-dominant pole around the transistor's cut-off frequency, ω_T, and a left half plane (LHP) zero at:

$$z_x \cong \frac{-1}{r_{o1}C_x} \tag{6}$$

Hence, the transfer function for the main path can be described as:

$$H_1(s) = \frac{A_1}{1+s/p_{\pi 1}} \tag{7}$$

Similarly, the auxiliary path's transfer function is modeled as:

$$H_2(s) = A_2\frac{(1+s/z_x)}{(1+s/p_{\pi 3})(1+s/p_h)} \tag{8}$$

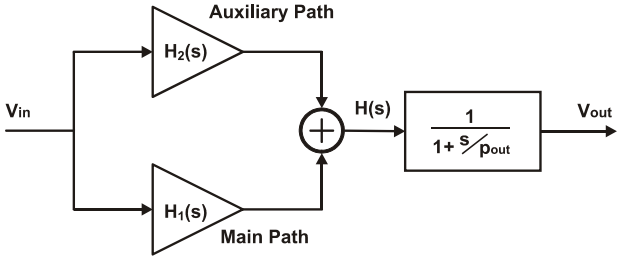

Figure 6: The equivalent system for the driver

The complete system can be modeled as the parallel combination of these two paths followed by the non-dominant pole at the output, as shown in Fig. 6. Ignoring the non-dominant output pole, the equivalent transfer function of the resultant system is:

$$H(s) = H_1(s) + H_2(s) = A\frac{(1+s/z_1)(1+s/z_2)}{(1+s/p_{\pi 1})(1+s/p_{\pi 3})(1+s/p_h)} \tag{9}$$

where $A = A_1 + A_2$, and z_1 and z_2 are new real zeros. It is noteworthy that the transfer function of the compound system, $H(s)$, has the same poles as $H_1(s)$ and $H_2(s)$, but a different pair of zeros, whose values depend on C_h.

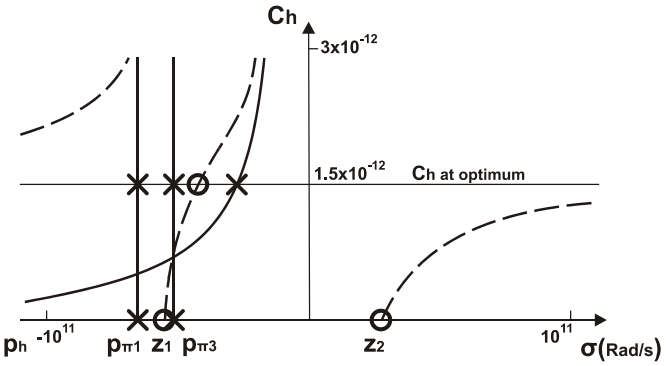

Figure 7: Location of poles and zeros as a function of *Ch*

Fig. 7 shows how the real poles and zeros of the overall system move as a function of C_h (y-axis). As can be seen, initially we have a right half plane (RHP) zero, z_2, whose

phase contribution can degrade the waveform. By increasing C_h, this zero is quickly pushed to higher frequencies and eventually becomes a non-dominant LHP zero. On the other hand, p_h, is initially completely non-dominant but quickly moves in to become dominant. Fortunately, z_1 moves close to p_h and hence partially compensates p_h and $p_{\pi 3}$ at the optimum point.

Experimental Results

The driver was fabricated in IBM's 0.18µm SiGe BiCMOS process. For this design, only SiGe HBTs with an f_T of 120GHz were used. The die micrograph is shown in Fig. 8.

A) Setup

The chip could not be directly mounted on a ground plane because the silicon substrate had to be at a negative supply relative to ground. Thus, it was placed on a cheap CVD thick-film diamond (grown by SP3 Diamond Cutting Tools) for good heat dissipation and electrical insulation. The chip and the crystal were then placed on a piece of brass. All three were connected using conductive silver epoxy (Epoxy Tech. H20E). A PCB (Rogers Corp. RT5880) was attached to the brass to carry the signals to and from the chip. All the pads were wire bonded including the signal input and output pads. Input and output wire bonds were directly connected to 50Ω transmission lines leading to SMA connectors. Before testing, the chip and the wire-bonds were covered with thermally conductive and electrically insulative epoxy (Epoxy Tech. H70E) to allow for better heat dissipation and protect the die. The input was differentially fed using a pulse pattern generator (Anritsu MP1763C). The output was connected in many different configurations for both electrical and optical testing. For electrical testing a 50GHz oscilloscope sampling head (Agilent 83484A) was used.

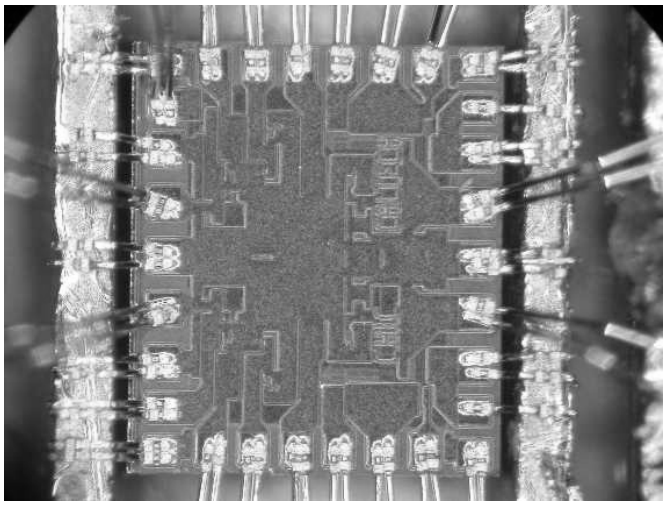

Figure 8: Die photo

B) Measurements

The measured differential output swing at 10Gb/s was between 7V to 8V depending on the power supply voltage. The eye diagram in Fig. 9 is an electrical eye diagram of the single-ended output of the driver with a 3.8V swing. For Fig. 9 the output signal was connected through a bias T and a 20dB attenuator to the oscilloscope. The power supply was -6.5V and the current drawn was 562mA. The input signal was differential 10Gb/s with 250mV swing on each input. The chip was tested for extended periods of time both optically and electrically, measuring the bit error rate (BER). No error was observed running the driver continuously for more than three days at 10Gb/s, setting an upper bound of 10^{-15} on the BER.

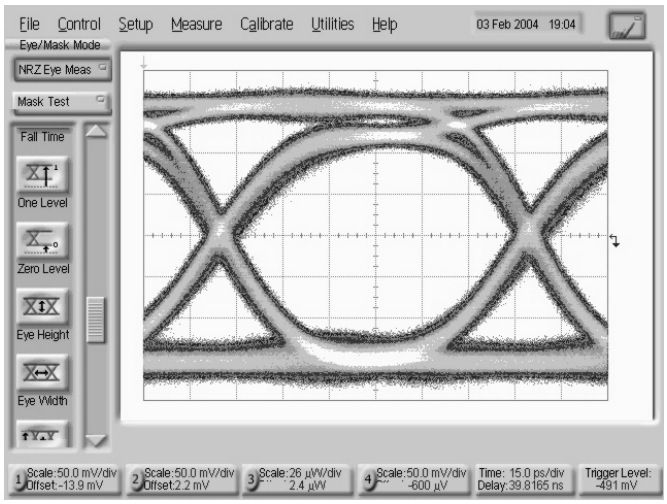

Figure 9: Electrical eye diagram of one ouput

Conclusion

We have shown a novel BV Doubler topology that can alleviate the low breakdown voltage of high-speed silicon devices for use in high voltage drivers. This topology divides the output swing equally on two transistors allowing an output voltage swing of $2BV_{cer}$ without exceeding BV_{cer} on any single transistor. This topology differs from the standard cascode by synchronously driving the base voltage of the upper transistor. The measured chip had a differential output swing of 8Vpp at 10Gb/s. A very conservative maximum value of V_{CE} was used in designing this circuit. As shown in [4] this process technology can sustain a V_{CE} swing as high as 3.2V, and therefore, using the same process technology and design, one can achieve a differential voltage swing up to 12.8V.

References

(1) H.-M. Rein, R Schmid, P. Weger T. Smith, T Herzog, and R. Lachner, "A Versatile Si-Bipolar Driver Circuit with High Output Voltage Swing for External and Direct Laser Modulation in 10 Gb/s Optical-Fiber Links," *IEEE J. Solid-State Circuits,* vol. 29, pp. 1014-1021, Sept. 1994.

(2) R. Schmid, T. F. Meister, M. Rest, and H.-M. Rein, "40Gbit/s EAM driver IC in SiGe bipolar technology," *Electronics Letters,* vol. 34, pp. 1095-1097, 28th, May 1998.

(3) R. Schmid, T. F. Meister, M. Rest, and H.-M. Rein, "SiGe Circuit with High Output Amplitude Operating up to 23 Gb/s," *IEEE J. Solid-State Circuits,* vol. 34, pp. 886-891, June 1999.

(4) D. J. Friedman *et al.*, "SiGe BiCMOS integrated circuits for high-speed serial communication links," *IBM J. Research & Development,* vol. 47, pp. 277-279, March/May 2003.