Dynamic Polarization Control

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Abstract—Dynamic polarization control (DPC) is the method of setting the polarization of the far-field electric field generated by a radiating antenna entirely electronically in order to maintain polarization matching with the receiving antenna regardless of its polarization or orientation in space. This work implements a fully integrated 2 × 1 phased array radiator in 32 nm CMOS SOI at 105.5 GHz with DPC. The system consists of a central locking oscillator that phase locks oscillators within the core of each antenna followed by three amplification stages with variable gain that drive the antennas. By controlling the amplitude and phase of two orthogonal polarized subparts of each multi-port antenna, various far-field polarizations can be realized. The array is capable of beam steering, controlling the polarization angle across the entire tuning range of 0° to 180° while maintaining axial ratios above 10 dB, and controlling the axial ratio from 2.4 dB (near circular) to 14 dB (linear) in various directions of radiation. It radiates a maximum EIRP of 7.8 dBm with a total radiated power of 0.9 mW. To the best of the authors’ knowledge, this work presents the first integrated radiator with dynamically controllable polarization.

Index Terms—Electromagnetic polarization, integrated microwave circuits, integrated radiators, mm-wave silicon RFICs, silicon phased array.

I. INTRODUCTION

ADVANCEMENTS in silicon CMOS integrated circuit (IC) technologies have provided devices capable of operating at mm-wave frequencies where the wavelengths are on the same order of magnitude as the IC dimensions. This has opened new design and application spaces for integrated mm-wave systems engineering while also providing new challenges as low frequency lumped models of devices and metals begin to fail [1]–[5]. One challenge associated with this mm-wave system engineering is generating RF power and coupling it to the outside world [6]–[8]. Traditional methods of power transfer such as wirebonding and flip-chip become increasingly lossy at mm-wave frequencies above 100 GHz, necessitating other power transfer methods [9], [10]. Integrating antennas on-chip and radiating directly from the IC becomes feasible when the carrier electromagnetic wavelengths are similar to the dimensions of the IC [11]–[20]. This increased level of integration can improve efficiencies and lower costs compared with solutions requiring external power transfer components.

One challenge in mobile wireless communication links is coupling loss due to polarization mismatch. Polarization mismatch is a phenomenon where additional coupling losses between the transmit and receive antennas occur in addition to the free-space propagation loss if the antennas are not of the same polarization and aligned in space. Electromagnetic polarization describes the parametric trajectory of the electric and magnetic field vectors of an electromagnetic plane wave as it propagates through space. Three examples of various transmit antennas and their associated far-field electric fields are depicted in Fig. 1. If the signal is being received by a horizontally polarized receive antenna, it will be polarization matched to the transmit antenna with horizontal linearly polarized and the power received at the port of the antenna will simply be the input power to the transmitter multiplied by the free space propagation loss. If the transmit antenna is rotated in space, the received signal will continue to degrade due to polarization mismatch to the point where very little signal is received when the antennas are completely mismatched with orthogonal polarizations. Theoretical 3 dB degradation in coupling due to polarization mismatch will also occur when one of the antennas is circularly polarized while the other is linearly polarized.

The polarization of the far-field electric field can be defined by its polarization axial ratio and polarization angle. The electric field, when plotted on a two-dimensional plane normal to the direction of propagation, produces an ellipse over one period. The polarization axial ratio is the ratio of the major to minor axes of the ellipse and determines how circular (low axial ratio) or how linear (high axial ratio) the polarization is. In order to orient the ellipse in space, the polarization angle can be defined as the angle between the major axis of the ellipse and a reference vector, which for the purposes of this paper will be taken as the horizontal X-axis. This means that the full range of axial ratios is from unity through infinity, and the full range of polarization angles is from 0° through 180°. Finally, the direction that the electric field travels around the ellipse will determine if the polarization is left-handed (clockwise when propagation is toward the observer) or right-handed (counter-clockwise when propagation is toward the observer).

If an electromagnetic radiator is capable of controlling the polarization angle and axial ratio over their full tuning range for right- and left-handed polarization in the far field, then it can produce any possible far-field polarization, and can produce a polarization match with a receiver regardless of its polarization or orientation in space as shown in Fig. 2 [20]. It is important to note that as the receive antenna rotates, both its polarization and directivity in the direction of the transmit antenna may change. While a transmit antenna with Dynamic Polarization Control (DPC) will be able to maintain polarization matching by changing its polarization, the coupling between the two an-
Fig. 1. Effects of polarization mismatch on coupling transmit/receive antenna pairs. Maximum coupling occurs for polarization matched antenna pairs (top), no coupling for completely mismatched pairs (middle) and partial coupling for partially mismatched pairs (bottom).

In this paper, we show a fully integrated 105.5 GHz 2x1 phased array radiator implemented in a 32 nm CMOS SOI process with dynamic polarization control capable of tuning polarization angle and axial ratio with effective isotropically radiated power of 7.8 dBm and 0.9 mW total radiated power. The remainder of the paper is organized as follows: the system implementation of DPC radiating array is presented in Section II, followed by the circuit design and simulation in Section III. Next, Section IV presents the design, analysis and simulation electronics due to the unpredictability of the orientation during usage.

Fig. 2. A radiator with Dynamic Polarization Control (DPC) can transmit any polarization angle and polarization axial ratio in order to maintain polarization matching with a receive antenna of any polarization or orientation in space.

tennas may change due to changes in the free space propagation loss due to the changes in directivity. In order to know what polarization to transmit to a mobile receive antenna, some information feedback from the receiver to the transmitter would be required for this implementation. While some work has been done on switchable polarization on printed circuit board (PCB) antennas [21], [22] where polarization can be switched between different modes, truly dynamic control of the polarization is desired where the polarization can be set to match any receiver polarization. This is particularly important in the case of portable communication systems based on integrated
of the antennas with polarization control used in this work. Measurements of the radiator that demonstrate DPC follow in Section V, with concluding remarks in Section VI.

II. SYSTEM ARCHITECTURE

In order to have full control of both dimensions of polarization, as well as the amplitude and phase of far-field electric field, a minimum of four degrees of freedom are required from the input ports. This is why a stationary single-port antenna in a linear, isotropic medium cannot perform DPC, and rather has a fixed polarization at a given frequency (for example, a dipole antenna is linearly polarized along the axis of the dipole, and a helical antenna is circularly polarized). For these single-port antennas at a given frequency, there are only two degrees of freedom at the input, namely its amplitude and phase, and adjusting these values will in turn adjust the amplitude and phase of the far-field electric field without changing its polarization.\footnote{Multiple single-port antennas with different polarizations can control the polarizations in the far field through the superposition of the individual antennas. However, in an integrated setting, it is difficult to create the feeds for these antennas while maintaining their isolation, and the additional area adds significantly to the cost of the IC.}

Additional degrees of freedom can be obtained by driving a single antenna from multiple ports. By independently controlling the amplitude and phase of the various ports, it is possible to generate the four degrees of freedom required to have full control of polarization as well as amplitude and phase of the signal in the far field. One type of antenna that is particularly well suited for integrated radiator arrays with DPC is the four-spoke multi-port driven (MPD) antenna [12]. It consists of a signal ring that is driven at four points against a set of ground spokes that extend radially from the center of the antenna out to the signal ring. While the previous implementation of the MPD antenna involved equally spaced drive phases to create a circular polarization, modifying the amplitudes and phases of the various drive ports can create any polarization.

In this work, we have implemented a $2 \times 1$ DPC radiator array in 32 nm CMOS SOI process using two polarization-controlled MPD antennas locked to each other in a 1-D phased array, shown in Fig. 3. Each DPC radiator element is designed to perform local power generation using its own driver circuitry within the element's core. The drive phases and amplitudes of the generated waveforms are controlled through phase rotators and multiple buffer stages, respectively. Although such a drive circuit is sufficient for dynamic polarization control of a single element DPC radiator, the proper operation of the entire DPC phased array requires a central locking network to ensure phase locking of the individual elements. It should be kept in mind that these array dependent blocks introduce additional power overhead for small phased arrays such as this, but they become less significant as they become shared among more elements in a larger array, and are a requirement of the radiator being a phased array. This overhead should not be associated primarily with the ability to control polarization.

The block diagram of the driver circuitry of the DPC phased array is shown in Fig. 4. The DPC phased array is designed to
locally generate power within each element of the array and also lock the phases of the two individual radiating elements to a central reference. This allows us to synchronize the frequencies of the two elements as well as locally adjusting the phase of the reference signal within each element to enable independent control over its phase based on the reference phase [20].

A central quadrature oscillator provides the reference quadrature signals at the desired frequency for radiation. The quadrature signals are then distributed across the chip through a locking network consisting of three buffer stages and additional feed lines that route the quadrature signals into the cores of the two radiating elements. In each core, these quadrature signals drive two phase rotators whose phases can be arbitrarily set through independent control lines. Output of each of these phase rotators is then injected into one of the two oscillators of the core, as seen in Fig. 4. These oscillators are implemented to locally generate power inside the core which allows the locking network to distribute lower power levels. Injection of phase rotators' outputs into the oscillators results in locking each oscillator's phase and frequency to the phase and frequency of the injected signal from the corresponding phase rotator, thus achieving both frequency synchronization and full phase control over core's driving circuit. Oscillators' outputs are then amplified by another set of three buffer stages and drive the antenna of the radiating element and radiate with the desired polarization that corresponds to the phase rotator's specific settings.

III. CIRCUIT IMPLEMENTATION

The driver circuitry used in this design contains blocks including the oscillators, locking network phase rotators and amplifying stages (Fig. 4). These blocks allow for power generation, signal distribution, frequency synchronization of the radiating elements, and phase and amplitude control of the driving signals.

A. Oscillator Design

The central quadrature oscillator generates quadrature signals at the fundamental frequency of operation to synchronize the frequencies of individual radiators and to overcome possible frequency drifting or mismatch of individual elements' oscillators. An inaccuracy in the modeling of the tank inductors and parasitic capacitors that manifested differently in the central oscillator than the radiator oscillators due to their loading differences resulted in a slight frequency deviation to 105.5 GHz and diminished frequency overlap of the locking range. The quadrature signals, when routed to each element, provide the possibility of arbitrary phase generation through proper weighted summation of in-phase and quadrature components.

The quadrature oscillator's schematic is shown in Fig. 5. It consists of two cross-coupled differential oscillators that are also coupled to each other to provide quadrature signals. Although strong coupling through quadrature coupling transistors would have been sufficient to ensure quadrature oscillation [23], such strong coupling degrades the phase noise of the oscillator [24], [25]. Thus, in our design, the coupling between the two oscillators happens through two different mechanisms whose simultaneous operation ensures quadrature oscillation while avoiding strong quadrature coupling to minimize phase noise degradation.

The first coupling mechanism is a resistive network at the tails of the two cross-coupled oscillators that couples them through second harmonic injection. Such resistive coupling on its own allows four different oscillatory modes: leading quadrature, lagging quadrature, differential, and common-mode oscillation [26]. In order to prevent differential and common-mode oscillations and enforce quadrature oscillation, a second coupling mechanism through small quadrature coupling transistors is added to the circuit. Although the resistive network does not guarantee quadrature oscillation on its own, its presence reduces the effective strength of quadrature coupling transistors and thus improves the phase noise.
Simultaneous operation of the two mechanisms can be better understood by replacing the “Y” resistive network ($R_{c}$ and $R_{t}$) with its equivalent “Δ” network ($R'_{c}$ and $R'_{t}$) and then simplifying it by introducing ideal current sources ($I_{tail}$) instead of tail resistors, $R'_{c}$, as demonstrated in Fig. 5. In the simplified circuit, the value of coupling resistor, $R'_{c}$, can be adjusted to apply any arbitrary second harmonic coupling strength between the two oscillators without affecting their DC currents which are set to $I_{tail}$ by ideal current sources. In the absence of any second harmonic coupling at the tails, i.e., large values of $R'_{c}$, phase noise of the quadrature oscillator at 1 MHz offset degrades as the width of the coupling transistors increases, as shown in Fig. 6, motivating use of very small transistors for improved phase noise performance. However, in practice, using very small coupling transistors may result in insufficient coupling strength for the two oscillators to lock to each other in the presence of layout parasitics and undesired coupling through substrate to other signals. In order to overcome this issue, we add second harmonic coupling between the two oscillators by reducing $R'_{c}$. In quadrature mode of operation, each oscillator tries to push the other oscillator out of phase through the coupling transistors and the equal strength of the two oscillators results in quadrature operation. In this mode, the common nodes of the two oscillators ($P$ and $Q$ in Fig. 5) contain significant 180° out of phase second harmonic voltages due to transistors nonlinearity. In the presence of $R'_{c}$, we can use the Y-parameters of the two-port network to see that the magnitude of second harmonic current at the tail of each oscillator is equal to $|V_{P, h/2} / R'_{c} - V_{Q, h/2} / R'_{c}|$, which means that due to differential operation of $V_{P, h/2}$ and $V_{Q, h/2}$, each oscillator injects additional in-phase second harmonic current into the other oscillator and helps it to maintain its existing phase as opposed to quadrature coupling transistors. Reducing the value of $R'_{c}$ increases the strength of this coupling which in turn reduces the overall effective quadrature coupling strength but improves phase noise. This is also shown in Fig. 6 where simulated phase noise at 1 MHz offset is plotted versus $R'_{c}$ for different coupling transistors widths.

The equivalent “Δ” network at the tail also reveals that there is no additional voltage headroom loss due to the resistive coupling network since the coupling resistor, $R'_{c}$, appears in parallel to the tail current sources or the tail resistors and does not draw any DC current. The value of $R'_{c}$ determines the DC current of the oscillators and $R'_{c}$ sets the desired second harmonic coupling strength. It should also be noted that stronger second harmonic coupling increases the output amplitude of the oscillators since the two oscillators help each other constructively through the tail network. However, very strong second harmonic coupling (very small values of $R'_{c}$) increases the second harmonic content of individual outputs of the oscillators and corrupts the output waveform compared to a clean sine wave, as shown in Fig. 6. Thus the tolerable amount of harmonics in the output waveform sets a lower limit on $R'_{c}$.

Once the values of $R'_{c}$ and $R'_{t}$ are set, either of equivalent “Δ” or “Y” networks can be used based on layout constraints. In this work, we have used “Y” network due to better layout compatibility with $R_{c} - R_{t} = 15 \Omega$, $W_{M_{t}} = 0.5 \mu m$, and $W_{M_{c}} = 20 \mu m$. The post-extraction simulated phase noise of the quadrature oscillator is −73.5 dBc/Hz at 1 MHz offset from the carrier frequency and it provides −14 dBm of output power per quadrature line that feeds the locking network buffer chain.

### B. Locking Network

Quadrature oscillator outputs are distributed to the radiating elements through the locking network. Two chains of three differential amplifier stages follow both in-phase and quadrature outputs of the oscillator. Each chain consists of a 5 μm wide differential common source and two differential cascode stages (15 μm and 30 μm). The gain of the buffer set can be adjusted through the biasing network to allow additional control over the signal strength. After the third stage, the outputs split and form two sets of quadrature signals. Each set is then routed into the core of one of the radiating elements. The feeding lines from the locking network are routed above the ground plane to the vicinity of the antennas. Beyond that point they are pushed below the ground plane and are routed to the core under one of the ground spokes to minimize electromagnetic interaction between the antenna and the reference quadrature signals. Inside the core, these quadrature lines are connected to the phase rotators. Quadrature outputs of the locking network provide −26.5 dBm of input power per quadrature line to the phase rotation unit of each radiating element.

### C. Phase Rotators

The phase rotation unit of each element consists of two phase rotator circuits. Fig. 7 shows the schematic of each phase rotator circuit consisting of two Gilbert cells that are fed by the four quadrature input voltages (from the locking network) and produce in-phase and quadrature currents as outputs [27]. The outputs of the Gilbert cells are connected together to add up the output currents. All four tail currents of the two Gilbert cells can be independently controlled by adjusting the control voltages at the gates of tail transistors. Independent control over the tail currents allows setting arbitrary weights for I-I and Q-Q components, thus enabling full 360° phase control as well as amplitude control over the differential output current. Simulated
output current of one of the phase rotators for eight different settings results in eight different phases while maintaining constant amplitude as illustrated in Fig. 8. The differential output current of each phase rotator is then directly injected into the output nodes of one of the two cross-coupled oscillators of the radiator core and locks the oscillator’s outputs at the phase and frequency of the injected current, producing two sets of differential signals whose phases can be arbitrarily adjusted. To maintain polarization matching, only relatively slow control of the phase and amplitude are required, and thus low frequency control lines were routed to the radiator core, though if faster switching of polarization was desired, higher speed lines could be implemented in future versions.

D. Amplifiers

Each of the two differential outputs of the oscillators in each core drive a differential buffer chain. The chain consists of three stages of amplification (Fig. 9). The first stage is a 5 μm wide differential common source stage which is DC coupled to the oscillator. The next two stages are differential cascode amplifiers, 15 μm and 30 μm wide, respectively and are AC coupled to previous stage to allow for differential voltage at the drains and gates of the cascode and common source transistors. The AC coupling capacitors are set at 22.6 fF to maximize the power transfer to the next stage based on impedance matching requirements. Differential amplification of oscillator outputs allows using differential inductors as load impedances that in turn reduces the amount of required bypass capacitance for proper performance by advantageing virtual grounds.

The DC currents of the amplifiers are set through the biasing network. Thus, by adjusting the DC currents of the amplifiers, we can control the gain of the entire chain. Simulation results show that the gain can be adjusted from 0 dB to 12.5 dB, while providing a maximum output power of −3.1 dBm per quadrature line.

IV. DESIGN, ANALYSIS, AND SIMULATION OF ANTENNAS

A. Antenna Analysis

A simplified analysis similar to that in [12], but generalizing for the ports’ phases and amplitudes provides insight into how this polarization control is obtained. The DPC is achieved by separating the antenna into two isolated superposition
subparts that independently produce two orthogonal polarizations. By controlling the amplitude and phase of each of these polarization subparts independently, the polarization of the overall electric field can be controlled. In order to gain design insights a couple of simplifying assumptions must be made: the antenna will have a circumference of $g\lambda$ (Fig. 10) and it will be analyzed in free-space with the substrate neglected for the moment. The first assumption is that there is low coupling between the ring and various spokes, and this assumption has been verified through full 3D electromagnetic simulation [12]. This will allow for superposition where the signal ring and ground spokes will be analyzed separately, 2 ports at a time. The second assumption is that currents on a line that are terminated with a virtual short will form sinusoidal standing current waves similar to a lossless transmission line. The broadside electric field, $E$, due to a set of time harmonic currents, $I$, on a plane can be given by [28]:

$$E = \frac{j\omega\mu}{4\pi} \int_C I e^{-jKR} dI$$

where $\mu$ is the permeability of the medium, $\omega$ is the angular frequency of the signal, $k = \omega\sqrt{\mu\varepsilon}$, $\varepsilon$ is the permittivity of the medium, and $R$ is the distance between the current plane and the observer. Thus, the direction of the electric field vector will be the same as that of the integration of the currents, and its polarization will be determined by that same integration. Thus once the currents on the ring and spokes are defined, they can be integrated to generate expressions for the far-field electric field. For this 4-spoke MPD antenna, pairs of ports on opposite spokes (ports 1 and 3, and 2 and 4) will be analyzed separately using superposition, and will be referred to as superposition subpart A (ports 1 and 3) and superposition subpart B (ports 2 and 4). These pairs of ports are driven with the same amplitude but 180° out of phase.

Due to the symmetry of the ring, the portion of the currents orthogonal to spoke A on the top half of the ring will cancel those from the bottom half, while the currents parallel to the spoke will add constructively. Thus, a single quadrant of the ring can be analyzed and the electromagnetic field produced by the currents parallel to the spoke will be quadrupled to take all four quadrants into account. Once only superposition subpart A is being considered, there will be three virtual shorts along the differential axis of symmetry. The port impedances of ports 2 and 4 can thus be neglected in the calculations for subpart A as they are in parallel with the virtual short. In practice, this means that as the phase and amplitude of subpart B are changed, the current densities being contributed by subpart A will not be changed, and there is isolation between the two subparts in this simplified model. The current densities can then be defined on the ring and spoke structures shown in Fig. 11. This allows the current densities to be expressed as

$$I_{\text{ring A}Q1} = I_{\text{max}} \cos \beta l - I_{\text{max}} \cos \left[\frac{g(\pi/2 - \phi)}{\lambda}\right]$$

for the current on the ring in the first quadrant, and

$$I_{\text{sp A}} = I_{\text{max}} \cos \beta l - I_{\text{max}} \cos \left(\frac{2\pi}{\lambda}\right) \hat{u}_x$$

for the current on spoke A. Integrating this current for the far-field electric field given in (1) yields

$$E_{\text{ring A}} = -I_A \frac{j\mu\varepsilon e^{-jKR}}{2\pi} \frac{g}{R} \left(\frac{1}{g^2 - 1}\right) \hat{u}_x$$

$$E_{\text{sp A}} = -I_A \frac{j\mu\varepsilon e^{-jKR}}{2\pi} \frac{1}{H_0} \tan(g) \hat{u}_x$$
for the electric fields due to currents on the ring and spoke respectively from subpart A, and that sum to the far-field electric field for the entirety subpart A of

\[ \mathbf{E}_A = -I_A \frac{j \mu_0 c e^{-jkRe}}{2\pi} \left[ \frac{g}{g^2 - 1} + \tan(g) \right] \mathbf{u}_x. \quad (6) \]

The analysis for subpart B is identical to subpart A, but rotated 90°, and yields a far-field electric field for the entirety subpart B of

\[ \mathbf{E}_B = -I_B \frac{j \mu_0 c e^{-jkRe}}{2\pi} \left[ \frac{g}{g^2 - 1} + \tan(g) \right] \mathbf{u}_y. \quad (7) \]

There are two interesting observations to note from (6) and (7). The first is that the ring should be sized such that \( 1 < g < \pi/2 \) in order to have the currents on the spoke and ring add up constructively. The resulting current distributions for each subpart for a design within this range are shown in Fig. 12 and provide both a general design guideline, and also a frequency range over which a given implementation of the design will maintain the desired current patterns [12]. The second observation is that regardless of any of the design parameters being considered, the far-field electric field will always be linearly polarized along the axis of the subpart's spoke.

When summed together, each superposition subpart will determine the phase and amplitude of orthogonal linear polarizations, with the drive ports of each subpart being isolated from one another as shown in Fig. 13. This result gives the required four degrees of freedom to enable control of the phase and amplitude at any far-field polarization.

The control of the amplitude and phase of each subpart will determine the far-field polarization. For example, if the two subparts are either in phase or 180° out of phase, it will result in linear polarization in the far field, that can be rotated the full 180° polarization angle by changing the relative amplitudes of the subparts. On the other hand, controlling the phase difference between the two subparts can create linear polarization when they are in phase, all the way to circular polarization when they are in quadrature and have equal amplitudes. Any desired far-field polarization can be obtained by decomposing it into the projections of that polarization into the two orthogonal linearly polarized components and adjusting the amplitudes and relative phases of subparts A and B to provide those orthogonal polarization components.

B. Electromagnetic Simulation of Antenna Array

The simplified analysis of the DPC antenna provides intuition to the operation of the radiator, but some of the non-idealities associated with the physical implementation of the antenna also must be considered to ensure proper functionality of the radiator, including the effect of the surrounding metals on the surface of the chip as well as the effect of the silicon substrate on the radiator. The antenna cannot operate in isolation and proper consideration must be given to providing DC and locking signals to the driver circuitry without being detrimental to the antenna's radiation pattern.

The circuitry will be located within a driver core at the center of the antenna and be shielded by a local ground plane as depicted in the block diagram in Fig. 4. This ground plane will both help to shield the transistors and inductors from the antenna's electromagnetic radiation as well as to provide a ground to the microstrip transmission lines that route the signals from the output amplifier stages to the ports of the antenna. The size of this local ground plane should be kept to a minimum to ensure that the mm-wave currents traveling through the spoke and ground plane stay as close to the desired operation as possible. This will limit the space to layout the core circuitry and create a tradeoff between core size and isolation between the various inductors within the core. The DC ground will be fed through the ground spokes that are extended out to a global ground plane that has been pulled back from the antenna by around \( \lambda/4 \), as shown in Fig. 14. The impedance looking outward down the spokes from the antenna's ports should be high as it is \( \lambda/4 \) from the ground plane, and thus most of the return ground current will flow back down the spoke toward the center of the antenna as assumed in the previous analysis. DC supply and locking signal
Fig. 13. Radiated far-field electric fields due to each subpart, and how they sum together to produce any far field polarization by controlling amplitude and phase of each subpart.

Fig. 14. Additional non-idealities including the effects of extending the spokes out to an upper ground plane pulled back $\lambda/4$ from the antenna as well as a standard substrate around thick mounted on a PCB with a lower ground plane.

lines are run underneath the spokes to minimize interference with the radiated signals.

The silicon substrate will also significantly affect the radiation pattern. Because the dielectric constant of silicon is much higher than that of air, most of the radiated power will initially go down into the substrate. The standard 250 $\mu$m thick chip is mounted onto a ground plane to reflect that signal back up and out of the chip (Fig. 14). The thickness of the chip is close enough to a quarter of a wavelength that the reflected wave will add constructively with the signal that is initially radiated upward. Another way of thinking about it is to look at impedances, where the top of the chip is around a quarter wavelength from the ground plane, which creates a high impedance looking downward and thus directs most of the power upward. In simulation there is a 1 dB variation in gain from the 250 $\mu$m substrate thickness for any substrate thickness from 220 $\mu$m to 270 $\mu$m, well within the tolerance of standard thinning processes.

The $2 \times 1$ radiator array design was simulated using 3D finite element method electromagnetic solver HFSS with a lossy substrate and chip conductors, but an ideally conductive reflection off of the PCB ground plane as it is estimated that the losses associated with the doped substrate will dominate. The ground plane of the inner radiator core is included in the simulation, but does not affect the radiation significantly ($< 1$ dB change in gain). The diameter of the antenna ring is 520 $\mu$m, with an array spacing of 1 mm. It is important that the gain of the antenna be similar regardless of the desired polarization so that the power flux in a given direction will not change significantly as the polarization is controlled. Due to the isolation between the two superposition subparts, the gain of the simplified antenna does not depend on the desired polarization, but verification is required to insure that none of the non-idealities captured by the electromagnetic simulation cause significant deterioration to this isolation. When compared to the equations of the simplified analysis, the polarization achieved for various drives is similar to what is predicted, with full tuning range of polarization angle and a maximum deviation of less than $7^\circ$ compared with the analysis, and axial ratios from 1.8 dB (compared to 0 dB for circular polarization) through 25 dB (compared with infinity for linear polarization). The antenna gain patterns in linear and circular polarization modes are shown in Fig. 15 for two planes: $\phi = 0^\circ$ and $\phi = 90^\circ$. The efficiency from the output of the transistors (including impedance transformation, signal routing and antenna) to the far field radiation is 12%. The maximum gain of the antenna (again from the output of the transistors to the far field radiation) in linear polarization mode is 0.8 dBi, which is within 0.3 dB of the maximum gain in circular polarization of 0.5 dBi, with similar single lobe patterns which allows the polarization to be controlled while maintaining reasonably similar levels of power flux.
Fig. 15. Simulated radiation gain pattern of the 2 × 1 array in circularly polarized mode and linearly polarized mode for planes $\phi = 0^\circ$ (a) and $\phi = 90^\circ$ (b) show similar patterns and maximum gains within 0.3 dBi of each other.

Fig. 16. Measurement setup for the 2 × 1 radiator with DPC.

V. MEASUREMENTS

The chip was fabricated in a 32 nm CMOS SOI process with two 1.2 $\mu$m thick top copper layers and a 2.275 $\mu$m aluminum layer. The measurement setup is shown in Fig. 16. The chip was mounted using silver epoxy onto a ground plane on an FR4 PCB. DC supply and control voltages were wire bonded to traces on the PCB. The PCB was then mounted to a two-dimensional rotational stepper motor to enable radiation pattern measurements. The radiated signal was captured with a 22 dBi gain linearly polarized horn antenna that is fed to an 8th harmonic mixer whose IF output is amplified and fed to a spectrum analyzer. The distance between the radiator and receive antenna is 120 mm, or 42 wavelengths, a distance at which the received power shows a dependence, indicating far-field operation. The entire setup is calibrated using an Erikson PM4 calorimeter-based power meter that measures absolute broadband power by converting the electromagnetic power to heat. The antenna is rotated to capture the projection of the polarization onto the linear axis at every angle between 0° and 180° in a similar manner to the approach explained in the appendix of [12]. By capturing the linear projection at all angles, the angles of the maximum and minimum power can be obtained, which correspond to the major and minor axis of the polarization ellipse. The angle of the major axis corresponds to the polarization angle, while the ratio of powers between the major and minor elliptical axes corresponds to the polarization axial ratio. For the antenna pattern measurements, the entire pattern was swept for receive antenna angles stepped every 5° from 0° to 180°. The radiator consumes 476 mW of DC power from a 1.3 V supply and occupies a physical chip area of 2.64 $\text{mm}^2$.

The measured calibrated received spectrum when the radiator array is in linear polarization mode is given in Fig. 17. An effective isotropic radiated power (EIRP) of +7.8 dBm was measured at 105.5 GHz. Next the radiator was rotated across the entire half-space to produce the antenna patterns. Two measured elevation plane patterns are plotted in Fig. 18 for $\phi = 0^\circ$, along the axis of the array and $\phi = 90^\circ$, perpendicular to the array. To show the beam steering capabilities of the one dimensional phased array, the phases of all ports in one of the antennas were shifted to steer the beam along the axis of the array ($\phi = 0^\circ$), and beam steering of up to 15° along that axis is observed and plotted. The steering range is limited to the small size of the two element array and to substrate mode coupling at more extreme angles and thus also increases coupling between the two antennas through the substrate. A side lobe is observed in the plane. The beam is narrower in the plane because it is the plane of the array and thus experiences array gain. The total radiated power integrated over the entire half space was measured to be 0.9 mW which is higher than the expected simulated power of 0.5 mW, which may be due to an overestimation of the loss of the substrate at these frequencies.

It is important to consider polarization in many radiation directions when discussing the polarization of antennas, and especially integrated antennas where the substrate can affect the polarization in non-broadside radiation directions. One benefit of this implementation of DPC is that the polarization can be controlled not just in the broadside dimension, but off axis as well. To showcase this, all of the DPC measurements have been performed at three separate directions of Fig. 19. One is in the broadside direction, one is 20° off axis when $\phi = 0^\circ$ and one is 30° off axis when $\phi = 90^\circ$. When the polarization is being
controlled along the axis of the array, beam steering is also implemented to steer the beam toward the target as well as controlling its polarization.

Predictable and deterministic polarization control of the radiator is shown through two measurements: controlling the polarization angle while maintaining linear polarization, and controlling the axial ratio while maintaining a constant polarization angle, depicted in Fig. 20. Due to variation between the various circuit blocks, a calibration was done by measuring the output polarization at various settings and creating a lookup table to ensure that the proper phases were being fed to the antennas. The first measurement shows the viability of using this radiator to maintain polarization matching to a linearly polarized receive antenna whose orientation is rotating in space. The measurements in Fig. 21 show complete tuning range of the polarization angle from $0^\circ$ to $180^\circ$ while maintaining near linear polarization with axial ratios above 10 dB in all three of the demonstrated directions.

The second DPC measurement is to tune the polarization axial ratio while maintaining a constant polarization angle, as shown in Fig. 22. These measurements show tunability of polarization ratio from 2.4 dB through 14 dB in all three radiation directions, with the high end of 14 dB being limited by the SNR of the measurement test setup. The low end of 2.4 dB, while being typical of circularly polarized systems, means that the radiator was not able to produce completely circular polarization, which is likely due to the fact that the array is not square and thus the coupling to substrate modes in the directions parallel and perpendicular to the array were not the same. If lower axial ratios were necessary for the application, a perfectly square phased array can be utilized to achieve a larger tuning range on the axial ratio.

To the best of the authors' knowledge this work presents the first integrated radiator with dynamically controllable polarization. Table I gives comparisons with other integrated radiators with static polarizations without external dielectrics. A die photo of the radiator is shown in Fig. 23.

VI. CONCLUSION

Dynamic control over the electromagnetic polarization of an integrated radiator allows for polarization matching and maximum coupling between antennas to be maintained regardless of polarization and orientation in space of the receive antenna.
This work demonstrates DPC using a $2 \times 1$ fully integrated phased array at 105.5 GHz in 32 nm CMOS SOI. It utilizes a central locking oscillator that locks the core of each radiator at the fundamental frequency. Phase rotators in the locking network give independent phase control to two subparts of each radiator, while gain control of the amplifying stages provides amplitude control to each subpart. Reasonable electromagnetic isolation between the subparts of each antenna allow the phase and amplitude of each subpart to be controlled independently without significant degradation to the radiating performance of the orthogonal subpart. The radiator array achieves a complete tuning range of the polarization angle from 0° to 180° for linear polarization in the broadside direction as well as in off-axis directions. A tuning range from 2.4 dB to 14 dB of the polarization axial ratio is shown while maintaining near constant polarization in the broadside direction while being able to steer its beam in one dimension.

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REFERENCES

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