A 7GHz Wideband Self-Correcting Quadrature VCO

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***Abstract*— A 4.0 to 6.6GHz self-correcting quadrature voltage controlled oscillator (QVCO) with phase compensation loop is implemented in a 65nm CMOS process. The topology couples IQ oscillation signals of two LC-VCOs, a phase shifter, and buffers with circular configuration. This paper introduces the idea to obtain low phase noise and accurate IQ phase quadrature oscillation signal, by employing phase compensation loop to correct the IQ phase error. The self-correcting QVCO achieves the IQ phase error less than a degree, and 1MHz offset phase noise -107dBc/Hz at 6.9GHz.**

I. INTRODUCTION

The ever-increasing demand for wireless communication transceiver keeps pushing wireless LAN (WLAN) systems such as IEEE 802.11a/b/g/n, WiMAX, and LTE to support higher data rates over greater distances. In the realization of these systems, local oscillators with quadrature outputs with wide frequency tuning range and low phase noise are key building blocks. There are several ways to generate quadrature local signals, such as using poly-phase filter, even-stage ring oscillator, frequency divider, and quadrature LC VCO (QVCO) [1], [2], [3]. For 6GHz quadrature local generation, poly-phase filters are not able to create precise quadrature signals due to the susceptibility to the RC component inaccuracy and loss in the signals amplitude. The combination of frequency divider and differential LC VCO (Fig. 1a) is common way to create quadrature signals, however, it requires the VCO to oscillate at twice the necessary quadrature local frequency, making it more difficult to realize a wide frequency tuning rage VCO due to the effect of the parasitic capacitances. Furthermore, buffer amplifiers operating at 12GHz are needed to transfer and condition local signals. In terms of the power consumption and frequency tuning range, QVCO is the ideal candidate to create quadrature local signal.

Since a quadrature LC oscillator was introduced in the standard CMOS technology, extensive research on the phase noise and phase accuracy analysis of quadrature output LC VCO has been carried out [2], [3]. Fig. 1b shows the schematic of the conventional QVCO with the coupling current source [4]. The coupling factor of the conventional QVCO is controlled by the coupling current I_C. If the coupling factor is low, the output signal of the QVCO shows low phase noise, but poor quadrature phase accuracy. On the other hand, if the coupling factor is high, it can produce precise phase accuracy at the expense of degraded phase noise.

To overcome the trade-off between phase noise and phase accuracy, self-correcting phase correction loop was employed.

II. SELF-CORRECTING QVCO

A. Topology of the overall QVCO

Fig. 2 shows block diagram of the self-correcting QVCO. It is composed of a QVCO core which consists of coupled two LC VCOs, and a phase compensation loop which corrects the IQ phase error. Its core is composed of two differential LC VCOs and phase shifters, and it has IQ output with inverter buffer. The phase compensation loop consists of a phase detector, low pass filters, amplifiers, and phase shifters. The IQ outputs of the QVCO are fed to the phase detector to detect the phase error at the QVCO. The low pass filter attenuates the high frequency components of the phase detector output. The dc component output of the phase detector is amplified by the low bandwidth amplifier, and this signal is fed back to control input of the phase shifter. Fig. 2b shows the block diagram of the core of the self-correcting QVCO, which consists of two LC VCOs, inverter buffers, and phase shifters. Outputs of the VCOs are placed with phase shifters and inverter buffers in a circular configuration. The I and Q output signals come out at the node

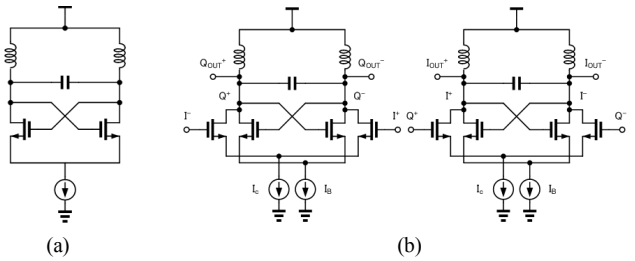
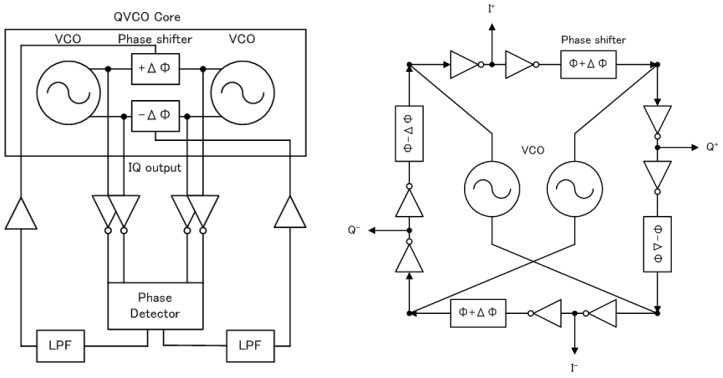


Figure 1. Topology of (a) Differential LC VCO (b)Conventional QVCO



(a) (b)

Figure 2. (a)The self-correcting QVCO (b)QVCO core

between the two inverter buffers. One of the differential phase detector output signals is sent back to the phase shifter $+\Delta\Phi$, described in Fig. 2, and the other is to $-\Delta\Phi$. This coupling technique reduces the noise source of the oscillator, because it does not require extra current and transistors, contrary to the current sources of the conventional quadrature VCO for the coupling.

B. Differential LC VCO

To achieve wide tuning range for the oscillation frequency, there are two main issues in the design of LC VCO. First, it is desirable to keep the oscillation signal amplitude constant. However, the negative resistance required to start and maintain oscillation varies across the tuning frequency range. One way to achieve this is to choose the transistor transconductance to be sufficiently large to assure the start up and oscillation, which causes the deterioration of the phase noise at the high oscillation frequency due to the excess signal amplitude and an increase in the power consumption. Second, the VCO gain variation over the frequency range can lead to challenges for designing stable PLL.

To satisfy the start-up condition of the oscillator, transistors of the oscillator need to provide the transconductance, to compensate the oscillator tank loss during the oscillation, indicated in the following equation.

$$g_m \geq 1/R_T = R_{sL} / (\varpi_0 \cdot L)^2 \qquad (1)$$

where the g_m, R_T , R_{sL}, and ϖ_0 are a total transconductance of a VCO, a tank equivalent resistance, an inductor series resistance, and oscillation frequency, respectively.

This equation describes the minimum requirement for the oscillator transconductance, and it also indicates that the lower limit of the transconductance strongly depends on the oscillation frequency. If the oscillation frequency is halved, the required minimum transconductance increases roughly by the factor of four. Therefore, if the oscillator uses the constant transconductance for wideband VCO, most of the power is wasted at the maximum oscillation frequency.

It is important to keep oscillation signal amplitude at the optimum amplitude. As described above, if the oscillation

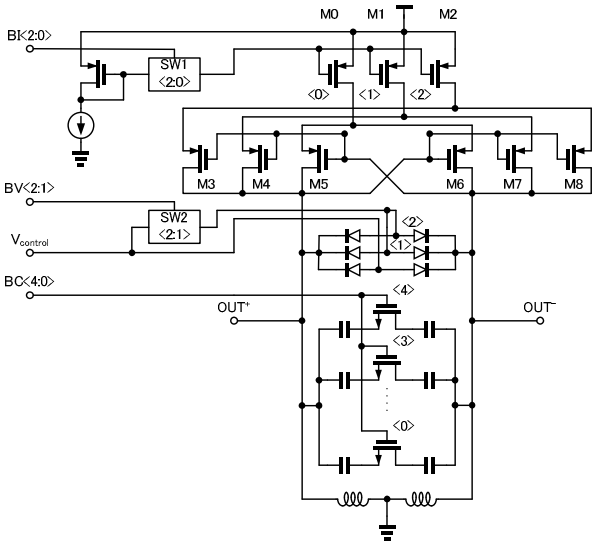


Figure 3. Schematic of the LC-differential VCO

frequency is halved, equivalent tank impedance is reduced by the factor of four. Thus, the current of the oscillator should be four times greater to keep the amplitude constant. Moreover, as described in (1), it is necessary to increase the transconductance by a factor of four to maintain oscillation. If the increase of the transconductance is achieved by changing the transistor size by a factor of four, operating point of the transistor is constant, and the oscillator can operate at the optimum region, close to the boundary condition between voltage limited region and current limited region. Thus, to obtain low phase noise, it is important to keep both oscillation signal amplitude and operating point constant, and it can be achieved by controlling the overall transconductance.

To overcome these issues, the transistor gate width in the LC VCO is made controllable by changing the control bits BI<2:0> in the Fig. 3. This control bit is powered down M0-2 by controlling SW1, and the transconductance of the transistor M3-8 is also controlled.

To keep the VCO gain constant, varactor finger number can be controlled depending on the oscillation frequency with BV<2:1> bits. Varactors are divided into three binary weighted segments, where the smallest one is always active. The other two can be given fixed high voltage to minimize and to keep constant capacitance when they are not used for controlling the frequency.

The coarse frequency tuning is controlled by the 5-bit BC<4:0> in Fig. 3, which controls the binary weighted MOM capacitor bank bits. And, the fine tuning is carried out by the control voltage $V_{control}$ in Fig. 3, and BV<2:1> is also controlled depending on the BC<4:0> to maintain the VCO gain constant. The tuning range is heavily depends on the parasitic capacitance associated with the switch transistor for the MOM capacitor bank, and the transconductor transistor of the oscillator.

C. Phase compensation loop

The self-correcting QVCO has the phase compensation loop, to correct the I and Q phase mismatch due to the

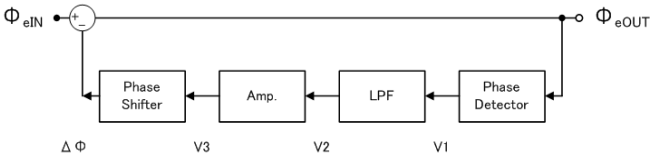


Figure 4. Block diagram of the phase compensation loop

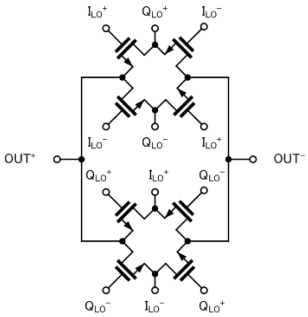


Figure 5. Schematic of phase detector

inductor coupling, and device mismatch [3]. The block diagram of this loop is shown in the Fig. 4. The loop is composed of a phase detector, a low pass filter, an amplifier, and a phase shifter. The phase error of the oscillator signal is detected by the phase detector, and the high frequency component of the output signal is removed by the low pass filter. Then, the dc component of the signal is amplified, and this is used for controlling the phase shifter input to control the phase of IQ signal.

1) Phase Detector: The phase detector schematic is shown in the Fig. 5. This is composed of passive mixers, and the differential output signal V_1 is given by

$$V_1(t) = 4 \cdot A_{VCO} \cdot \sin(2 \cdot \varpi_0 \cdot t + \phi_e(t)) + 4 \cdot A_{VCO} \cdot \sin\phi_e(t) \quad (2)$$

where A_{VCO} is the amplitude of the oscillation signal, and ϕ_e is the IQ phase error. As the $2 \cdot \varpi_0 \cdot t$ component is removed by the low pass filter, the transfer function is approximated as follows.

$$H_{PD}(s) = V_1(s) / \phi_e(s) = 4 \cdot A_{VCO} \quad (3)$$

2) Low Pass Filter: The low pass filter is a simple RC filter. It attenuates the twice the oscillation frequency signal output from the phase detector, and pass through the dc components originated from the IQ phase error. The transfer function of the low pass filter is expressed by

$$H_{LPF}(s) = V_2(s) / V_1(s) = 1 / (1 + R_{LPF} \cdot C_{LPF} \cdot s) \quad (4)$$

where R_{LPF}, C_{LPF} are the resistance and capacitance of the low pass filter.

3) Amplifier : The amplifier is a low bandwidth two-stage operational amplifier, which amplifies the low frequency

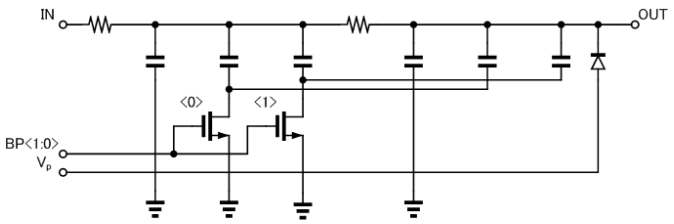
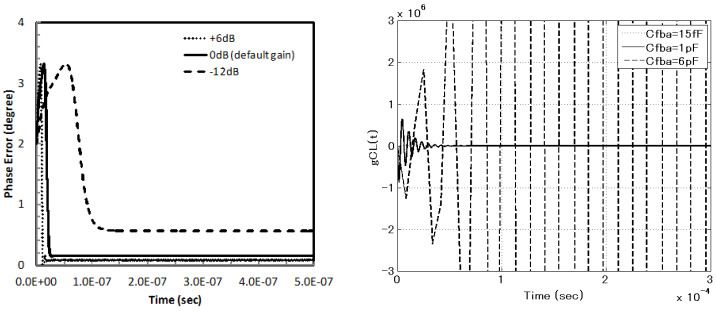


Figure 6. Schematic of phase shifter



(a) (b)

Figure 7. (a)Phase error compensation (b)Impulse response of the loop

output of the low pass filter. It consumes 0.5mW from 1.0V power supply. The transfer function of a two-stage amplifier is expressed by

$$H_{AMP}(s) = V_3(s) / V_2(s) = (a_0 / (1 + b_1 \cdot s))^2 \quad (5)$$

where a_0 and b_1 are the coefficients of the amplifier transfer function.

4) Phase shifter: The phase shifter is composed of RC filter with 2 bits capacitance control switch, and a varactor, as shown in the Fig. 6. These control bit are changed depending on the oscillation frequency. The amplifier output signal controls varactor input node V_P in the Fig. 6, and controls phase compensation. The input voltage and the phase output is given by

$$\phi_e(t) = \phi_{PS}(V_3(t))$$

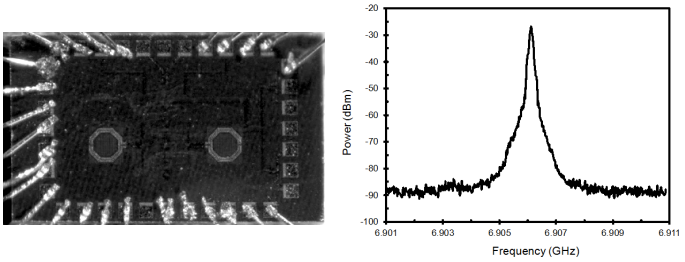
$$= a_4 \cdot V_3(t)^4 + a_3 \cdot V_3(t)^3 + a_2 \cdot V_3(t)^2 + a_1 \cdot V_3(t) + a_0 \quad (6)$$

where a_i is the coefficients of the polynomial. The $\Delta\phi_e$ is the amount of phase shift in the phase compensation loop, and given by

$$\Delta\phi_e(t) = f_{PS}(V_3(t)) - f_{PS}(V_3(0)) \quad (7)$$

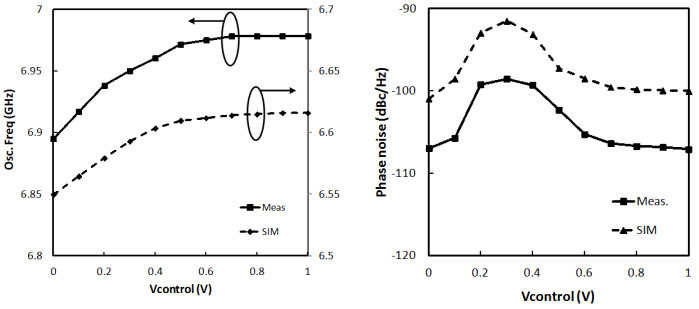
The transfer function of the phase shifter is expressed by

$$H_{PS}(s) = \phi_e(s) / V_1(s) = K_{PS} / s \quad (8)$$



(a) (b)

Figure 8. (a)Chip micrograph (b)Measured output spectrum



(a) (b)

Figure 9. (a)Measured oscillation frequency (b)phase noise

where K_{PS} is the coefficient of the transfer function. Therefore, the open loop transfer function $G_{OP}(s)$ is give by

$$G_{OP}(s) = -H_{PD}(s)\cdot H_{LPF}(s)\cdot H_{AMP}(s)\cdot H_{PS}(s) \quad (9)$$

$$= -4\cdot A_{VCO}\cdot(1/(1+R_{LPF}\cdot C_{LPF}\cdot s))(a_0/(1+b_1\cdot s))^2(K_{PS}/s) \quad (10)$$

Then, the close loop transfer function $G_{CL}(s)$ results in

$$G_{CL}(s) = \phi_{eOUT}(s) / \phi_{eIN}(s) = 1/(1-G_{OP}(s)) \quad (11)$$

The phase error response of the loop was analyzed with (11). Fig. 7a shows the phase error is corrected by the loop to less than 0.2degree in the initial phase error 2degree case. The higher amplifier gain gives more error correction, but excess gain makes the loop behavior unstable. Fig. 7b shows impulse response of the phase compensation loop. It also shows optimum amplifier output capacitance (C_{fba}) is inevitable for the stable loop response. Total power consumption of phase compensation loop is 0.5mW, consumed by the amplifiers.

III. EXPERIMENTAL RESULTS

The self-correcting QVCO has been fabricated in 65nm CMOS process with eight aluminum metal layers and 3μm copper thick metal option. The chip micrograph of the self-correcting QVCO is shown in Fig. 8a. The chip size is 1.2mm × 0.9mm including pads for probing and bonding, and the QVCO core circuit is 0.7mm × 0.3mm. Coupling circuits, composed of inverter buffers, phase shifters, and low pass filters, are in the circular configuration between two LC VCOs to achieve symmetry in the layout. The phase detector is located in the center of the coupling circuits. The chip is mounted on the 69mm × 79mm PCB, composed of 2-layer 1.6mm thick FR-4. And, it is wire bonded to the PCB, only the oscillation signal is probed by a RF probe.

Fig. 8b shows the spectrum from the QVCO at the maximum oscillation frequency 6.9GHz. Fig. 9a shows the measured and simulated maximum oscillation frequency versus VCO control voltage, $V_{control}$, for minimum capacitor code. The relation between phase noise and $V_{control}$ are shown in the Fig. 9b. The phase noise at 1MHz offset from 6.9GHz carrier is -107dBc/Hz. The IQ phase error is measured at the output of the QVCO buffer, connected at the input of the phase detector, with RF probe and oscilloscope. The phase error is less than a degree at 6.9GHz. The simulated VCO gain at the maximum and minimum frequency is 150MHz/V and 100MHz/V, respectively. The measured VCO gain at the maximum frequency is close to the simulated value.

Performances of the self-correcting quadrature VCO have been evaluated with following figure of merit.

$$FOMTP = 10\log\left(L\{f_{offset}\}\cdot P_{DC}\cdot\left(\frac{f_{offset}}{f_0}\right)^2\cdot\left(\frac{10}{FTR}\right)\cdot(PhaseError)\right) \quad (12)$$

where $L\{f_{offset}\}$ dBc/Hz is phase noise at 1MHz offset, f_{offset} Hz, P_{DC} mW is the dissipated power of the oscillator, f_0 Hz is the oscillation frequency, *FTR* % is the frequency tuning range of the oscillator, and *PhaseError* degree is the IQ phase error of the quadrature oscillator output. The self-correcting QVCO dissipates 17mW from 1V supply at the 6.9GHz maximum oscillation frequency. The measured and simulated results show 6.9 and 5.3GHz center oscillation frequency, 1 and 50% FTR, -107 and -120dBc/Hz at 1MHz offset phase noise, and 1 and 0.5degree IQ phase error. The FOMTP of measured and simulation are 153 and 200dBc/Hz, respectively.

IV. CONCLUSION

The self-correcting QVCO with phase error compensation loop has presented. The conventional quadrature oscillator suffers from the trade off relation between phase noise and the phase accuracy. This topology corrects IQ phase error while it maintains low phase noise and constant VCO gain. Furthermore, the coupling technique of two LC VCO achieves low noise and low power consumption.

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