CMOS I/Q Subharmonic Mixer for Millimeter-Wave Atmospheric Remote Sensing

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***Abstract*—A compact second harmonic 180 GHz I/Q balanced resistive mixer is realized in a 32-nm SOI CMOS technology for atmospheric remote sensing applications. The MMIC further includes two on-chip IF amplifiers at the mixer's I and Q channels. A conversion gain of +8 dB is achieved with 74 mW of dc power consumption using a 1.2 V supply. The measured IF frequency range is from 1 to 10 GHz. The mixer achieves a 20 dB image-rejection (IR) ratio with an LO input power of +4 dBm. The chip size is 0.75 mm^2 including probing pads.**

***Index Terms*—CMOS integrated circuit, millimeter-wave integrated circuit, mixers, MMICs, remote sensing.**

I. INTRODUCTION

CMOS has been the favored technology for high volume and low cost applications due to its capability of high level of integration and high yield. There has been enormous development in the field of CMOS circuits operating at millimeter-wave frequencies [1], [2]. Besides low noise (temperature), miniature size, low power consumption, and light weight are desirable features for large array radiometers, such as Geostationary Synthetic Thinned Aperture Radiometer (GeoSTAR) [3]. These features have been traditionally obtained using III–V compound semiconductors. The possibility to integrate more functions on a single silicon chip would enable reducing the size and mass of the synthetic array radiometers and small satellites (CubeSats) [4].

The aim of this letter is to study the feasibility of using CMOS technology in atmospheric remote sensing receiver front-ends operating at an atmospheric window channel of 183 GHz. In general, the gain and noise performance of the CMOS technology is not competitive with that of III–V semiconductor technologies. However, CMOS circuitry could be utilized by employing preceding III–V high-gain low-noise amplifiers determining the required receiver noise figure. Bearing this receiver architecture in mind, in this letter we present the design of a compact wideband CMOS 180 GHz second harmonic balanced I/Q resistive mixer along with two IF amplifiers at the mixer's I and Q channel.

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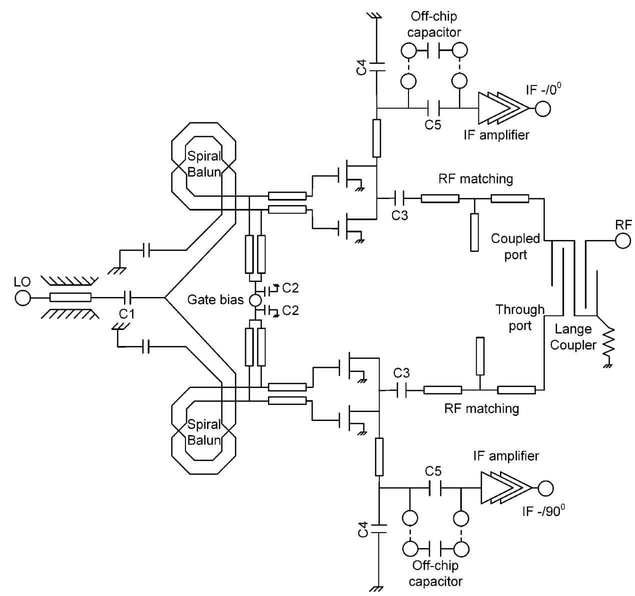

Fig. 1. A simplified schematic of the designed image-rejection subharmonic resistive mixer with integrated IF amplifiers. The IF amplifiers consist of three-stage cascaded resistive feedback inverters.

II. CIRCUIT DESIGN AND REALIZATION

The concept of a subharmonically pumped resistive mixer was first demonstrated at X-band in [5]. It has a number of advantages over the fundamental mixers, especially in millimeter-wave frequencies. For example, it requires only half of the LO frequency compared to a fundamental mixer and increases the LO to RF isolation significantly. Therefore, subharmonically pumped resistive mixer topology is utilized in this design. The design methodology applied for the second harmonic I/Q balanced resistive mixer is similar to the one realized in Indium Phosphide (InP) HEMT technology [3].

The simplified circuit schematic of the designed balanced second harmonic I/Q resistive mixer together with the IF amplifiers is shown in Fig. 1. The mixer consists of two single-balanced unit resistive mixers where each unit has two 11×1 μm NMOS transistors. The LO signal is applied from a coplanar waveguide and split up into two spiral transmission

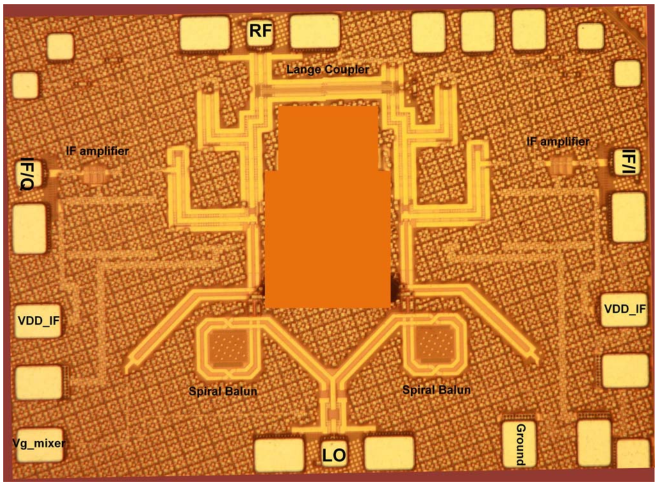

Fig. 2. Micrograph of the realized CMOS subharmonic I/Q mixer.

line baluns. The spiral baluns provide the required 180° phase shift to the transistor gates of each unit mixer [6]. A short circuited differential shunt stub together with a series line is used to transform the low-impedance of the transistor gate to a higher impedance level which helps to obtain better LO port matching [7].

The RF-signal is applied through a Lange coupler to generate the required wideband 90° phase shift for good image-rejection performance at the drains of the unit mixers. The generated in-phase IF signals are combined by connecting the transistor drains of each unit mixer. The connection points are virtual grounds for the LO signals. Quarter-wavelength short-circuited shunt stubs at RF frequency are used to prevent the millimeter-wave signals from entering into the IF circuitry. Finally, the IF signals from the two channels (I and Q) are amplified by the IF amplifiers. Each amplifier consists of three-stage cascaded resistive feedback inverters.

The transistor modeling relies on the RC parasitic extraction of the transistor layout and the EM simulation of the drain, gate, and source accesses. The Lange coupler is implemented in the microstrip environment [8]. The matching networks for the RF side are also realized in the microstrip environment and modeled through an EM simulator. EM simulations are also carried out for modeling the LO and RF probe pads and spiral transmission line baluns. Finger capacitors are used in the circuit design and their models are taken from the design kit's library model. The chip was fabricated in a 32-nm SOI CMOS technology. The chip area including the probing pads is 0.75 mm^2. A micrograph of the chip is shown in Fig. 2.

III. Measured Mixer Performance

On-wafer measurements were carried out to characterize the mixer performance. The required LO signal was obtained from a signal source together with a 4× W-band multiplier chain. The RF-signal was also generated by multiplying the signal from a signal generator using a G-band 12× multiplier. Coplanar (ground-signal-ground) RF probes are used for delivering the LO and RF signal to the chip. The LO signal power from the multiplier chains was calibrated using a power meter along with

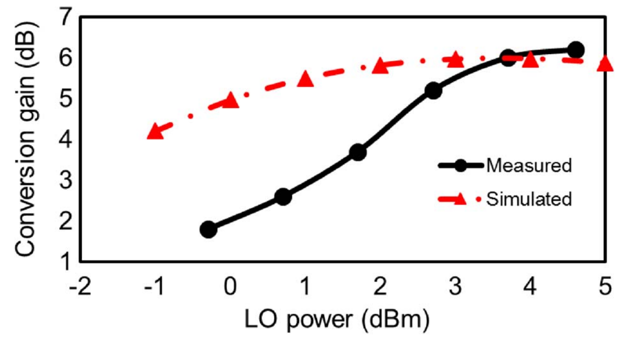

Fig. 3. Measured and simulated conversion gain of Q-channel as a function of LO-power at a fixed LO and RF frequency of 85 GHz, and 172 GHz, respectively.

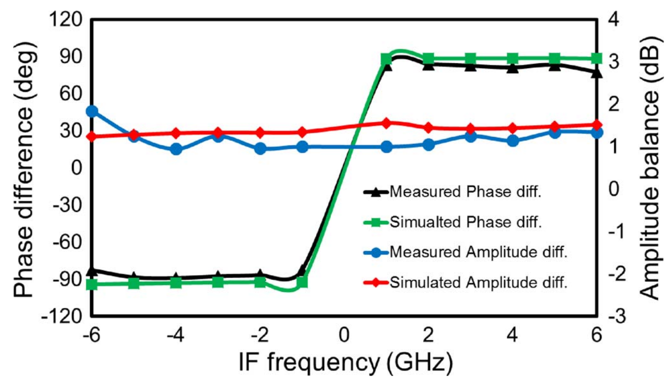

Fig. 4. Measured and simulated quadrature response as a function of IF frequency. The LO was at 90 GHz and RF was swept from 174 to 186 GHz.

a W-band power sensor and the RF signal was calibrated with an Erikson calorimeter. The output IF signal spectrums were measured with a spectrum analyzer and the time domain IF signals were measured with an oscilloscope. The mixer gates were biased to 0.16 V which is below the pinch-off for optimum mixing performance. The resistive mixer does not draw any current but the IF amplifiers consume a total current of 62 mA using a 1.2 V supply.

The conversion gain was measured as a function of the LO power and as can be seen from Fig. 3, a +4 dBm LO power level is enough for optimum mixing operation. A low LO power performance is very important since it will simplify the LO system development and reduce the receiver power requirements [3].

The down-converted quadrature response of the designed mixer is shown in Fig. 4. The response was recorded from 1 to 6 GHz where the upper frequency limit was set by the measuring equipment. The mixer along with the IF amplifiers exhibits an amplitude imbalance of less than 2 dB and the phase imbalance of maximum 5° between the IF channels.

The measured upper and lower side-band conversion gain at a fixed IF frequency of 2 GHz is presented in Fig. 5. An RF frequency range from 158 to 182 GHz is achieved with a conversion gain of 8 to 5.6 dB. The measured conversion gain and image-rejection ratio as a function of IF frequency are shown in Fig. 6. A 3 dB IF bandwidth is realized from 1 to 6 GHz with 20 dB IR ratio. The conversion gain is limited at

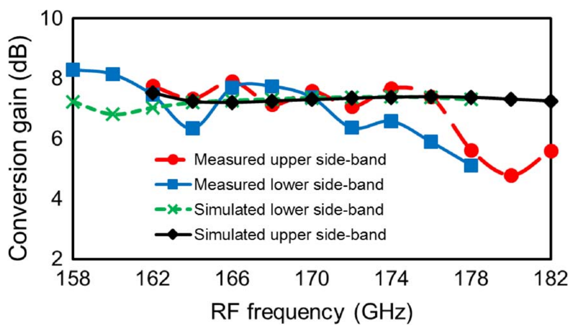

Fig. 5. Measured and simulated upper and lower side-band conversion gain of I-channel at a fixed IF frequency of 2 GHz when the LO was swept from 80 to 90 GHz using a +4 dBm LO power.

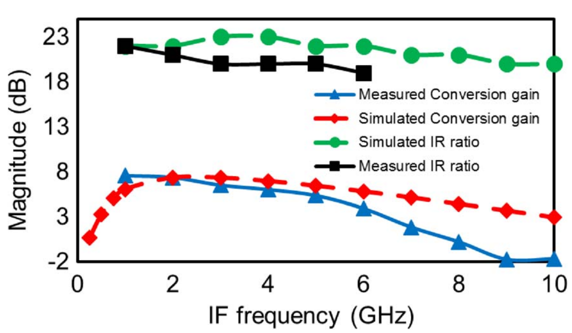

Fig. 6. Measured and simulated conversion gain of I-channel and IR ratio as a function of the IF frequency. The LO was fixed at 85 GHz and RF was swept from 170 to 180 GHz.

lower frequencies because of on chip DC-blocking capacitors, C5 (Fig. 1) used between the mixer channels (I and Q) and the IF amplifiers to simplify the mixer circuit design. Although not tested in this work, off-chip capacitors shown in Fig. 1 can be used to extend the lower frequency bandwidth. Nevertheless, the measurement results show that the designed MMIC is capable of providing an IF bandwidth from 1 to 10 GHz which is required for certain atmospheric radiometer systems [9].

The mixer and IF amplifier chain has a simulated noise figure of 26 dB which should be adequate for the intended application assuming high-gain low-noise InP HEMT amplifiers in the preceding stages.

IV. Conclusion

In this letter, we have presented the design of a CMOS millimeter-wave subharmonic I/Q balanced resistive mixer in the 180-GHz frequency band. This compact design includes on-chip LO power division, required phase shift for the IF signals, and IF amplification. The state-of-the-art results published for MMIC subharmonic I/Q mixers around 180 GHz are shown in Table I . The presented results show record conversion gain at 180 GHz in CMOS technology. A wide RF frequency tuning range and good phase and amplitude balance between the channels are realized. Furthermore, a very good agreement between the simulation and measurement results indicates the accuracy of our circuit modeling. More importantly, the performance of this first cycle developed CMOS mixer is comparable to the InP HEMT mixer reported in [3], and demonstrates the potential of the CMOS technology for designing 180 GHz receiver front-ends suitable for atmospheric remote sensing applications.

TABLE I
State-of-the-Art Performance of mm-Wave I/Q Subharmonic Mixers

Ref.	This work	[3]	[10]	[11]
Technology	32-nm SOI CMOS	35-nm InP HEMT	GaAs Schottky diode	MHEMT
Circuit topology	2x mixer + IF amplifier	2x mixer	4x mixer	2x mixer
RF frequency (GHz)	158-182	180	180-196	182-201
LO frequency (GHz)	80-90	90	47	91
Peak conversion gain (dB)	+8*	-21⁺	-21	-18
IR ratio (dB)	>20	>20	>15	>20
IF bandwidth (GHz)	1-10	0.01-1	1-8	0.01-1
LO power (dBm)	4	3	18.7	2
DC power (mW)	74	0	0	0

*Simulated conversion gain of the stand-alone mixer is -23 dB.
⁺Estimated mixer conversion gain.

References

[1] C. Marcu, D. Chowdhury, C. Thakkar, J.-D. Park, L.-K. Kong, M. Tabesh, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, E. Alon, and A. Niknejad, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3434–3447, Dec. 2009.

[2] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.

[3] P. Kangaslahti, D. Pukala, T. Gaier, A. Tanner, I. O'Dwyer, B. Lambrigtsen, X. Mei, and R. Lai, "Miniature low noise G-band I-Q receiver," in *IEEE MTT-S Int. Dig.*, Anaheim, CA, May 2010, pp. 497–500.

[4] A. Toorian, K. Diaz, and S. Lee, "The cubesat approach to space access," in *Proc. IEEE Aerosp. Conf.*, Mar. 2008, pp. 1–14.

[5] H. Zirath, "A subharmonically pumped resistive dual-HEMT mixer," in *IEEE MTT-S Int. Dig.*, 1991, pp. 857–878.

[6] M. Varonen, M. Kärkkäinen, J. Riska, P. Kangaslahti, and K. Halonen, "Resistive HEMT mixers for 60-GHz broad-band telecommunication," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1322–1330, Apr. 2005.

[7] D. Parveg, M. Varonen, M. Kärkkäinen, A. Vahdati, and K. Halonen, "Design of 130-GHz up and down-conversion CMOS mixers," in *Proc. 9th Conf. Ph. D. Res. Microelectron. Electron. (PRIME)*, Villach, Austria, Jun. 2013, pp. 77–80.

[8] M. Kärkkäinen, D. Sandstrom, M. Varonen, and K. Halonen, "Transmission line and lange coupler implementations in CMOS," in *Proc. Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Paris, France, Sep. 2010, pp. 357–360.

[9] S.-T. Brown, B. Lambrigtsen, R.-F. Denning, T. Gaier, P. Kangaslahti, B.-H. Lim, J.-M. Tanabe, and A.-B. Tanner, "The high-altitude MMIC sounding radiometer for the global hawk unmanned aerial vehicle: Instrument description and performance," *IEEE Trans. Geosci. Remote Sensing*, vol. 49, no. 9, pp. 3291–3301, Sep. 2011.

[10] J. Archer and J. Tello, "A 180–196 GHz image-reject schottky-diode MMIC mixer," *Microw. Opt. Tech. Lett.*, vol. 49, no. 10, pp. 2319–2322, Oct. 2007.

[11] D. Lopez-Diaz, I. Kallfass, A. Tessmann, A. Leuther, H. Massler, M. Schlechtweg, and O. Ambacher, "Subhamonically pumped 210 GHz I/Q mixers," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, Monterey, CA, Oct. 2010, pp. 1–4.