200-GHz CMOS amplifier with 9-dB noise figure for atmospheric remote sensing

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The feasibility of using CMOS technology for RF amplification in atmospheric remote sensing receiver is studied. The design and measurement results of a 200-GHz low-noise amplifier which is fabricated using a 32-nm SOI CMOS technology are presented. The 8-stage amplifier in a common-source configuration achieves a 9-dB noise figure and 25-dB gain with a power consumption of 33 mW.

Introduction: The recent development of millimetre-wave CMOS and SiGe circuits have made silicon technologies attractive also for non-commercial low-volume applications such as the atmospheric remote sensing where III–V compound semiconductors have been traditionally used for the millimetre-wave receiver technology. The possibility to integrate more functions on the same silicon chip would enable reducing the mass and size of synthetic array radiometers and small satellites (cubesats). The scaling of silicon technologies has enabled CMOS and SiGe amplifiers to operate above 200 GHz [1–3]. Although the gain performance of these circuits is promising the noise figure (NF) is not competitive to their III–V counterparts making them not suitable as the first amplification stage for atmospheric remote sensing receivers presented in [4], where InP HEMT technology is used to reach the required sensitivity. However, provided that the NF is low enough (i.e. below 10 dB for the 183 GHz receiver in [5]) and the gain and power consumption are reasonable a silicon amplifier could be utilised so that the receiver NF would be determined by the preceding HEMT MMIC low-noise amplifier. So far an 11-dB NF was measured at 245 GHz using SiGe technology [3] and an 11-dB NF was demonstrated around 210 GHz using CMOS technology [6]. In this Letter, we present the design and measurement result of a 200-GHz amplifier fabricated using a 32-nm silicon-on-insulator (SOI) CMOS technology, which achieves a 9-dB NF around 200 GHz with a 25-dB gain and a power consumption of 33 mW.

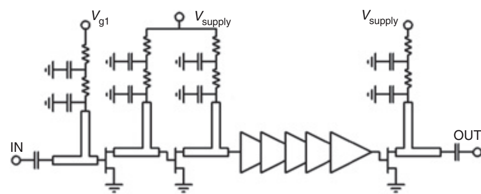

Fig. 1 *Simplified schematic of amplifier*

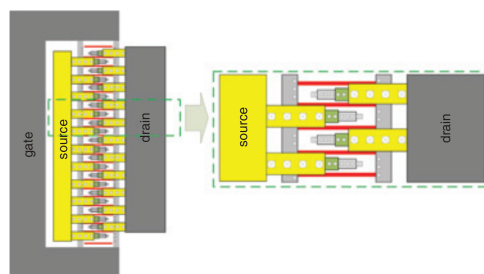

Fig. 2 *Simplified transistor layout. 21 × 1 μm device was used in all amplifier stages*

Circuit design: A simplified schematic of the amplifier is shown in Fig. 1. Series transmission lines and short-circuited shunt stubs are used for matching eight common-source stages. All stages use similar matching network topology. The shunt stubs are also used for biasing. Bias lines include resistor capacitor networks to ensure low-frequency and out-of-band stability. Transmission lines were designed as grounded coplanar waveguides (GCPWs) similarly as in [7]. GCPW topology was chosen because it can provide a good ground access for the transistor source through the bottom ground plane of the GCPW and at the same time fulfil the metal density requirements without allowing any dummy metal between the side grounds. For optimum transistor performance a relaxed gate pitch [8] with double contacted gates and staggered drain and source metal connections [9] were utilised in transistor layout drawing as shown in Fig. 2. A 21 × 1 μm wide transistor was chosen as a suitable device size for the amplifier design. As shown in the schematic dc-blocking capacitors are utilised only at the input and output of the amplifier. The gate of the first stage is biased separately and the rest of the gates and drains are dc-coupled.

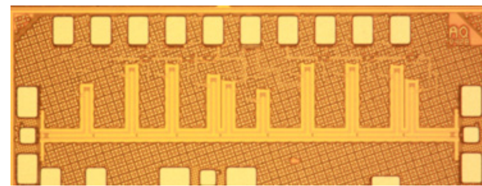

Fig. 3 *Micrograph of amplifier*

Although biasing the gate and drain to the same voltage reduces gain performance of the transistor, potential modelling errors and loss of the decoupling capacitors are avoided in this way (as discussed in [1, 10]).

Measurement results: The LNA was fabricated in a 32-nm SOI CMOS technology and the micrograph of the amplifier is shown in Fig. 3. The chip area is 1.240 mm × 0.450 mm. The *S*-parameters of the amplifier were measured on-wafer using WR5 waveguide frequency extenders. Results are shown in Fig. 4. The circuit draws a total of 47.7 mA of DC current using a 0.69-V supply voltage. The small-signal gain is 25 dB around 200 GHz and better than 20 dB from 190 to 210 GHz. Input and output matchings are better than 10 dB at 200 GHz.

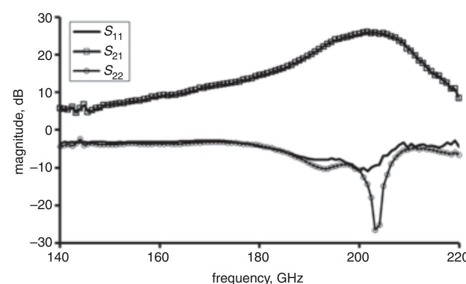

Fig. 4 *Measured S-parameters of amplifier*

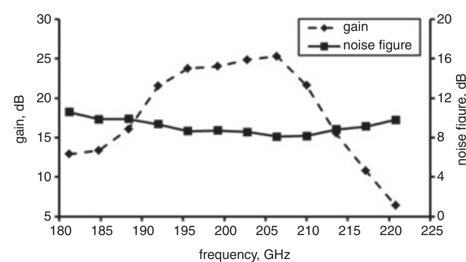

Fig. 5 *Measured NF and insertion gain of amplifier. Loss of probes and backend contribution are subtracted from results*

The noise measurement was carried out on-wafer using Y-factor method. A standard WR5 horn antenna was connected to the RF input probe. The cold load was an absorber coated cone-load dunked in liquid nitrogen at 77 K, while the hot load was at room temperature (295 K) load. A WR5 second harmonic mixer is used to downconvert the RF signal to baseband after which the IF signal is amplified, filtered and detected using a power meter. To obtain the amplifier chip noise with a minimum backend noise contribution an in-house developed WR5 InP HEMT LNA module was used between the output RF probe and the mixer. The LO source consists of a multiplier chain fed from a synthesiser. Insertion loss of the RF probes (GGB Industries Inc. WR5 coplanar waveguide probes) was obtained by measuring the S-parameters of the series combination of the input and output probes when placed on a thru line and the net series insertion loss was divided into half as in [11]. The insertion loss of a single probe was estimated to be 2.2 dB around 200 GHz and was verified using two different lines, i.e. a thru line on a GGB CS15 alumina calibration substrate and a

GCPW line implemented in a 50-μm thick InP MMIC technology. The measured NF and insertion gain are shown in Fig. 5. The amplifier chip achieves a 9-dB NF around 200 GHz.

Table 1: Low-noise amplifier performances around 200 GHz

Ref.	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	P_{DC} (mW)	Gain/ stage (dB)	Gain/ P_{DC} (dB/ mW)
[5]	InP HEMT	183	18	4.1[a]	12	6	1.5
[12]	SiGe BiCMOS	200	16.9	9.4[b]	18	8.5[c]	0.94
[3]	SiGe BiCMOS	245	18	11	303	3.6[c,d]	0.06
[6]	SOI CMOS	210	18	11	44.5	2.6[d]	0.40
This work	SOI CMOS	200	25	9	33	3.1	0.76

[a]Waveguide packaged
[b]Simulated
[c]Cascode
[d]Differential

Conclusion: Table 1 shows a comparison of amplifiers operating around 200 GHz and implemented in InP HEMT, SiGe and CMOS technologies. The amplifier presented in this Letter achieves the lowest measured NF in silicon technologies and highest gain performance in CMOS technologies. The achieved gain and noise performance are adequate for utilising the amplifier as a second amplification stage in an atmospheric remote sensing receiver front-end. However, it should be noted that the power consumption is doubled compared to an InP HEMT amplifier. Nevertheless, the excessive power requirement of the stand-alone LNA may be restored in receiver level design by the potentially high integration level obtained from CMOS technology.

Acknowledgments: This work was supported by the Academy of Finland, by Alfred Kordel Foundation and in part by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

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Submitted: *30 September 2015* E-first: *28 January 2016*
doi: 10.1049/el.2015.3337
One or more of the Figures in this Letter are available in colour online.

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