Fully Integrated CMOS X-band Power Amplifier Quad with Current Reuse and Dynamic Digital Feedback (DDF) Capabilities

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***Abstract*—A 10GHz fully-integrated stacked PA quad with dynamic digital feedback and control loops provides total output power of 200mW at 37% PAE. It utilizes data provided by multiple on-chip sensors to maintain safe operating conditions and regulate the individual power PA power supply voltages and independent power control for each PA. This digitally controlled stacked PA quad with on-chip matching allows higher operation voltages while maintaining current consumption constant, leading to higher overall system efficiency, as ohmic drop losses under large supply-to-breakdown voltage ratios are reduced.**

***Index Terms*—CMOS integrated circuits, phase shifters, power amplifiers, microwave integrated circuits, phased-arrays, dynamic digital feedback, MIMO, phase locked loops**

I. Introduction

CMOS radio-frequency integrated circuits (RF ICs) have continued to penetrate and will eventually dominate various high-frequency applications, many of which have been the sole domain of other technologies in the past. This is primarily due to the favourable yield, achievable system complexity, and cost structure of CMOS SoCs in large-scale production. MIMO (e.g., [1]) and phased-array systems consisting of a large number of radiators and chips continue to be of great interest in various communications, sensing, ranging, and energy management systems to increase their range, data rates, and performance.

The design of fully integrated power amplifiers (PAs) in CMOS technologies for these applications is challenging due to the low breakdown voltages of CMOS transistors compared to other technologies. Cascode or stacked transistor techniques (e.g., [2][3][4]) have been used to reduce the voltage stress on any single transistor. However, MIMO and phased array systems require independent control of the signal characteristics of each channel (e.g., phase and amplitude), which presents a challenge in stacked design due to the strong coupling of the voltages and currents of individual stages. In this paper, we propose a novel architecture that stacks the power amplifier in supply domain and, thereby, reuses the supply current while operating from a high supply voltage and allowing for independent control of the operation point of different stages. The architecture is devised to withstand a broad range of intended variations (phase and amplitude), as well as unintended deviations (load mismatch and temperature fluctuation) of the operation conditions among the stages in the stack.

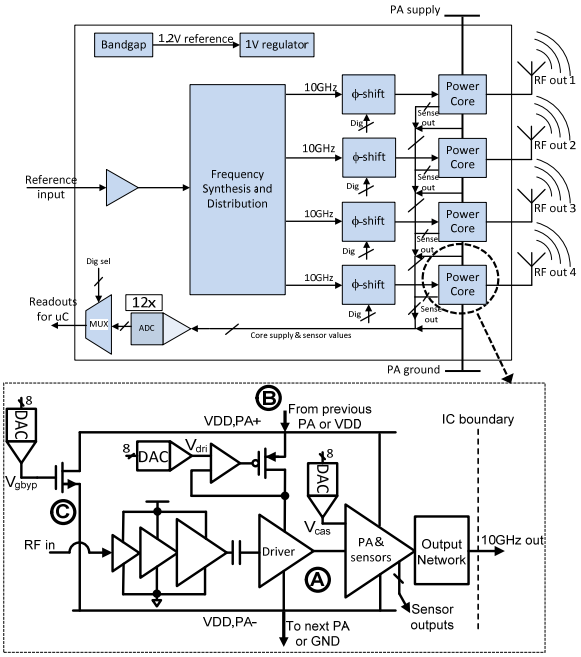

Fig.1: Simplified block diagram of the integrated X-Band power amplifier quad

II. Stacked Quad PA Architecture

To achieve independent control of power cores in a stack of multiple amplifying stages, the DC voltage and operating conditions of the individual amplifiers need to be dynamically monitored, as a change in operating conditions of any one amplifier in the stack affects all other PAs. Furthermore, PA bias needs to be constantly actuated to operate each PA under known and safe conditions to guarantee long-term reliability. For a phased-array transceiver, all RF output phases need to be adjustable, with some amplitude control highly desirable. To address these requirements, we implemented a fully integrated power amplifier quad that operates four PAs in a stack from a nominal 3.2V supply, while providing full phase and amplitude control, as shown in the block diagram of Fig.1.

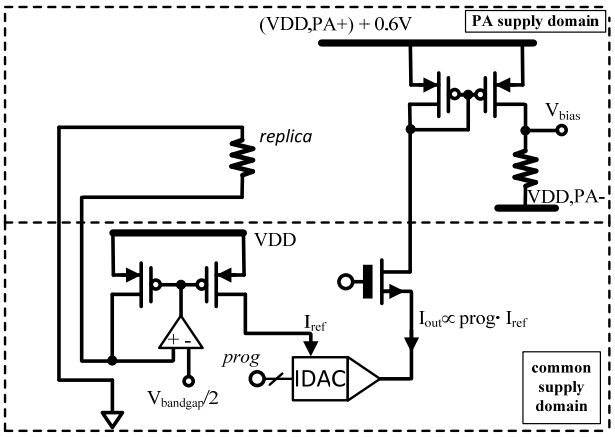

Fig. 2: Bias current generation used for crossing supply domain boundaries. DACs and regulators operate in the common supply domain, providing currents across boundaries to generate voltage offsets proportional to a bandgap voltage in the PA supply domains

Each of the four power cores implements a full amplifier chain that amplifies a phase controlled signal RF_{in} to the desired output power level of 17dBm while operating the power consuming driver and PA stage from a floating supply. Operational sensors monitor the local supply voltage drop as well as the PA core current consumption and voltage stress. Local ADCs convert the sensor outputs for use with digital operation and feedback control.

III. Implementation Details

Shown in fig. 1, each of the four driver and PA output stages (marked A) are operated from a separate local supply domain (marked B). Both stages are biased using digitally controllable driver supply/PA gate bias voltage V_{dri} and PA cascode voltage V_{cas}, which can be used to lower or increase the supply current drawn from the PA supply domain and set the output power.

All bias voltages are referenced to the local PA ground voltage to provide constant biasing conditions to the driver and output stage. The bias voltages are digitally controlled and compared to a known bandgap bias voltage. A simplified circuit diagram is shown in Fig. 2. Biasing currents for all nodes are generated by a current DACs (IDACs) operating in a common 1V supply (lower half of figure). Reference currents for each of the IDACs are generated to provide a voltage drop commensurate with a bandgap voltage over a resistor in each core. Replica resistors in the cores are then biased with currents proportional to the reference currents to generate known drops across these resistors.

In the event of a sudden undesirable change in the load condition seen by any of the power cores resulting in reduced supply current, a digitally controllable bypass device (marked C in Fig.1) is activated to maintain the overall branch current keeping the voltage drops across all stacked stages within a pre-specified range of variations. Each PA output stage includes a cascode peak voltage sensor and a DC current sensor. On-chip ADCs convert the output of these sensors as well as the absolute voltage levels of the local PA supply voltages to allow an MCU to make the appropriate adjustment on these via V_{dri}, V_{cas} and V_{gbyp} using the IDACs. These bias voltages are generated using on-chip current-mode DACs as described above.

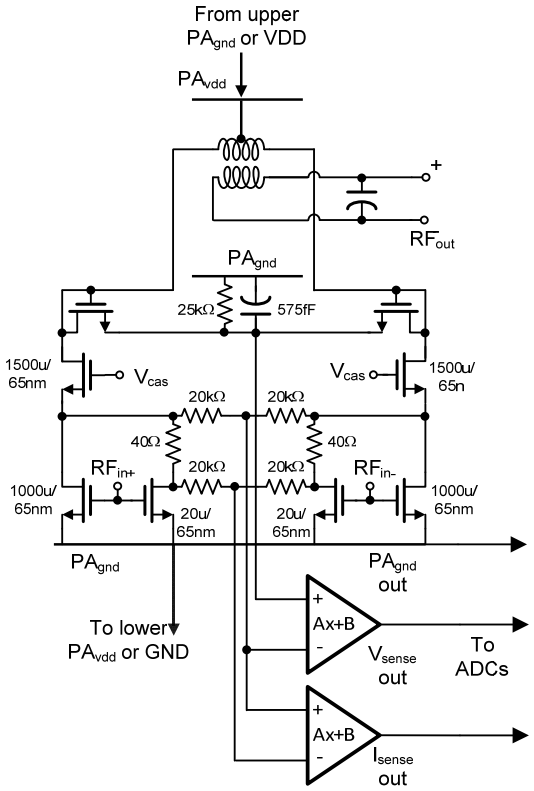

Fig. 3: Circuit detail for PA core, cascode peak voltage and DC current detectors, as well as supply level readout for digitally assisted operation

In order to complete a digital feedback loop and full operational control, detectors for the DC current and (cascode) peak voltage are implemented within the PA core (Fig.3) together with ADCs for digital readout of detector values and intermediate supply voltage levels. Linear voltage amplifiers with preset offsets are used to limit the detector output to a known window of operationally relevant outputs. The amplifiers use input choppers to limit errors due to noise and mismatch from 25mVrms input referred to 500uVrms, allowing to use small geometry devices and limiting required current overhead. The ADCs are realized using an 8-bit SAR architecture including periodic offset compensation. ADC outputs are selected and serialized to be readable by a microcontroller via a standard SPI interface. The SPI interface also allows the MCU to program all operational

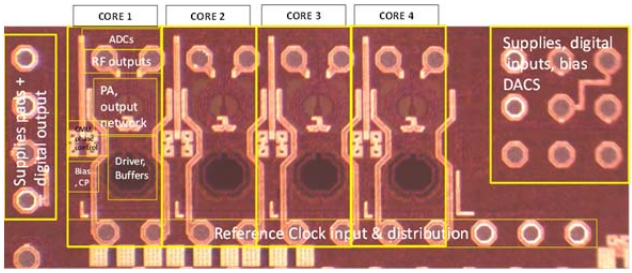

Fig. 4: Die photograph of implemented power amplifier quadrant

registers (e.g., for bias voltages). The on-chip RF signal is synthesized and phase-shifted from an input clock at one fourth of the output frequency using on-chip clock multiplier units that consume less than five mA of current while providing digital output phase control.

IV. Measurement Results and Conclusion

A fully integrated, four PA stack (quad) including integrated output transformer and impedance matching networks, sensors, clock-multiplier units (CMUs) and phase shifters, is implemented in a bulk 65nm CMOS process. Fig.4 shows the die photograph. Total die are is 0.8 x 2.3mm. An off-chip MCU based on an ARM® Cortex-M0® processor supports operation of all aspects of the system. Four power cores are stacked to operate from an overall 3.2V voltage supply (compare Fig. 1 and Fig 5). The MCU continuously reads sensor values for all four PAs and implements a software Proportional-Summation-Difference (PSD) controller to adjust the gate voltages of the bypass devices (C in Fig. 1). PSD values to provide stable and well-damped controller operation were determined using manual adjustment of coefficients. Plotted in Fig. 5 is the actual transient response of all local power amplifier supply voltages to a disturbance of operating conditions at t=0 as measured and recorded by the on-chip ADCs and the MCU, respectively.

The use of fully digital operational control allows for

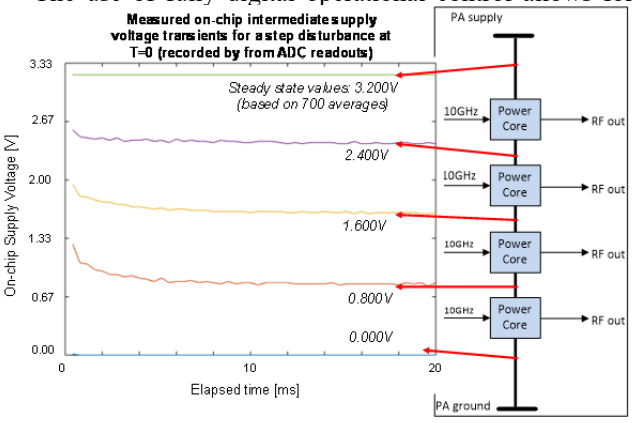

Fig. 5: Measured supply voltage regulation for PSD controller under disturbance at iteration t=0

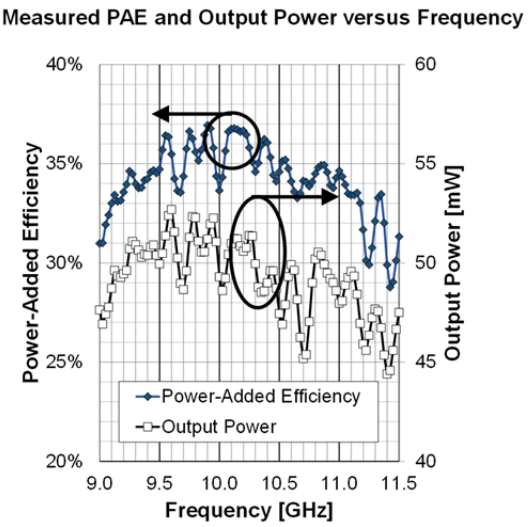

Fig.6: Measured PAE and output power over frequency

great flexibility in controller operation for various applications. A look-up tables (LUTs) alternative to the implemented controller enables determining the load VSWR and operation conditions of each power amplifier and adjusting the biasing conditions optimally to a large number of different circumstances. Because multiple sensors are employed, sensor errors changing with operating conditions (e.g. PVT and VSWR) can be greatly mitigated.

The individual PA output power and PAE versus frequency under nominal conditions are plotted in Fig.6. In the targeted phased-array system, output power is combined in space, with the total RF output power of 23dBm for the quad from a 3.2V supply and nominal antenna impedances of 50Ohm that are transformed using fully-integrated on-chip 2:1 transformer baluns. In-space power combining was experimentally verified by adjusting programmed output phases to maximize broadside radiated power. Taking into account PCB antenna gains and efficiencies, free-space performance compares well to simulations (within measurement error of 0.5dB). Amplitude control via the cascode voltages is shown in Fig. 7 for operation at 10.0, 10.25 and 10.5-GHz.

Phase-shifting performance of the integrated CMUs is verified by measuring steady-state output waveforms using a sampling oscilloscope as the effective 9-bit phase setting value is varied (for positive and negative signs). Zero-crossing times of the output signal can be varied by 140ps, providing phase control well in excess of 360° as shown in Fig.8 (including standard deviation). Measured output jitter is less than 500fs RMS when using a spectrum analyzer

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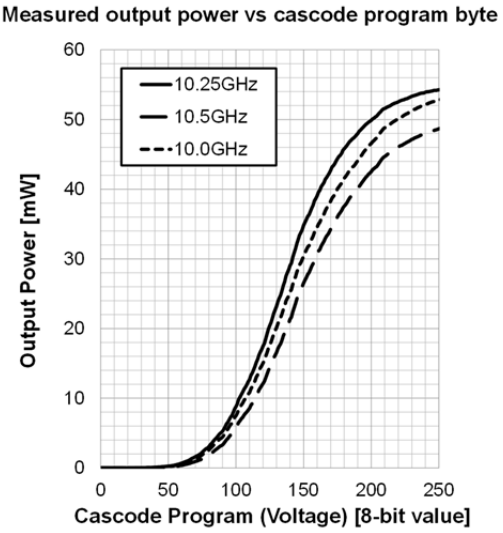

Fig.7: Measured output power over cascode voltage

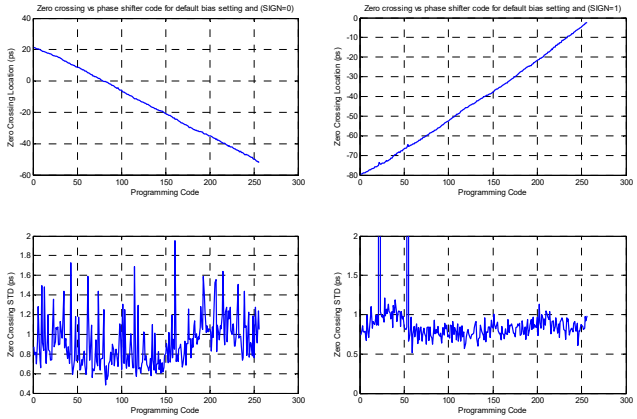

Fig.8: Measured relative signal zero crossing location and standard deviation versus phase program for positive (left) and negative (right) code settings. The absolute crossing times for a programming code of zero coincide for a total of 140ps of timing control.

Table I shows a performance summary and comparison to state-of-the-art CMOS PA implementations. It shows that the desirability of the proposed supply sharing and controller scheme for MIMO and phased-array applications.

In summary, the presented novel power amplifier supply sharing scheme is well suited for phased-array and MIMO applications for communications, sensing, ranging, and energy management systems.

ACKNOWLEDGMENT

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR WORK

Reference	Frequency [GHz]	Peak Output Power [dBm] [Stack/Cell]	Power supply [V] (stack/cell)	Peak PAE [%]	Peak Drain Efficiency [%]	Technology
1	5.0	26.7	3.3/3.3		25.3	65nm bulk CMOS
2	29	23.7	5.2/5.2	29		45nm SOI CMOS
3	5.9	22.2	1.2/1.2		49.2	40nm LP CMOS
4	10	22.8	4.8/4.8	25.7		45nm SOI CMOS
5	10	24.5	3.0/3.0	18		0.18u CMOS
6	9	20.3	2.6/2.6	28.9		0.11u CMOS
This work	10	23.0/17.0	3.2/0.8	37.0		65nm bulk CMOS