## 10.2 A 77GHz Phased-Array Transmitter with Local LO-Path Phase-Shifting in Silicon

A. Natarajan, A. Komijani, X. Guan, A. Babakhani, Y. Wang, A. Hajimiri

California Institute of Technology, Pasadena, CA

High output power and directionality are essential requirements for mm-wave transmitters used in broadband wireless communications, automotive radar, and remote sensing due to the considerable excess path-loss and lower effective antenna area at these frequencies. A phased-array transmitter provides a robust solution to the challenges of high-frequency power generation by increasing the effective isotropic radiated power (EIRP) due to its array gain properties. A silicon-based mm-wave transmitter can leverage the benefits of integration to realize a complex SoC with improved performance and reliability while lowering the overall cost. In this paper, a fully integrated 77GHz SiGe phased-array transmitter is presented that has 4 elements and utilizes a new *local* LO-path phase-shifting architecture to achieve electronic beam-steering.

A 2-step upconversion architecture is adopted in the transmitter, as shown in Fig. 10.2.1. Quadrature upconversion in the first stage attenuates the first image signal at the 26GHz IF while the image of the second upconversion step is sufficiently attenuated by cascaded tuned 77GHz amplifying stages. An on-chip 52GHz VCO generates the LO signal for the second upconversion stage while a quadrature injection-locked divide-by-two supplies the I and Q LO signals at IF for quadrature upconversion. The choice of the 26GHz IF allows for potential dual-band operation in both 24GHz and 77GHz radar bands [1] by bypassing the RF section for 24GHz operation.

The output of the quadrature upconversion mixers at 26GHz drives a pair of signal-distribution amplifiers, as shown in Fig. 10.2.1. The long interconnect length (of the order of the wavelength) can be a major barrier to reliable signal distribution at these frequencies. In addition to the large parasitics associated with these lines, radiation and coupling issues at mm-wave can pose further challenges to the design if not properly accounted for. To overcome these problems, on-chip differential microstrip tub transmission lines (t-lines) with well-defined characteristic impedances are used for high-frequency signal distribution throughout the chip. Optimal power transfer is ensured by matching the input and output of all high-frequency blocks to the characteristic impedance of the t-lines.

The IF outputs are upconverted to 77GHz by Gilbert-type differential upconversion mixers in each of the four elements. Each of the 77GHz mixers are followed by a driver stage (Fig. 10.2.2) that provides the input to the fully integrated +17.5dBm 77GHz PA, the details of which can be found in [2]. All circuits up to and including the RF mixers, are differential whereas the PA driver and the PA are single-ended due to area limitations and to facilitate output power measurement. Accordingly, one of the outputs of the mixer is terminated to 50Ω while the other output is fed to the driver whose input is also matched to 50Ω. In the mixer, the 100Ω differential impedance matching at the RF and LO ports is optimized for large signals to maximize the output power at 77GHz.

The four transmitter outputs are generated by on-chip PAs in each element. While the first three stages of each PA are designed for maximum gain, the output stage is designed for maximum efficiency. Each of the PAs is connected to an on-chip dipole antenna that can be trimmed out for direct electrical measurements via pads.

In the LO path, the output of the differential cross-coupled 52GHz VCO is distributed to the phase rotators in each element through a symmetric network of distribution buffers that ensures that the phase of the LO signal is the same at the input of the phase rotator in all transmit elements. Phase rotators in the LO path generate the desired phase shift for each element. This local phase generation scheme minimizes the number of t-lines carrying the 52GHz signal over long distances and enables the use of well-defined t-lines and power-matched LO-path buffers without excessive area and power penalties. Unlike the multi-phase distribution approach in [3], the local phase-shifting presented here does not suffer from additional coupling-induced phase errors and signal loss in the distribution path. Also, the phase shift resolution is limited by the DAC or the analog control voltage used to control the phase rotator.

The phase rotator generates the quadrature phase necessary for the phase interpolation by using a λ/4 t-line at 52.5GHz (Fig. 10.2.3). The lower emitter-degenerated differential pairs in each half of the phase shifters control the relative weights of the I and Q signals that are combined at the output of the phase shifter. Phase shifts from -180° to 180° can be achieved by providing the appropriate I and Q control voltages.

The chip performance is measured using a combination of waveguide-based probing and self-test mechanisms incorporated into the chip. At all high-frequency measurement points, the pads are absorbed into a tapered coplanar waveguide structure, thereby accounting for pad parasitics while maintaining the 50Ω impedance. For instance, both VCO and divide-by-two outputs are connected to such pad structures to enable direct measurement. The VCO can be tuned from 50.35GHz to 55.49GHz, while the locking range of the divider is from 51.4GHz to 54.5GHz which is sufficient for the intended application.

The transmitter is characterized using a waveguide probe that is followed by an external downconverter (with a 59GHz LO). The transmitter generates up to +12.5dBm output power and has 40.6dB of gain from baseband to 77GHz (Fig. 10.2.4) with a bandwidth of 2.5GHz.

The phased-array transmitter is implemented on the same chip as the 77GHz receiver [4], which allows for testing via an internal 77GHz *loopback* option. In the *loopback* mode, the output of the 77GHz upconversion mixer in a transmit element is connected to the input of the 77GHz downconversion mixer in a receive element. This option allows for TX and RX array patterns to be measured using baseband input-output, with no off-chip mm-wave connection. Figure 10.2.5 shows the measured patterns with 2 transmit-receive pairs active in the *loopback* mode which demonstrates the beam-forming capabilities of the transmitter.

The transmitter is implemented in a 0.12μm SiGe BiCMOS process with seven metal layers [5]. The transmitter and local phase-shifting portions occupy 17mm² of the 6.8mm×3.8mm transceiver chip (Fig. 10.2.6). The performance of the phased-array transmitter is summarized in Table 1 (Fig. 10.2.7).

*Acknowledgements:*
The authors thank S. Weinreb, D. Rutledge, and T. Yu for their assistance and support.

*References:*
[1] Federal Communications Commission, FCC 02-04, Section 15.253.
[2] A. Komijani, et al., "A Wideband 77GHz, 17.5dBm Power Amplifier in Silicon," *Proc. IEEE CICC*, pp. 571-575, Sept., 2005.
[3] H. Hashemi, et al., "A 24GHz SiGe Phased-Array Receiver-LO Phase Shifting Approach," *IEEE Trans. Microwave Theory and Techniques*, pp. 614-626, Feb., 2005.
[4] A. Babakhani, et al., "A 77GHz 4-Element Phased-Array Receiver with On-Chip Dipole Antennas in Silicon," *ISSCC*, Paper 10.1, Feb.. 2006.
[5] B. Jagannathan, et al., "Self-Aligned SiGe NPN Transistors with 285GHz $f_{MAX}$ and 207GHz $f_T$ in a Manufacturable Technology," *IEEE Electron Device Letters*, vol. 23, no. 5, pp. 258-260, May, 2002.

 

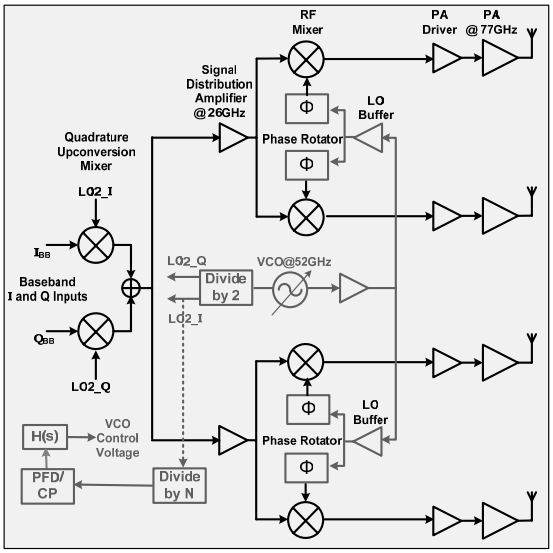


Figure 10.2.1: Architecture of 4-element 77GHz phased-array transmitter.

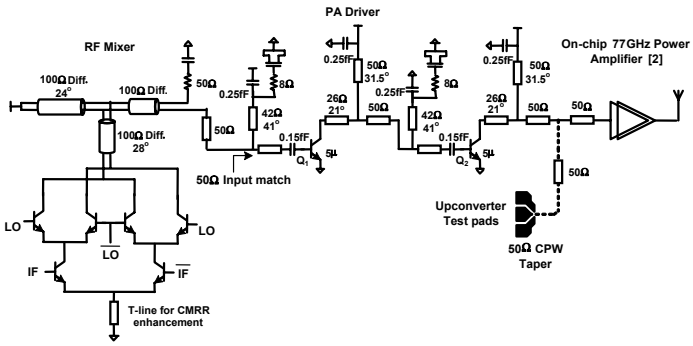


Figure 10.2 2: Schematic of 77GHz signal path in each element.



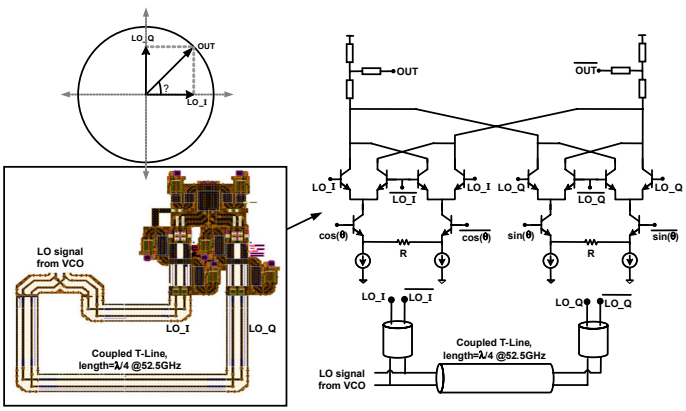


Figure 10.2.3: Schematic of 52GHz phase rotator in each element.

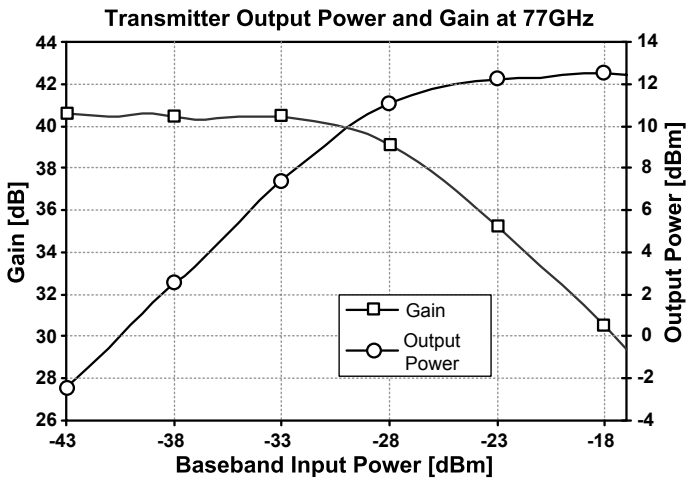


Figure 10.2.4: 77GHz transmitter gain and output power.

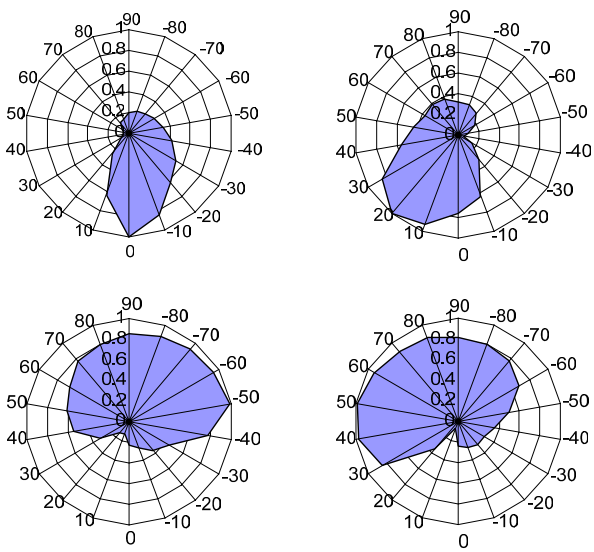

Figure 10.2.5: Measured 2-element loopback array pattern.

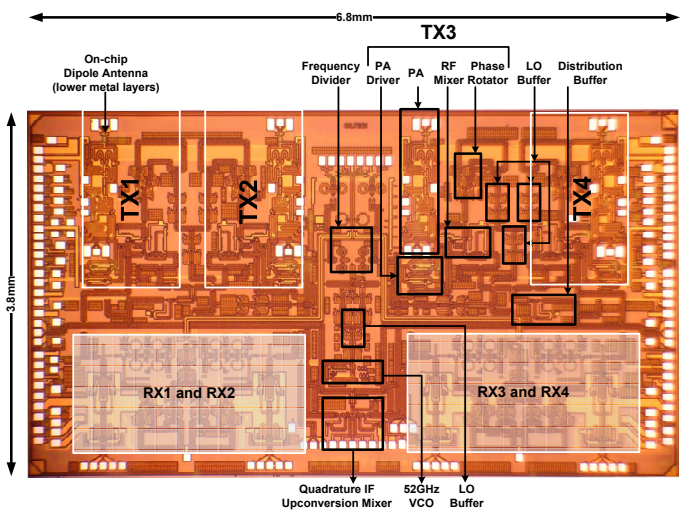


Figure 10.2.6: Die micrograph of 77GHz phased-array transmitter.

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| | |
|---|---|
| **Transmitter performance** | |
| Maximum output power | +12.5dBm |
| 4-element EIRP | +24.5dBm |
| Transmit 3dB-bandwidth | 2.5GHz |
| Gain | 40.6dB (single element) |
| Output referred 1dB compression point | +10.2dBm |
| Output 3rd-order intercept point (OIP3) | +18dBm |
| Image signal attenuation | > 20dBc (for first upconversion step)<br>> 30dBc (for second upconversion step) |
| LO leakage power | <-19dBc |
| **Transmitter power consumption** | |
| Signal path @ 77GHz | |
| PA and PA Driver (@1.5V) | 265mA (per element) |
| RF mixer and buffer (@2.5V) | 18mA (per element) |
| Distribution buffers and baseband mixers (@2.5V) | 46mA |
| **Phased array performance** | |
| Peak-to-null ratio (2-element *loopback*) | > 12dB |
| Beam-steering resolution | Continuous (limited by DAC resolution in practice) |
| VCO tuning range | 50.35GHz to 55.49GHz (9.6%) |
| Divider locking range | 51.4GHz to 54.5GHz (5.9%) |
| **LO-path power consumption** | |
| VCO and buffers (@2.5V) | 10mA |
| Analog divider core (@2.5V) | 3.1mA |
| Divider buffers/ LO path buffers (@2.5V) | 28mA and 12mA respectively |
| Phase rotators (@2.5V) | 14mA (each phase rotator) |
| 77GHz Transceiver Die size | 6.8mm x 3.8mm |
| Device Technology | 0.12㎜ SiGe BiCMOS |

**Figure 10.2.7: 77GHz phased-array transmitter performance summary.**

 