A 0.28 THz Power-Generation and Beam-Steering Array in CMOS Based on Distributed Active Radiators

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***Abstract*—In this paper, we present a scalable transmitter architecture for power generation and beam-steering at THz frequencies using a centralized frequency reference, sub-harmonic signal distribution, and local phase control. The power generation and radiator core is based on a novel method called *distributed active radiation*, which enables high conversion efficiency from DC to radiated terahertz power above $f_{\max}$ of a technology. The design evolution of the distributed active radiator (DAR) follows from an inverse design approach, where metal surface currents at different harmonics are formulated in the silicon chip for the desired electromagnetic field profiles. Circuits and passives are then designed conjointly to synthesize and control the surface currents. The DAR consists of a self-oscillating active electromagnetic structure, comprising of two loops which sustain out-of-phase currents at the fundamental frequency and in-phase currents at the second harmonic. The fundamental signal, thus gets, spatially filtered, while the second harmonic is radiated selectively, thereby consolidating signal generation, frequency multiplication, radiation of desired harmonic and filtration of undesired harmonics simultaneously in a small silicon footprint. A two-dimensional 4x4 radiating array implemented in 45 nm SOI CMOS (without high-resistivity substrate) radiates with an EIRP of +9.4 dBm at 0.28 THz and beam-steers in 2D over 80° in both azimuth and elevation. The chip occupies 2.7 mm x 2.7 mm and dissipates 820 mW of DC power. To the best of the authors' knowledge, this is the first reported integrated beam-scanning array at THz frequencies in silicon.**

***Index Terms*—Antenna, beam-scanning, CMOS, filter, frequency multiplier, millimeter wave power amplifier, on chip antenna, phased array, push-push, radiation, submillimeter wave, surface wave, Terahertz, traveling wave.**

I. Introduction

THERE has been a growing interest in the terahertz frequency range (0.3–3 THz) in the past few years for numerous applications ranging from ultrafast wireless communication, imaging, low-cost diagnostics to remote sensing, spectroscopy and quality control [1]–[4]. A major portion of the new applications are contingent on the availability of a low-cost technology in this frequency range, which is currently dominated by expensive and bulky optics, femtosecond and quantum cascade lasers, and compound III-V semiconductor processes. Silicon technology, especially CMOS, can fill this technology "vacuum". However, new techniques and innovations need to be developed to push current CMOS technology into the terahertz frequency regime, since the cut-off frequencies of most of today's technology nodes are in the sub-THz region.[1] In this paper, we propose a general design concept to efficiently generate, radiate and beam-steer at frequencies above $f_{\max}$ of a technology. The method is applicable to higher frequencies and scalable to larger number of elements in silicon or compound semiconductors alike.

The major challenges in realizing fully integrated THz sources in CMOS are efficient generation of THz signals with sufficient power on-chip and efficient extraction of the signal from the chip. The lower cut-off frequencies of CMOS compared to compound III-V processes of similar feature sizes imply that nonlinearities inherent in silicon integrated circuit technology need to be exploited to generate harmonic power above $f_{\max}$. However, low breakdown voltage, low quality factor passives and lossy filtering make on-chip generation and filtering of THz signals very challenging. Extracting the generated power from the silicon die is equally formidable. Classical antennas which work well in free-space, are not efficient radiators in silicon. When implemented in silicon, the substrate with its high dielectric constant acts as an excellent dielectric waveguide, trapping most of the radiated power into surface wave modes [5]–[9]. Mitigation of this problem requires expensive post-processing, external silicon lens or custom fabrication process options such as high-resistivity substrates [9]–[11]. Previous works have shown radiated THz power in CMOS in tens of nanoWatts of power, far too small to be of much practical use [12]–[15]. While interesting results on on-chip power generation with probe-based measurements have been reported in [16]–[19], [26], in this work, we will address the *generation* and *extraction* of the desired signal together, for the efficient conversion of DC into radiated THz signal.

In this paper, we present a scalable 4×4 element power-generation and beam-scanning 2D array in CMOS with near 10 dBm of Effective Isotropic Radiated Power (EIRP) at 0.28 THz and 80° of digitally controlled beam-scanning range in 2D space [20]. The architecture is shown in Fig. 1. The chip is implemented in a 45 nm CMOS SOI process with a typical $f_{\max} \sim$ 190–200 GHz [19], [21], [22].[2] In this paper, we

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[1]The Terahertz frequency is alternatively referred to as the sub-millimeter-wave frequency and technically extends from 300 GHz–3 THz.

[2]In [19], $f_{\max}$ is measured for a 30-μm-wide transistor with interconnects up to the top metal layer.

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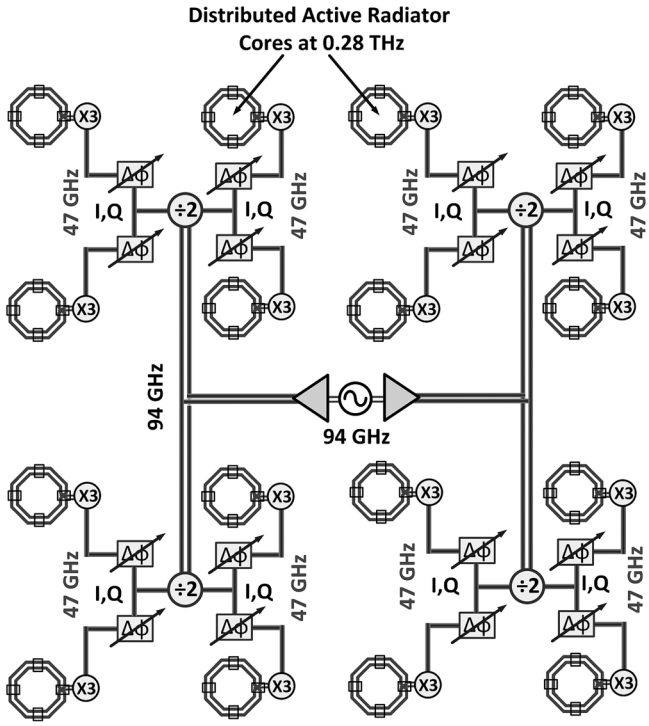

Fig. 1. Proposed scalable architecture of the integrated THz power generator and beam-steering array in CMOS.

propose an inverse design approach where we first formulate currents on metal surfaces in the silicon chip necessary to create the desired radiated THz far-fields, and then design actives and passives conjointly to synthesize, control and manipulate the formulated surface currents. This true circuits-electromagnetics co-design approach leads to the conceptual evolution of the power generating and radiating core in the array, which we call the *distributed active radiator* (DAR) [24], [25]. The DAR is an electromagnetic structure strongly coupled with actives, which achieves conversion of DC power into radiated power above $f_{\max}$, by consolidating signal generation, frequency multiplication, radiation of the desired frequency and free-space filtering of the undesired harmonics simultaneously. The active electromagnetic structure converts DC into a traveling wave oscillation at a design frequency and generates harmonic power due to distributed nonlinearities. Moreover, through a careful manipulation of currents at different harmonics, it suppresses fundamental signal radiation and allows the desired harmonic to radiate efficiently, by cancelling a major fraction of the surface wave power. As the paper will show, the structure is particularly suitable for array implementation for lossless power combination in air, high EIRP generation and electronic beam-scanning. The paper is organized as follows. Section II explains the challenges in terahertz power generation and radiation in silicon. Sections III and IV elucidate the conceptual evolution and design and optimization of DAR respectively. In Section V, we discuss the architecture for the beam-scanning array in CMOS, while circuits and building blocks are described in Section VI. The measurement results are presented in Section VII.

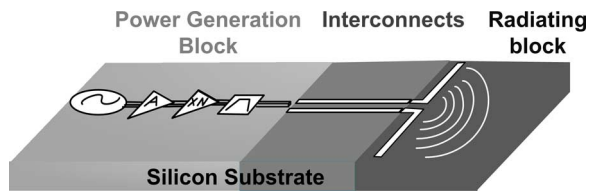

Fig. 2. A partitioned block-by-block approach to generation and radiation of power above $f_{\max}$.

II. Challenges of Terahertz Power Generation in Silicon: Partitioned Approach

As mentioned before, the two major challenges in realizing an efficient high power integrated terahertz source in silicon are signal generation and extraction from the silicon die. The relevant parameter to consider here is the *conversion efficiency from input DC power to total radiated Terahertz power and/or EIRP*.

The conventional approach, which we refer to as the partitioned approach, is illustrated in Fig. 2. This traditional design methodology separates the functions of *generation* and *extraction* into circuits and electromagnetics respectively. The circuit functionality is then realized using standard classical blocks such as oscillators, amplifiers, frequency multipliers, filters which are all designed separately and then interconnected through some combination of lumped passives, interconnects and transmission lines, as shown in Fig. 2. A self-sustained oscillator converts DC power into RF power below $f_{\max}$, which after amplification is frequency multiplied, filtered of all the undesired harmonics, and then propagated through a series of matching networks before getting radiated through a

tuned antenna. The partitioned approach with cascaded tuned elements does not scale well with frequency or output power. Higher output power will demand larger device sizes, which will make it prone to parasitic scaling, mismatches, modeling inaccuracies and frequency detuning. In addition, due to the significant loss in the matching networks, a substantial amount of fundamental and harmonic power is lost, while propagating from the signal source to the radiating element. An efficient mechanism of generating THz power onchip is only half the puzzle solved. The *extraction/radiation* of the generated signal from the chip is equally challenging. At these frequencies, wirebonds or flip-chip interconnects add unacceptable amounts of parasitics. Therefore, coupling it directly from the silicon die using on-chip radiative mechanisms is the most reliable way. However, silicon substrate, with its high dielectric constant ($\varepsilon_{\rm r} = 11.7$), acts as an excellent dielectric waveguide in its interface with air. It traps most of the radiated power into substrate modes which gets dissipated in the lossy silicon substrate (with bulk resistivity $\sim 10\,\Omega$-cm), reducing radiation efficiency drastically [5]–[9]. Therefore, if we assemble all the parts together in this block-by-block partitioned approach, the overall DC-radiated THz efficiency is likely to be sub-optimal. This is essentially because locally optimizing the design blocks forces us to work in an artificially created narrow design space and overlooks the innovations which may lie in a broader space [23].

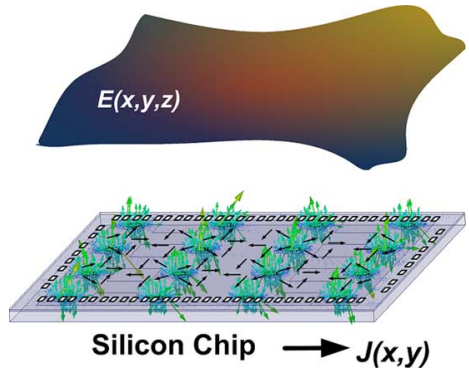

Fig. 3. A conceptual depiction of the inverse design approach: Formulate surface currents on metal in the silicon chip to create the desired field pattern and design passives and actives conjointly to synthesize, control and manipulate the surface currents.

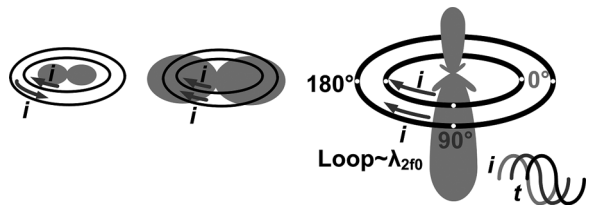

Fig. 4. Conceptual synthesis of fundamental and harmonic currents for free-space filtering of the fundamental signal and efficient radiation of the desired second harmonic signal.

III. Inverse Design Approach: Design Evolution of Distributed Active Radiator

At a higher level of abstraction, we are interested in generating radiated electromagnetic fields at THz frequencies of desired strength at a certain far-field distance. By Maxwell's laws, the radiated fields depend on the surface currents in the silicon chip. Silicon technology offers the capability of integration of very large number of high-speed transistors and layers of back-end-of-the-line metal stacks with fine lithographic resolution. Therefore, it may be possible to create complex current configurations and finely controlled electromagnetic field profiles, using a judicious combination of actives and passives, which may not otherwise be possible for a much constrained design space, such as a single-port passive antenna element or in a block-by-block design approach. This concept is illustrated in Fig. 3, where the surface current configuration in the silicon chip is initially formulated and then synthesized directly to create the desired near or far field profiles. The design evolution of the Distributed Active Radiator will follow this approach of inverse solution to Maxwell's equations and build up harmonic power generation and radiation mechanisms from basic principles.

A. Conceptual Synthesis of Fundamental and Harmonic Surface Currents in Silicon

Let us suppose that it is possible to build oscillations at a frequency f_0 near $f_{\max}$ and we would like to radiate the second harmonic $2f_0$ (above $f_{\max}$) by suppressing the strong fundamental and the other undesired harmonics. Instead of any passive filtering with lossy elements onchip, we would achieve this with almost no loss in free-space. Two current elements which are out-of-phase, placed very closely to each other, cancel their radiated fields and therefore, constitute a poor radiator or a filter, as shown in Fig. 4. This is primarily the reason why on-chip transmission lines are poor radiators, since the forward and return currents, being out-of-phase and closely placed, cancel their individual radiated fields. However, if the currents are in-phase, they add up their radiated fields. Small loops are, however, inefficient radiators and their radiation plane lies in the plane of the loop, which is not suitable for an efficient onchip antenna. If we expand the loops such that their circumferences equal the wavelength at the desired radiation frequency of $2f_0$, then we have two loops sustaining two traveling waves at $2f_0$, which propagate and radiate in phase along the broadside direction and complete 360° in one loop traversal (Fig. 4).

B. Active Synthesis of Currents for the Desired Harmonic Radiation

In order to sustain traveling waves at $2f_0$ which constantly lose power through radiation, currents at $2f_0$ are injected at appropriate phase progression of 0°, 90°, 180° and 270° into the loops, at equi-spaced positions,[3] to maintain the total phase change of 360° over the loop, as shown in Fig. 5. Common-mode second harmonic currents $(2f_0)$ above $f_{\max}$ are generated by driving transistor pairs differentially at the fundamental frequency $f_{\rm o}$ $(< f_{\max})$ into strong nonlinear regime. As illustrated in Fig. 6, transistor pairs are driven differentially at f_0 at 0° and 180°, 45° and 225°, 90° and 270°, and 135° and 315° to generate common mode $2f_0$ drain currents at 0°, 90°, 180° and

[3]We consider the case of four current injection ports, but there can certainly be more injection currents at the appropriate phases distributed over the loop.

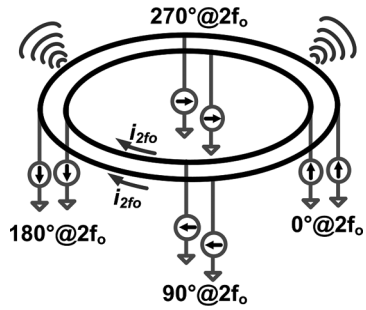

Fig. 5. Second harmonic current pumped in the appropriate phase progression to maintain in-phase traveling and radiating waves in two adjacent loops.

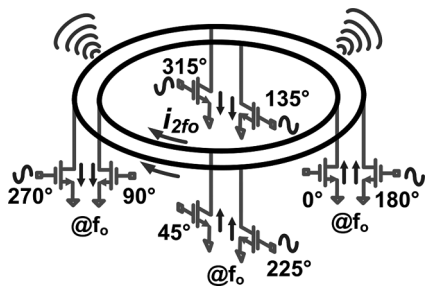

Fig. 6. Pseudo-differential pairs driven strongly at the first harmonic to create in-phase second harmonic currents pumped into the distributed radiating loops.

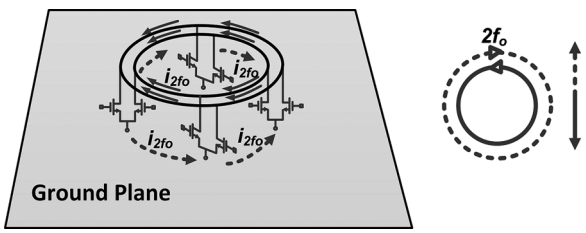

Fig. 7. The second harmonic return current from the actives channelized through a ground plane. The return currents on the ground are out of-phase with the forward currents on the loop, cancelling most of the radiated fields.

270° respectively. Section III-C will elaborate on the method for generation of the driving signal at f_0 at the required phase progression, but for now, we assume that such a synthesis is possible. In summary, if transistor pairs were driven differentially at the appropriate phase progression as shown in Fig. 6, it is possible to sustain traveling waves at the second harmonic $2f_0$ on both the loops, which propagate and radiate in phase.

However, as can be seen in Fig. 6, the second harmonic currents are common mode and in order to close the current loop, a return path has to be provided from the source to the sink. The radiative mechanism of the traveling wave loops can be understood by analyzing the entire current configuration at $2f_0$ including the return path through the transistor pairs. If this path is provided by a ground plane as shown in Fig. 7, then the loops will essentially behave like microstrip lines for all frequencies and therefore be poor radiators.[4] The forward propagating $2f_0$ currents on the loops and the return out-of-phase currents on the ground plane will cancel each other's radiated fields. It is apparent that the path of the return current with respect to the forward propagating wave decides how the radiated fields interfere. *We, therefore, turn the transmission line behavior into radiative behavior by modifying the manner in which the return current flows.*

[4]Fig. 7 shows the instantaneous current flow for a traveling-wave full-wavelength loop (not the direction of wave propagation). With time, the current and the electromagnetic field configuration rotate about the broadside axis.

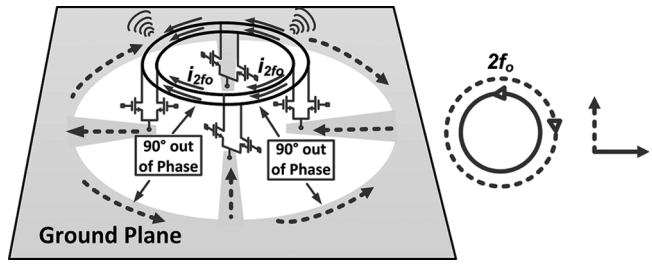

Fig. 8. The second harmonic return current from the actives channelized through a longer path through a ground aperture plane, creating a 90° phase difference between forward and return path. The radiated fields of two concentric loops add in quadrature in free-space, simultaneously achieving high radiation efficiency and high conversion efficiency, as shown later in Fig. 11.

Fig. 8 illustrates the concept. The return currents are forced outwards by creating a ground aperture opening, which channelizes the return current through an extended path length. As shown in Fig. 8, this creates a phase rotation between the forward current on the loop and the return current through the ground plane, determined by the radius of the ground aperture opening. Section IV will discuss the optimum choice of the aperture radius for maximum second harmonic power generation and radiation. In the implemented design, the optimum radius induces nearly 90° phase difference between the forward current on the loop and the return current through the ground plane. Therefore, instead of two out-of-phase currents cancelling their radiated fields in a microstrip line in Fig. 7, the radiated fields of the forward and return path are now in phase-quadrature and they add up their power in space (Fig. 8). It can be noted that the power at $2f_0$ injected by the transistors immediately gets radiated through the second harmonic traveling waves. This eliminates the usual propagation loss incurred in the matching networks and filters from the source of generation to the location of radiation in a traditional design approach (Fig. 2).

C. Distributed Active Radiation: Complete Chain of DC-radiated THz Conversion

We will now address the generation of multi-phase drive signal at f_0 at the gates of the pseudo-differential pairs. *We generate the drive signal at f_0 and all the required poly-phases from the radiating loops themselves*, thereby achieving a complete DC- radiated $2f_0$ ($> f_{\max}$) conversion.

In order to create a differential swing at the gates we cross couple the transistors and crisscross the loops into a Mobiüs strip as shown in Fig. 9. This creates a condition where traveling wave oscillation sets up at a fundamental frequency f_o, such that the total loop phase is 180° [27]. The loops act as differential transmission lines for f_o and all its odd-harmonics. The adjacent forward and return currents are out-of-phase and they cancel the radiation at the fundamental frequency of oscillation f_o and at all its odd-harmonics. As the fundamental wave propagates and creates a differential swing at the gates of the actives, second harmonic currents at $2f_o$ are injected in phase in both the loops and they radiate in the traveling-wave mechanism as described in Sections III-A and III-B. In summary, as soon as the transistor pairs are properly biased through

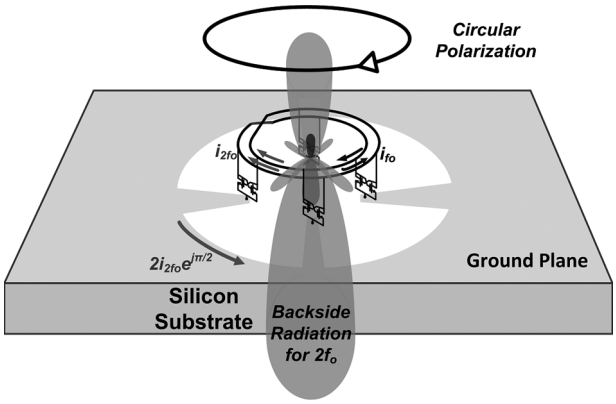

Fig. 9. Distributed Active Radiator: Electromagnetic structure strongly coupled with actives achieving signal generation from DC, frequency multiplication, efficient radiation of desired harmonic and free-space filtering of undesired harmonic simultaneously.

the cross-connected loop, a strong and filtered second harmonic signal at THz frequency couples to the aperture, finds the least impedance path through the high dielectric silicon substrate and radiates out from the backside. The fields are circularly polarized due to the traveling wave nature. Due to active synthesis and manipulation of harmonic currents, *the same loop acts as a transmission line for f_o and a distributed radiator for $2f_0$*, leading to a high DC-radiated THz conversion efficiency. The distribution of active devices over the loop allows power combination of multiple sources, while reducing effects of parasitic scaling. The details of design issues and novel radiative properties will be discussed in the next section.

IV. Design and Optimization of DAR

The DAR achieves four functions such as signal generation from DC, frequency multiplication, filtering and radiation simultaneously through a careful control of harmonic currents. The design of the structure, however, can be partitioned into a logical step-wise procedure.

A. Fundamental Frequency of Oscillation

The frequency of the traveling-wave oscillation is set by the length of the loop and the capacitive loading of the transistors. At the fundamental frequency, the loop behaves like a differential transmission line of characteristic impedance say Z_0, which is periodically loaded with differential capacitance of the cross-coupled pairs say C_0. Therefore, the phase shift θ experienced by the fundamental frequency f_0, through a unit section of t-line of length l loaded in the center with capacitance C_0, is given by

$$\cos(\theta) = \cos(\beta_0 l) - \pi f_0 C_0 Z_0 \sin(\beta_0 l) \tag{1}$$

where β_0 is the propagation constant of the unloaded transmission line at frequency f_0. The dispersion directly affects the propagation of the fundamental frequency and the odd-harmonics for which the structure behaves like a transmission line. The second harmonic signal injected by the actives, however, does not see a t-line, but a distributed radiative structure, whose properties are dependent on the aperture and the ground plane configuration which carries the return current (Fig. 8). In this design, four cross-coupled pairs are distributed over the DAR, as illustrated in Fig. 9. The pairs consist of 7.5-μm-wide transistors which results in a differential $C_0 \approx 16$ fF. The spacing of the loops in the DAR are chosen to be 5 μm on the top 2.1-μm-thick Al layer, leading to a $Z_0 \approx 100\ \Omega$. With these parameters, the mean diameter of the two loops in the DAR can be derived to be 85 μm (from (1)) for a desired fundamental frequency of oscillation of 140 GHz. As shown in Fig. 10, at the fundamental frequency of oscillation, each cross-coupled pair essentially sees a resonator with a quality factor of the differential transmission line i.e, $Z_{f0} = Z_{\rm osc} = R_{\rm osc} + j\omega L_{\rm osc}$, where the differential inductance $2L_{\rm osc}$ resonates with C_o at f_0 and $R_{\rm osc}$ is contributed by the ohmic loss of the differential t-line and residual radiation loss.[5]

B. Ground Plane Aperture and Optimum Impedance Matching

The differential swing at the fundamental frequency creates in-phase second harmonic currents I_{2f0} due to transconductance and capacitance nonlinearity as shown in Fig. 10. The drain of each transistor sees a radiative impedance $Z_{2f0} = Z_{\rm ant} = R_{\rm ant} + j\omega L_{\rm ant}$, where $R_{\rm ant}$ represents the radiation resistance of the DAR, which results in second harmonic power radiating out of the chip. For maximum second harmonic power generation, there exists a optimum load-pull impedance at $2f_0$ at the drain of each transistor. This radiative impedance $Z_{\rm ant}$ (as well as the radiation efficiency of the DAR) is a function of the aperture diameter. This is illustrated in Fig. 11. In the limiting case, when the aperture diameter tends towards zero, the structure becomes similar to Fig. 7. The loop segments then behave like t-line based inductors (impedance phase is near 90°) and radiation efficiency reduces to near zero, as can be seen in Fig. 11. If the aperture radius is too large, the inductance of the connecting leads affects the second harmonic power generation. In this approach of circuits and electromagnetics co-design, the aperture is designed so as to present the optimum load pull impedance $(145 + 235\mathrm{j}\,\Omega)$ for the maximum second harmonic power generation for the choice of the device sizes. As shown in Fig. 11, the radiation efficiency (backside radiation), for this choice of aperture radius (70 μm) attains a near maximum of 35% for the entire 4×4 array on a 250 μm silicon substrate. Due to the rotational symmetry of the DAR, all transistors see the same impedance at the fundamental frequency and all its harmonics. This approach of circuit and electromagnetic co-design removes the necessity for a separate matching network. The radiated second harmonic power per DAR can be calculated as

$$P_{\rm radiated,2f0} = 4\eta_{2f0} {I_{2f0}}^2 R_{\rm ant} \tag{2}$$

[5]It should be noted the effective impedance that one-cross-coupled pair sees cannot be analyzed in isolation and the simultaneous behavior of the other cross-coupled pairs have to be taken into account Therefore, the $\rm L_{osc}$ referred in Fig. 10, is the net effective impedance seen as a result of the traveling wave currents injected at the appropriate phase-progression by all the cross-coupled pairs. The frequency of other traveling modes exceeds $f_{\rm max}$ and are thereby naturally suppressed. The other possible modes such as standing-wave modes are suppressed by carefully choosing the locations of the cross-coupled pairs. As can be seen in Fig. 19 (or Fig. 10 or Fig. 14), a cross-coupled pair has been positioned at the cross-over of the two loops. In a standing-wave pattern, the cross-over point will be a virtual ground and the presence of the cross-coupled pair makes that mode unstable.

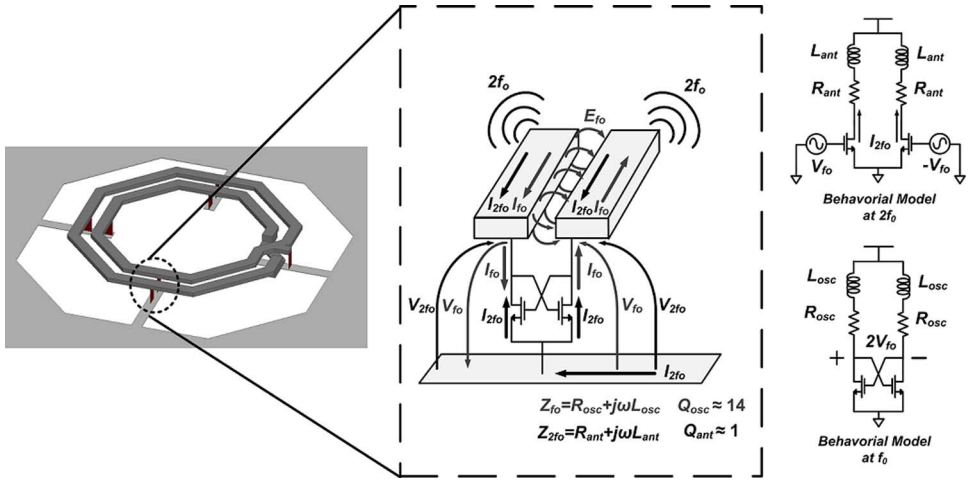

Fig. 10. The electromagnetic simulation structure of DAR with eight ports. Harmonic currents are designed to flow in such a way that each transistor, in the cross-coupled pair, sees a resonator at the fundamental frequency and a radiative impedance at the second harmonic.

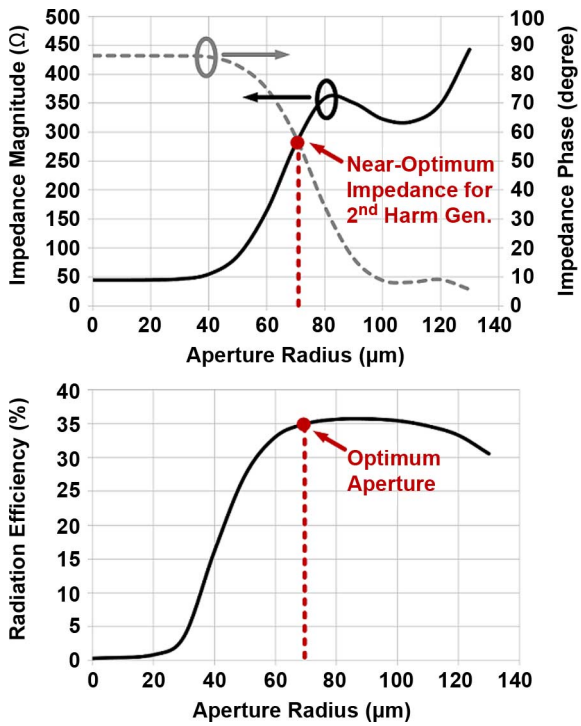

Fig. 11. The upper figure shows the variation of second harmonic radiation impedance (seen by each transistor in a cross-coupled cell) with the ground plane aperture radius. The lower figure shows variation of radiation efficiency (backside radiation) with the ground plane aperture radius for the 4×4 array chip on a 250-μm-thick substrate.

where the simulated radiation efficiency $\eta_{2f0} \approx 35\%$ and I_{2f0} is the amplitude of the second harmonic current injected into the DAR (Fig. 10). In order to calculate the fundamental power suppression, the total radiated power at f_0 can be enumerated as

$$P_{\text{radiated},f0} = 4\eta_{f0} {I_{f0}}^2 R_{\text{osc}} \tag{3}$$

where the simulated radiation efficiency $\eta_{f0} \approx 0.1\%$ and I_{f0} is the amplitude of the fundamental frequency current injected into the DAR.

An electromagnetic and circuit co-simulation is necessary to capture the signal generation, frequency multiplication, radiation and filtering effects simultaneously. As shown in Fig. 10, a 3D electromagnetic simulation with eight ports is carried out, where the ports signify the terminals of the cross-coupled pairs. A finely swept S-parameter simulation output, upto a few harmonics of the fundamental frequency, is exported to spectre-RF simulator and a harmonic balance analysis is carried out with the extracted models of the negative g_m-cells. This captures the self-sustained oscillation and currents and voltages of higher harmonics and also gives the total first and second harmonic power injected into the DAR. The electromagnetic simulation is revisited with the magnitude and phases of current injections at different harmonics to ascertain the radiation efficiency, radiation patterns, total radiated power and EIRP. The entire design is compliant with CMOS design density rules.

C. Radiation Properties, Bandwidth and Comparison With Classical Antennas

We will briefly review some electromagnetic properties of DAR and compare power generation and radiation mechanisms with other classical topologies and antennas. A well-known harmonic generation topology is a push-push oscillator where the second harmonic power is tapped from the common-mode point, as shown in Fig. 12 [13]. The second harmonic currents, generated by the transistors, have to flow through the inductor (in the resonator) before they reach the antenna. In addition to the ohmic loss suffered in the resonator, this also affects the second harmonic power matching, necessitating a separate matching network at the center-tapped point, as shown in Fig. 12. In a DAR, the resonator for f_0 behaves as a radiator for $2f_0$, and therefore, the second harmonic power gets immediately radiated out as soon as it is generated. Effectively, in a DAR, the resonator is transparent to the second harmonic current I_{2f0}, as illustrated in Fig. 12.

Further, impedance matching and performance sensitivity to process variations, parasitic mismatches and modeling inaccuracies are critical at these frequencies. Due to the traveling

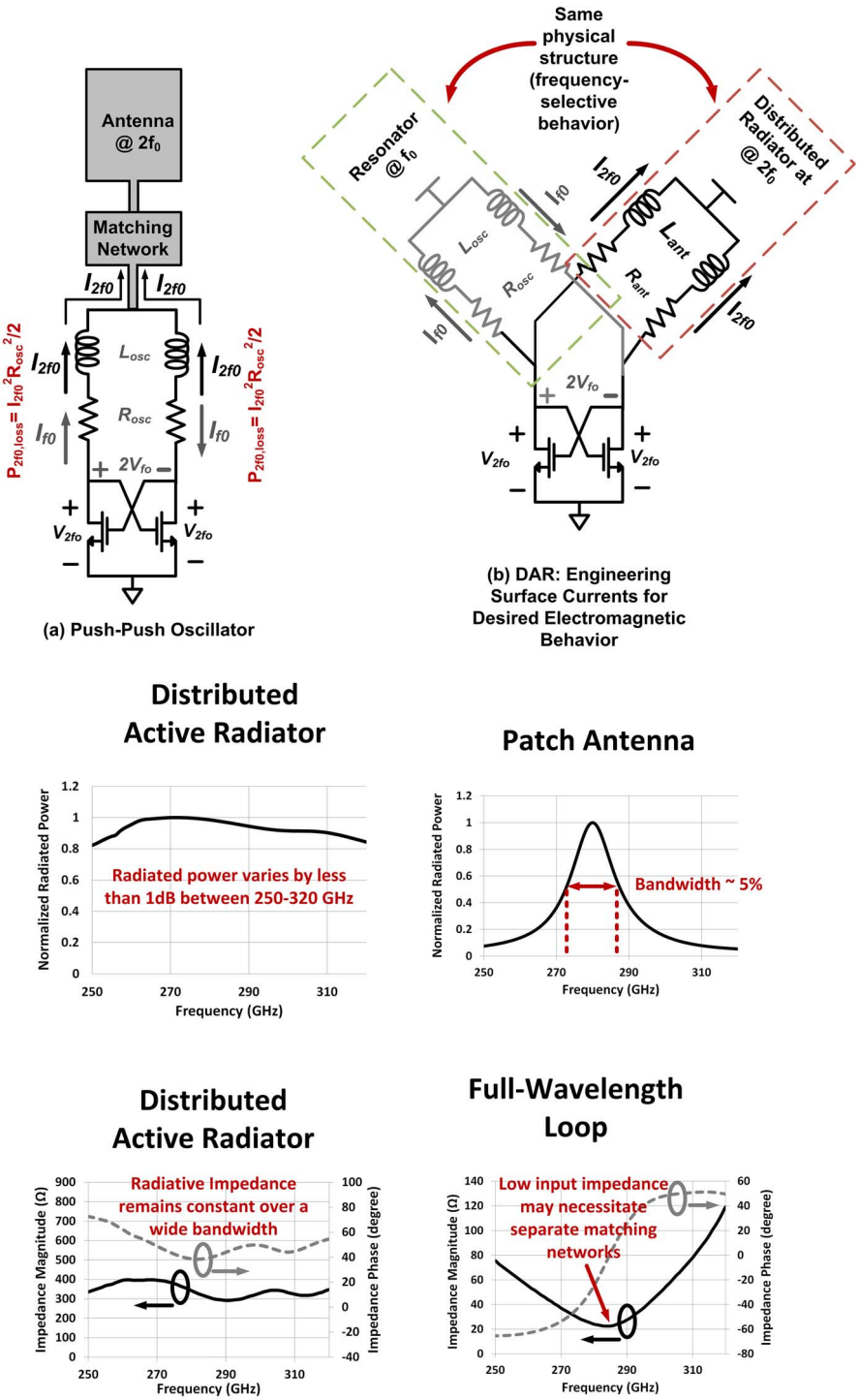

Fig. 12. Comparison of power generation and radiation properties of DAR with other classical harmonic generation and radiation mechanisms. (a) Push-push oscillator. (b) DAR: engineering surface currents for desired electromagnetic behavior.

wave nature of the radiator and multi-phase pumping, the current distribution on the loop does not sustain any maxima or null at the central frequency. Moreover, over a wide range of input frequencies of the injected currents, no sudden or sharp nulls develop along the loop. Consequently, the input impedance at the second harmonic remains fairly constant over a large bandwidth, as shown in Fig. 12. It can be see that even though the DAR is optimally matched near 280 GHz, the simulated radiated power varies by less than 1 dB over a 70 GHz bandwidth between 250–320 GHz. The range of the impedances for typical device sizes at these frequencies is very suitable for traveling-wave DAR architecture. A classical full-wavelength loop antenna, on the other hand, may present a very low input impedance due to the standing-wave current maxima at the input, as shown in Fig. 12. Additionally, since the resonator and radiator are the physically the same structure

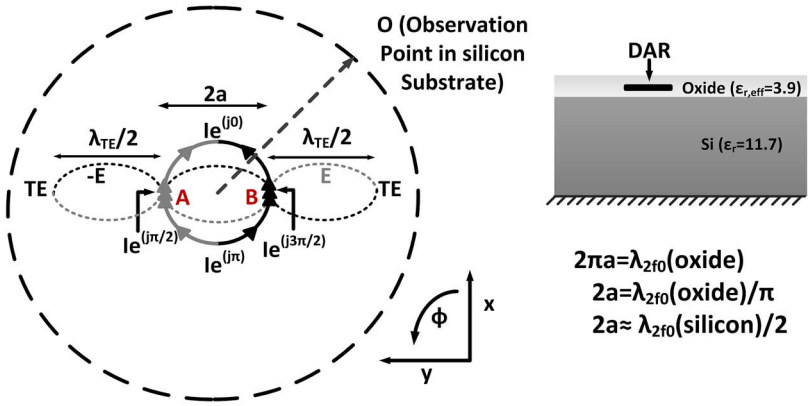

Fig. 13. Illustration of suppression of TE_0 surface wave mode in a full-wavelength traveling wave radiator, which is one of the two dominant surface wave modes for a substrate height of 250 μm. The other TM_1 is suppressed by spacing the array elements near $\mathrm{TM}_1/2$.

in a DAR, process variations and modeling inaccuracies affect the properties at fundamental frequency of oscillation and the second harmonic in correlated fashion. Due to parameter variations, if the frequency of oscillation shifts, the second harmonic currents will be still be pumped at the right phase progression. This makes the radiated power less sensitive to process variations. Comparatively, a classical onchip patch antenna can suppress surface wave excitation with a ground shield, but typically suffers from narrow bandwidth due to close spacing ($\sim$ 10 μm between the patch and the ground plane). A typical performance over frequency is shown in Fig. 12. There are design methodologies that extend the bandwidth, but in general, a patch antenna is a highly resonant structure, which makes the power generating element connected to the patch antenna sensitive to parameter variations.

A full-wave length traveling wave antenna also suppresses surface-wave excitation in the silicon substrate to a large extent. One full-wave length traveling wave radiator, with its current flow at one instant of time, placed over a finitely thick silicon substrate is shown in Fig. 13. As the wave travels around the loop, the current distribution and electromagnetic field configuration in the silicon substrate simply rotate about the broadside axis. This implies that the surface-wave power, excited by the radiator, is radially symmetric and independent of the angle of observation ϕ. Therefore it is sufficient to analyze the field configuration at any given instant of time. It can be shown that for a silicon substrate thickness of 250 μm with a ground shield on one side, the dominant surface waves for an infinitesimal current element are TE_0 and TM_1 contributing to 90% of the total surface wave power at the central frequency of 275 GHz [5]. The principle of substrate mode cancellation for a full-wavelength traveling-wave DAR relies on surface waves excited by one part of the loop cancelling that of the other part. The concept is illustrated in Fig. 13. For the instant of time shown, the instantaneous current maxima are located at $\phi = 90^\circ$ (A) and $\phi = 270^\circ$ (B). One of the dominant modes, the TE_0 mode, has maximum power-flow perpendicular to the direction of current [5]. Therefore if the radius of the loop is so adjusted, that the strongest current elements at A and B are near $\lambda_{\mathrm{TE}_0}/2$ apart,[6] then the TE_0 surface waves, excited by each of them, can be made to destructively interfere, canceling major portion of the mode power. However, as discussed in Section IV-A, the circumference of the traveling-wave loop is set by the fundamental frequency of oscillation, where it behaves like a transmission line embedded in the oxide layer, as shown in Fig. 13. For a loop phase of 180° at f_0, the loop diameter satisfies $2\mathrm{a} = \lambda_{2f0}(\mathrm{oxide})/\pi$.[7] Because of the ratio of effective dielectric constant between the oxide layer and silicon substrate ($\varepsilon_\mathrm{r}(\mathrm{oxide}) : \varepsilon_\mathrm{r}(\mathrm{silicon}) \approx 3.9 : 11.7$), this relation also implies that $2\mathrm{a} \approx \lambda_{2f0}(\mathrm{silicon})/2$. More precisely, the oscillation condition near 140 GHz requires $2\mathrm{a} = 175$ μm in the oxide layer, which also corresponds approximately to the near-optimum spacing of $\lambda_{\mathrm{TEO}}/2 = 186$ μm for the TE_0 mode cancellation in a 250 μm silicon substrate. A theoretical electromagnetic field analysis shows that more than 90% of the TE_0 power can be suppressed in such a way in a DAR. In the implemented design, where the loop diameter is reduced due to parasitic capacitances of the transistors, nearly 50% of the TE_0 mode power is still suppressed. The principle of cancellation also holds for other TE modes whose wavelengths are close to the TEM wavelength in bulk.[8] The remaining dominant surface-wave mode is the TM_1 mode with $\lambda_{\mathrm{TM1}} = 755$ μm. While the ideal DAR element spacing for TM_1 suppression is near $\lambda_{\mathrm{TM1}}/2$, the elements are placed at separations of approximately $\lambda_{\mathrm{air}}/2$ (≈ 500 μm) for a higher directivity and larger beam-scanning range, while still suppressing most of power leaked in the TM_1 mode. In summary, two of the dominant modes TE_0 and TM_1, are suppressed in a DAR array, leading to higher radiation efficiency and clean pattern for a typically thick silicon substrate of 250 μm.

D. Bias Network Design

The V_{dd} supply to the actives in the DAR is provided with a t-line network which is shown in Fig. 14. The network presents an open circuit impedance at both the fundamental and second harmonic so as not to load the DAR and affect its operation. At the fundamental frequency of f_0, the DAR sees a resultant

[6]In reality, due to the contribution to the other instantaneously less strong current elements distributed over the loop, the optimum spacing for TE mode cancellation is approximately $0.55\lambda_{\mathrm{TE}}$.

[7]$\lambda_{2f0}(\mathrm{oxide})$ and $\lambda_{2f0}(\mathrm{silicon})$ refer to TEM wavelengths in oxide and silicon; $\lambda_{2f0}(\mathrm{oxide}) = \lambda_{2f0}(\mathrm{air})/\sqrt{\varepsilon_\mathrm{r}(\mathrm{oxide})}$ and $\lambda_{2f0}(\mathrm{silicon}) = \lambda_{2fo}(\mathrm{air})/\sqrt{\varepsilon_\mathrm{r}(\mathrm{silicon})}$.

[8]The TE mode wavelength tends towards that of the TEM mode at higher frequencies or thicker substrates.

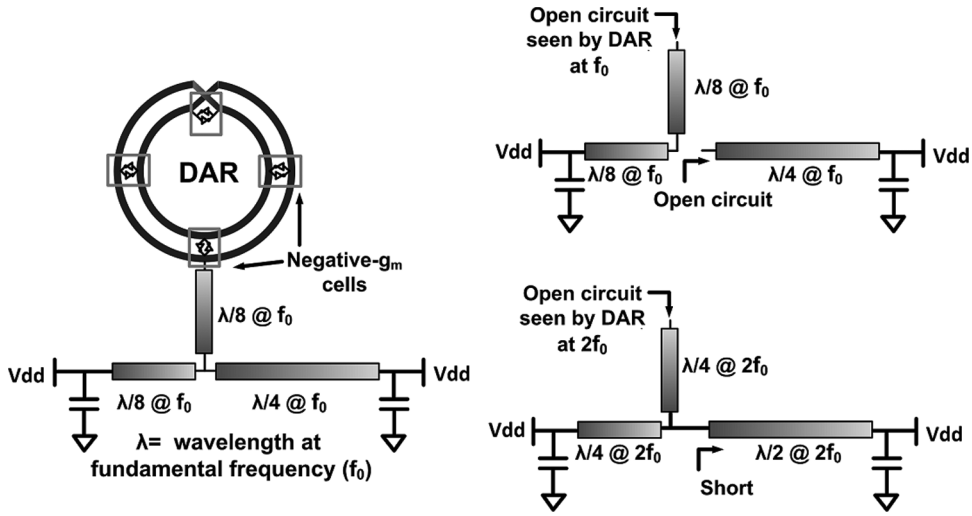

Fig. 14. The transmission-line network providing V_{dd} supply to the actives in the DAR without loading the DAR operation either at the fundamental frequency or at the desired radiation frequency of $2f_0$.

$\lambda/4$ shorted t-line stub due to the two $\lambda/8$ t-lines in series. At $2f_0$, the DAR seeing a resultant open-circuit presented by a $\lambda/8$ ($@$ f_0) and therefore $\lambda/4$ ($@$ $2f_0$) shorted t-line stub. The transistors were biased at their maximum $f_{\max}$ current density of 0.3 mA/μm, resulting in each DAR drawing nearly 20 mA of DC current.

V. Distributed Active Radatior Beam-Scanning Architecture at 0.28 THz

In the previous section, we showed distributed active radiation to be an efficient method of conversion from DC-THz power. In order to generate higher power and higher EIRP, arrays of such structures can be coherently locked to each other, so that the radiated signals combine coherently in free space without incurring onchip combiner losses. The total radiated power and EIRP scale as N and N^2 respectively, where N is the total number of array elements. Such an array realization also enables us to perform electronic beam-steering in space, by introducing individual phase control in each of the radiating elements. It is challenging, however, to synchronize multiple such autonomous radiating structures distributed across the chip, for coherent power combination. In [24] and [25], mutual synchronization networks using transmission lines [24] and nearfield coupling [25], were demonstrated in 2×2 arrays of DARs. The final frequency of oscillation of such a mutually injection locked system is determined by the common oscillation frequency of individually free-running oscillators [28]–[30]. In a practical system, we may often desire a central frequency reference controlling the frequency of the transmitted beam. Also in a mutually locked setting, it is difficult to scale the array to a large number of elements. In this paper, we present a scalable power-generation and beam-steering architecture with a central frequency reference, compatible to phase and frequency locking to a low frequency source.

The beam-scanning and power generation architecture is shown in Fig. 1. The key element in the overall architecture is that desired harmonic power is generated locally and radiated immediately. This happens at the front-end of the transmitter in the individual DARs, enabling high conversion efficiency from DC-THz. Therefore, the architecture simply enables a scalable frequency and phase control of the individual DARs and is not based on propagation of harmonic power from the source of generation through multipliers chains, matching networks, filters and antenna elements.

As shown in Fig. 1, a central frequency reference, constituted by an onchip VCO with differentials buffers, distributes signals to the entire chip at subharmonic frequencies to minimize losses in signal distribution. The VCO is tunable around 94 GHz with a 6 GHz tunable bandwidth. The central frequency of oscillation is one-third of the frequency of final radiated signal at 0.28 THz. The buffers distribute the 94 GHz differential signal to four symmetric junction points on the chip through impedance matched differential transmission lines with equal delays, as shown in Fig. 1. The t-lines at the four junction points are terminated by single-ended injection-locked divide-by-two blocks. The frequency dividers convert the differential signals at 94 GHz into differential quadrature signals, I and Q at 47 GHz for phase-rotation. An alternative approach would have been to generate the quadrature signals at 47 GHz centrally, and then distribute the four signals across the chip. However, this would have required simultaneous differential I and Q routing with good isolation which is difficult to achieve with area constraints.

The quadrature signals at 47 GHz can now be added with different weights to generate 16 independent phase-rotated signals at 47 GHz, each of which gets frequency and phase-locked to the 16 DAR cores. This facilitates control of phase of the radiated signal from each of the individual cores and enables beam-forming and beam-steering in 2D space. The outputs of 16 such phase rotators drive 16 injection-locked frequency triplers which are tuned at 140 GHz, each of which are locked to the fundamental frequency of oscillation of the DARs. Since the DARs only radiate the second harmonic, the chip generates and radiates power at 280 GHz. Therefore the phase rotation, say θ, induced at 47 GHz gets translated to 6θ at the radiated frequency of 280 GHz.

The signal distribution across the chip at mm-Wave frequencies is enabled through transmission lines, which are carefully

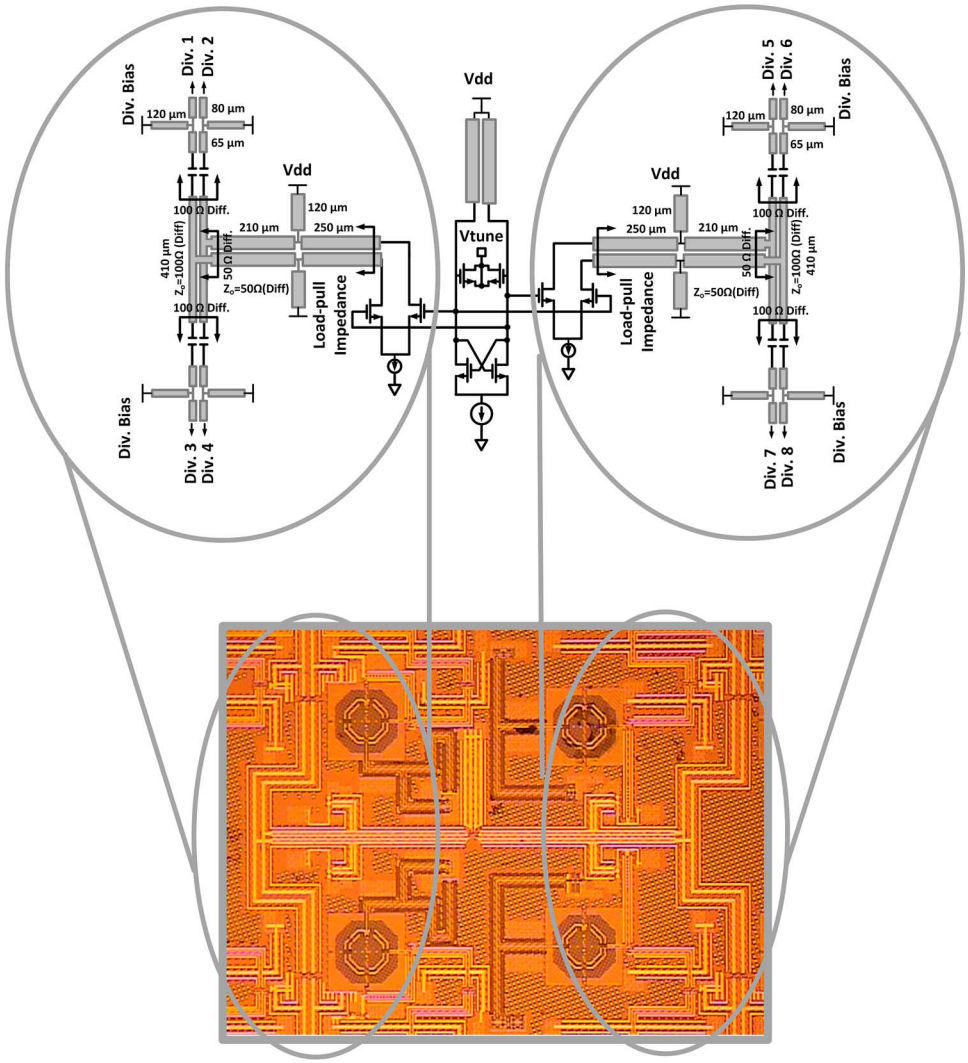

Fig. 15. The central VCO with differential buffers and the LO distribution with matching transmission-line driving 8 divide-by-two blocks.

modeled using 3D electromagnetic simulations. Since the load impedances are dependent on length of the t-lines, the input to the circuit blocks, such as divide-by-two and the frequency triplers, are matched to the characteristic impedance of the interconnect t-lines, details of which will be discussed in the following section. This decouples the design of the output matching network of the previous stage with the exact placement and layout of the succeeding blocks. The preceding circuit blocks, such as the oscillator buffers and the phase-shifters, drive load-pull impedances that ensure maximum power transfer to the succeeding blocks, such as the divide-by-two and the frequency triplers.

VI. Transmitter Circuit Blocks

A. 94 GHz Voltage-Controlled Oscillator and Buffers

The central VCO is realized as a cross-coupled pair with a differential t-line based inductor as shown in Fig. 15. The cross-coupled pair consists of two 12-μm-wide transistors (1-μm-wide fingers), biased at 0.4 mA/μm for a total current of 9.6 mA from a 1 V supply. The differential inductance of 38 pH is realized with coplanar strip lines placed in a ground tub which shields the lossy silicon substrate. The t-line is realized on 1.2-μm-thick copper metal and has simulated quality factor of 14 at 94 GHz. The varactors are realized with 32-μm-wide NMOS transistors (1-μm-wide fingers) and the VCO has a tunable frequency range of 6 GHz.

The buffers draw 11 mA each from a 1 V supply and drive load-pull impedance for maximum power transfer to the succeeding frequency dividers. As can be shown in Fig. 15, the inputs of the divide-by-two blocks are matched to 100 Ω differential impedances, which get translated to 50 Ω by matched transmission lines at the split junction. Through the t-line shunt-series matching network, this impedance is transformed to the differential load pull impedance, for maximum power transfer by the buffer, as illustrated in Fig. 15. Each of the output buffers drive 1.5 mW of RF power at 94 GHz into the t-line distribution network and approximately 180 μW of power reaches the single-ended input of each divide-by-two block, based on a simulated loss of 3 dB in the LO distribution network.

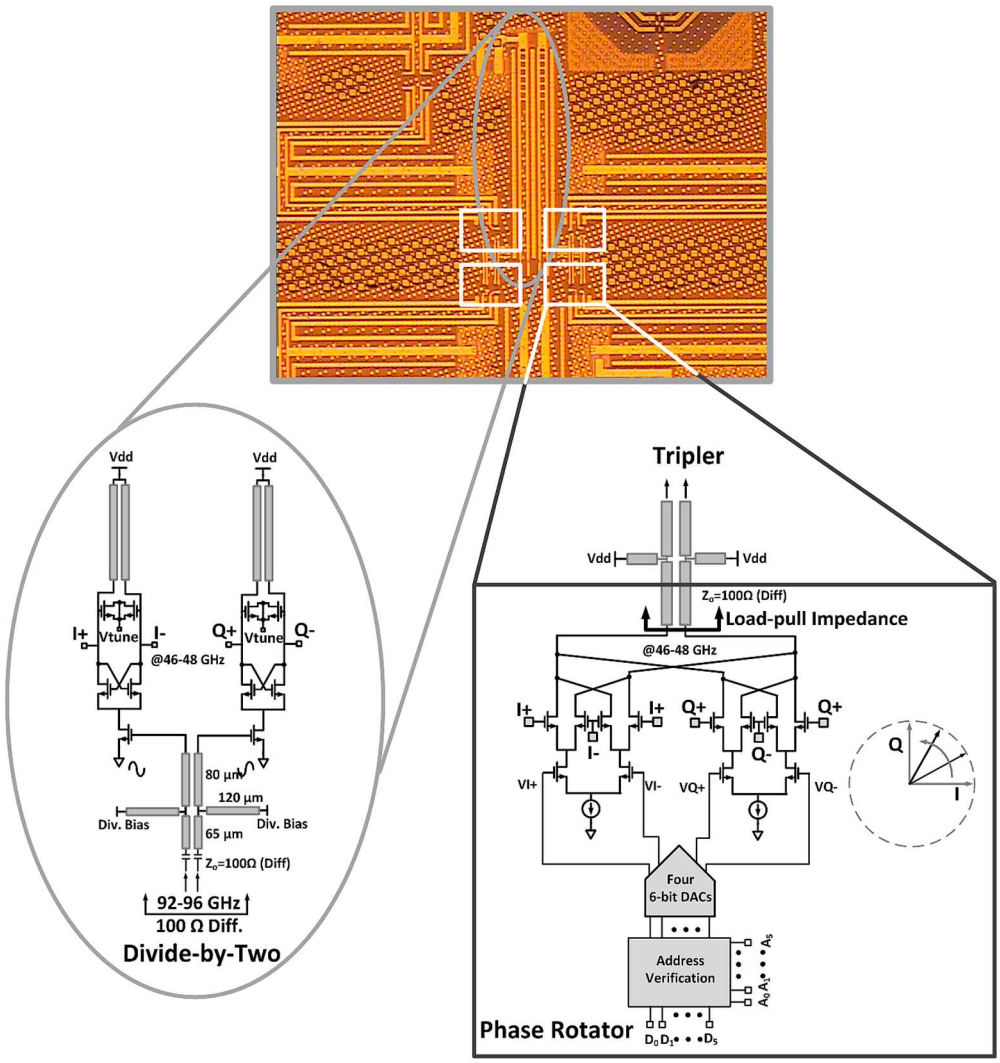

Fig. 16. The injection-locked divide-by-two block showing quadrature signal generation at 47 GHz. Each divider pair drives four phase-rotator blocks whose weights for the quadrature signals are controlled by 6-bit DACs. The placements of these blocks set are shown in the chip.

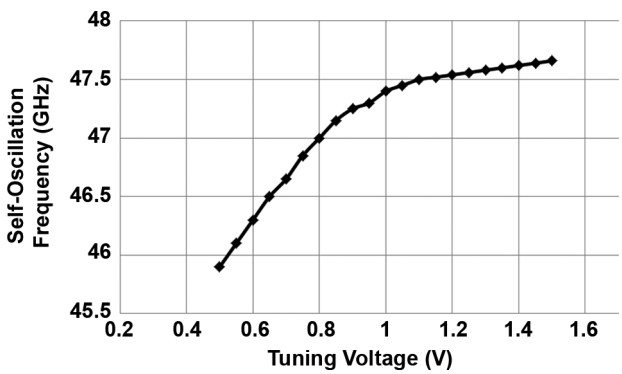

Fig. 17. Simulated variation of central frequency of oscillation of the injection locking divide-by-two block with varactor tuning.

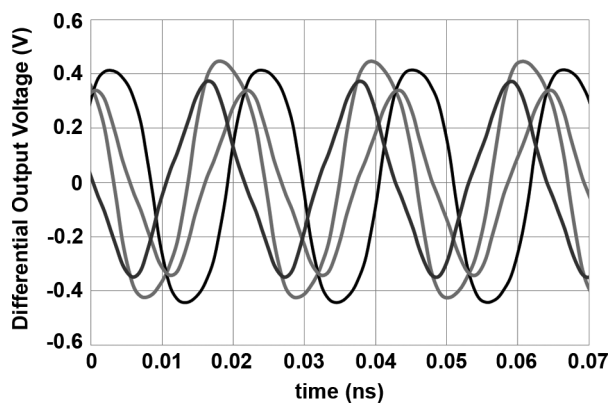

Fig. 18. Simulated outputs of 4 phase-rotators at 47 GHz separated by 45° in phase difference. The differences in their amplitudes do not translate to the succeeding blocks which are injection-locked.

B. 47 GHz Injection Locked Divide-by-Two

The differential signal at 94 GHz from the output buffers, drives the inputs of four sets of single-ended frequency divider pairs which are matched to $Z_{0,\text{diff}} = 100\,\Omega$, as shown in Fig. 16. The divide-by-two blocks achieve the quadrature signal generation, I and Q at half the LO frequency, which are then added

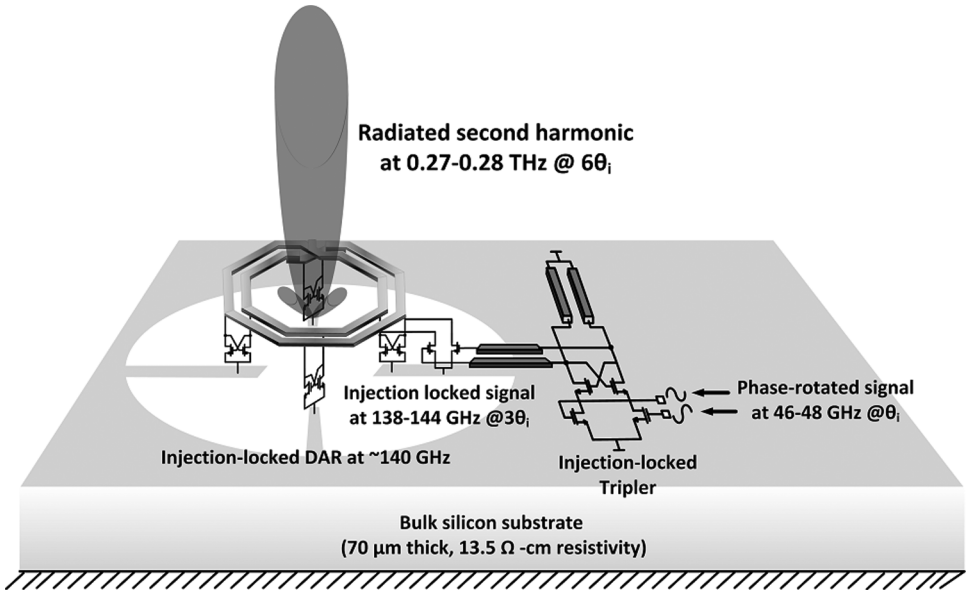

Fig. 19. Injection-locked frequency tripler associated with each DAR showing frequency and phase multiplication from the 47 GHz signal input to the radiated signal at 282 GHz.

with controllable weights to achieve unique phase-rotated signals to be locked to a final radiating DARs. Each divide-by-two pair drives four phase-rotator blocks in its vicinity, as shown in Fig. 16.

The self-oscillation frequency of the divider is designed around to be around 47 GHz, which is half of the center frequency of the central VCO. The differential inductors of 58 pH are realized with coplanar transmission lines isolated by ground tubs. Fig. 16 illustrates the placement of the individual blocks in the chip. Since each divider drives the phase-rotators directly without buffers, parasitic capacitance has to be carefully extracted to ensure accurate resonance frequency. The varactor allows around 1.8 GHz tuning range to the center frequency of the locking bandwidth as shown in Fig. 17. Each divider draws 5.5 mA of current from a 1 V supply.

C. 47 GHz Phase Rotator

Phase-rotation is achieved using a weighted summation of the quadrature signals at 47 GHz with two current-commuting Gilbert cells, as shown in Fig. 16 [32]. The four phase control voltages $(\mathrm{VI}+, \mathrm{VI}-, \mathrm{VQ}+, \mathrm{VQ}-)$ are generated using 6-bit DACs with a serial interface and a 6-bit address. The outputs of the Gilbert cells are current combined through a t-line matching network to generate the phase-rotated signals at 47 GHz that drive injection-locked triplers to generate phase-rotated signals at 141 GHz.

In such a scheme, the magnitude of the output current, and therefore RF power at 47 GHz, is a function of the phase-angle generated, as shown in Fig. 18. When both the quadrature signals are added in equal weights to generate a 45° signal, the output current is $\sqrt{2}$ times that of the case when only one of the quadrature signal is passed. This difference in amplitude, however, does not propagate to the succeeding blocks, since the output swing of the injection-locked tripler is primarily determined by the biasing condition and design of the tripler. However, to ensure that the tripler locking is achieved under the condition of minimum current swing in presence of process variations, the output of the phase-rotator is matched to the load-pull impedance for maximum power transfer as shown in Fig. 16. With a 6-bit control, a phase resolution of approximately 1.5° is achieved at 47 GHz which translates to a phase resolution of 9° at the radiated frequency of 0.28 THz. Each phase rotator draws 22 mA from a 1 V supply.

D. 141-GHz Injection-Locked Frequency Tripler

The schematic of the tripler, whose output locks to the self-oscillation frequency of the DAR, is shown in Fig. 19. The output signal from a phase-shifter at 47 GHz drive a differential current injection in a cross-coupled tripler tuned at 141 GHz [31]. As shown in the Fig. 19, the 47 signal with a phase-angle of θ locks to an output signal of 141 GHz with phase angle of 3θ, which ultimately translates to a radiated signal at 282 GHz with a phase angle of 6θ. The simulated suppression of the fundamental at the output is 21 dB and the simulated gain (@140 GHz/@47 GHz) is -7 dB. The frequency tripler draws 4 mA of current from a 1 V supply.

VII. Measurement Results

The 280 GHz beam-scanning array is implemented in a 45 nm SOI CMOS process with measured typical $f_{\mathrm{t}}/f_{\max} \sim$ 190–200 GHz [19], [21], [22]. The silicon-on-insulator technology does not offer the option of a high-resistivity substrate for low-loss passives and radiating structures. The insulator comprises of a 0.225-μm-thick buried oxide and the bulk resistivity of the silicon substrate below is typically 13.5 Ω-cm which is comparable to other bulk processes. The chip occupies 2.7 mm $\times$ 2.7 mm as shown in Fig. 26.

Previous works on DARs [24], [25] needed no substrate thinning and demonstrated radiation of the signal from the backside

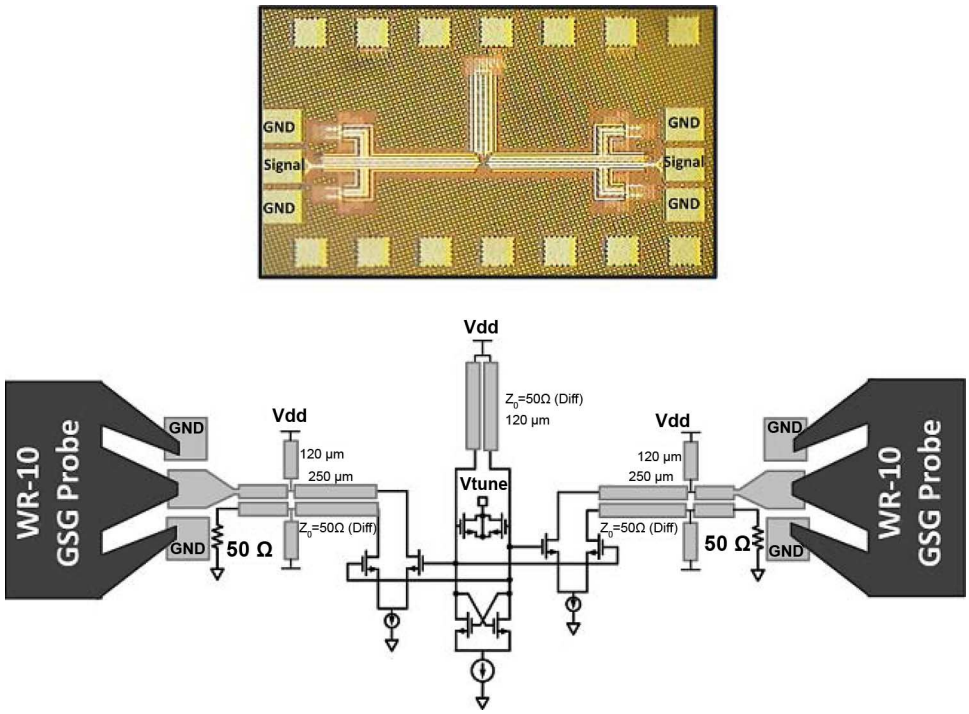

Fig. 20. Measurement set-up for the test structure comprising the central VCO and differential buffers.

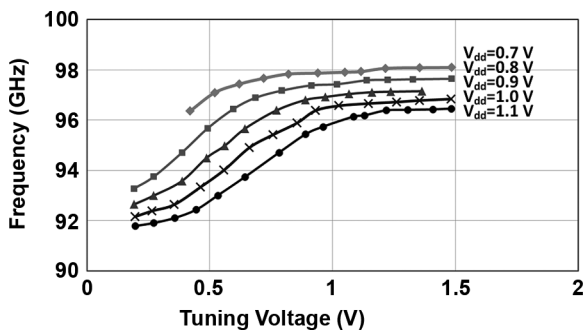

Fig. 21. Measured VCO frequency tuning against varactor and supply voltage.

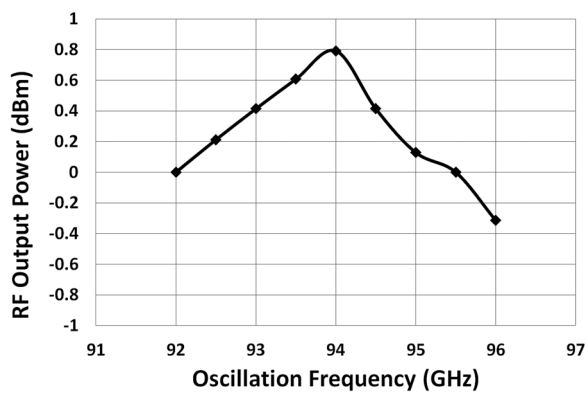

Fig. 22. Estimated differential output RF power from the buffers in the array based on measurements of the VCO test structure.

of the silicon die. However, the integrated beam-scanning array chip with local phase control, centralized frequency locking and LO distribution, presented in this paper, dissipates nearly 820 mW of DC power. The chip, therefore, needs a reliable thermal pathway, since heat dissipation through wirebonds and air is not enough to maintain a stable temperature. The chip is mounted on a brass board to provide that thermal pathway and the chip radiates from the top side, as shown in Fig. 19 and Fig. 26. The substrate is thinned to 70 μm such that the waves reflected from the backside brass mount interfered almost coherently with the topside radiation at 0.28 THz. Simulations showed that the radiation efficiency is not sensitive to the ± 10 μm tolerances of the thinning procedure. The thinning of the chip because of thermal issues does not invalidate the primary point about the effective radiation from electrically thicker substrate and suppression of the substrate modes. The array performance is quantified with free-space measurements and several breakouts of the array are measured as test-structures separately on wafer.

A. Central VCO and the Buffers

In order to characterize the central frequency reference, a stand-alone VCO test-structure with differential output buffers is measured with WR-10 waveguide probes, as shown in Fig. 20. In the 4×4 array chip, the VCO buffers drive load-pull impedances which are matched from 50 Ω differential impedances (Fig. 15). However, in the absence of differential probes in the WR-10 band, one of the output differential lines on each side of the test chip is terminated onchip with single-ended 50 Ω load. The other single-ended t-line is brought out to a 100 μm $\times$ 100 μm Al pad, as shown in Fig. 20. The VCO has a central frequency of oscillation of 94 GHz and can be tuned from 91.8–96.5 GHz under a supply of 1.1 V. The variation of the oscillation frequency with varactor voltage and V_{dd} is shown in Fig. 21. The phase noise of the free-running oscillator is

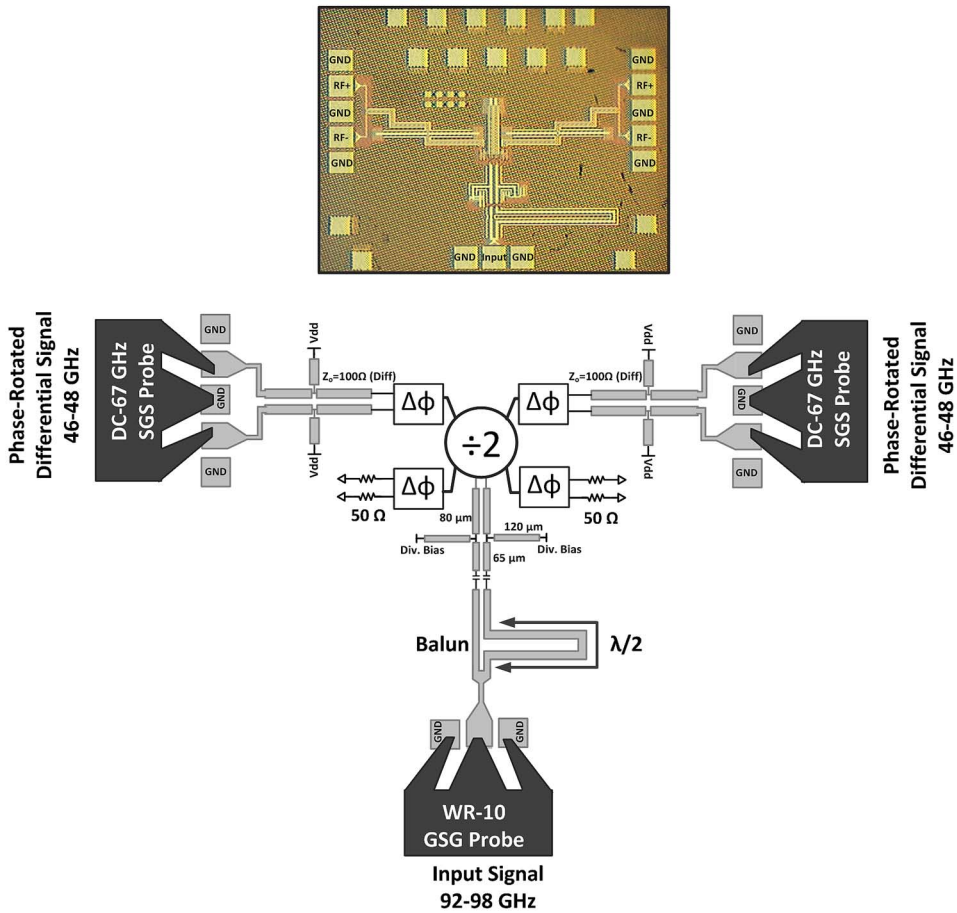

Fig. 23. Measurement set-up for the test chip comprising of one divide-by-two pair which generates quadrature signals at 47 GHz and drives four phase-rotators.

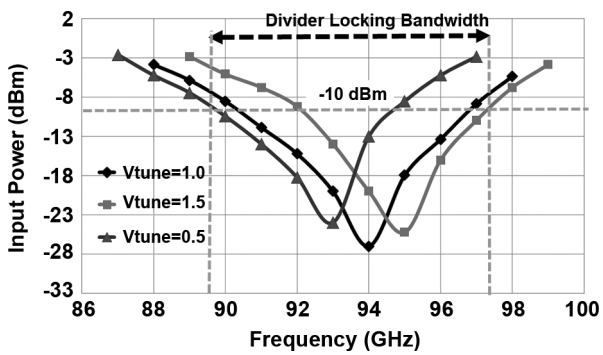

Fig. 24. Measured sensitivity of the injection-locked divide-by-two block for different tuning voltages. The divider locking bandwidth is marked for the LO buffer output power in the array chip.

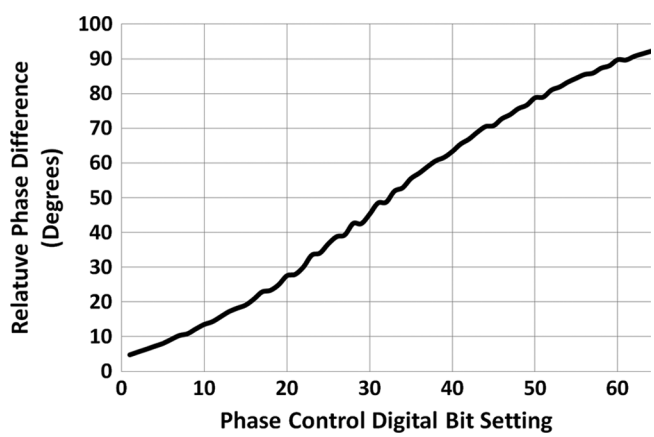

Fig. 25. Measured phase-difference between the output of the two phase-shifters in Fig. 23, as the 6-bit DAC setting for the phase control voltages of one phase-rotator is varied.

measured to be -112 dBc/Hz at 10 MHz offset. The core oscillator and the buffers together draw 30 mA of current from $V_{dd} = 1.1$ V.

A measurement of interest is the output power delivered by the oscillator buffers in the array, since it is critical in determining the locking range of the succeeding frequency dividers. However, because of the difference in output impedance seen by the buffers in the test chip and the array chip, the RF power delivered by the buffers in the 4×4 array is estimated from a measurement of output power from the test chip and 3D electromagnetic simulations of t-line networks in the two chips. Based on the measured single-ended output power at the pads in the VCO test chip, the estimated differential RF power at the buffer output in the array chip is shown in Fig. 22. The output power delivered by each buffer at 94 GHz is estimated to be 1.2 mW implying 150 μW of power would reach each divide-by-two blocks with a simulated loss of 3 dB in the LO distribution network.

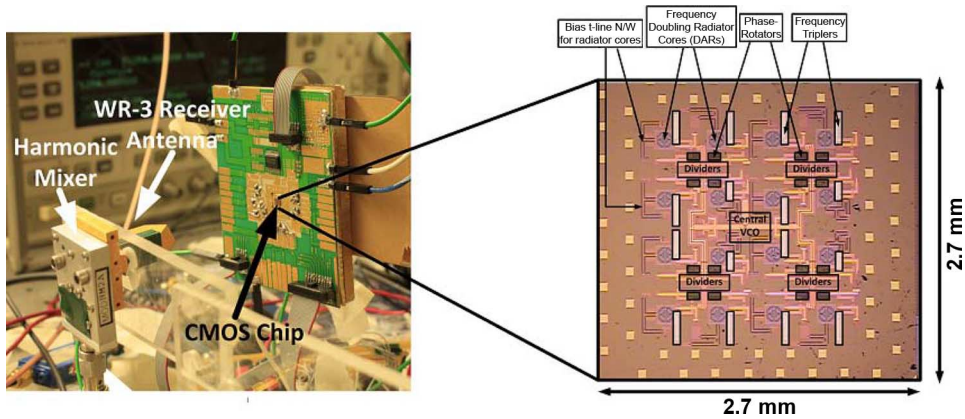

Fig. 26. Die micrograph showing placement of individual functional blocks along with a photo of the measurement setup showing the receiver antenna and the harmonic mixer, as in Fig. 28.

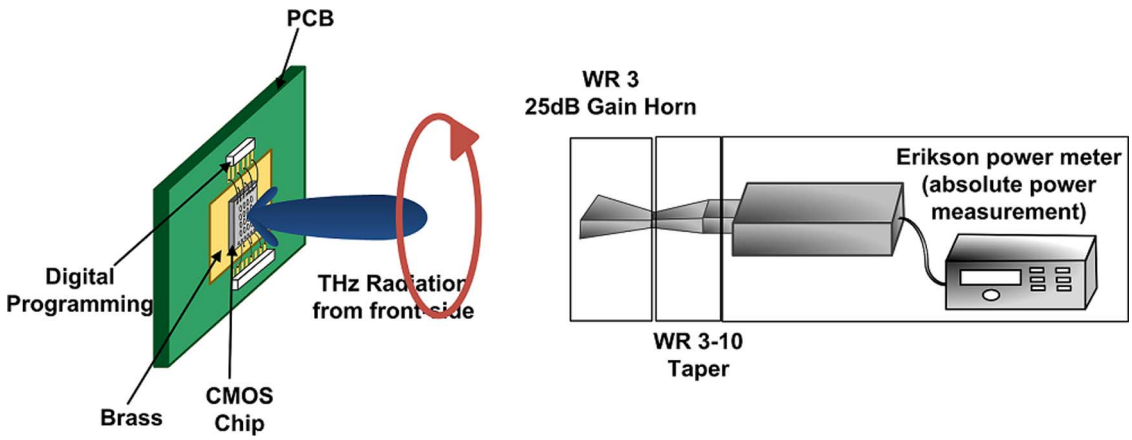

Fig. 27. Experimental set-up for the absolute power and EIRP measurement at the far-field of the radiating 4×4 array chip.

B. Quadrature Signal Generation and Phase-Rotation

A test-structure, comprising of the frequency divider generating the quadrature signals at 47 GHz which drives four phase-rotators, is measured. Due to the absence of a differential probe in the WR-10 band, a single-ended W band input signal is converted into differential mode using an onchip balun, as shown in Fig. 23. The input matching network of the divider and the output network of the phase-rotators are identical to the array chip. The measured sensitivity of the divider, which is the input power necessary to achieve locking and frequency division, is shown in Fig. 24, after calibrating for the loss of the on-chip balun. The divider locking range for the measured VCO output power extends from 89.5–97.3 GHz. The range covers the entire 92–96 GHz tuning range of the VCO for a single tuning voltage of $\mathrm{V_{tune}} = 1.0$ V for the divider.

The phase-rotator performance is measured by probing the outputs of two of the phase rotators with differential SGS probes, while the other two are terminated onchip, as shown in Fig. 23. The phase mismatch of the probes and the measurement equipment on the two sides are calibrated out. To ensure minimum sensitivity to offset voltages and transistor mismatches, the quadrature signals are added with equal weights in one of the phase rotators such that $\mathrm{V_{pr1}} = |\mathrm{VQ_{max}} + \mathrm{VI_{max}}|$, while the control for the other is varied from $\mathrm{V_{pr2}} = |\mathrm{VQ_{max}} + \mathrm{VI_{max}}|$ to $\mathrm{V_{pr2}} = |\mathrm{VQ_{max}} - \mathrm{VI_{max}}|$ using the 6 bit DAC setting. The measured phase-difference between the outputs is shown in Fig. 25. The measurement shows a full range of 90° of phase rotation with an initial offset of 5°.

C. Array Measurement

The die photo and the PCB are shown in Fig. 26. The chip micrograph shows the placement of the central VCO along with LO distribution, frequency dividers, phase-rotators, injection locking triplers and the frequency doubling DAR cores. The free-space measurement set up for the 4×4 array chip is shown in Fig. 27. The radiated power is captured at a distance of 50 mm, by a WR-3 (220–325 GHz) 25 dB standard gain horn antenna. The absolute power is measured using an Erickson power meter, which is a calorimeter based power measurement instrument between 75–2000 GHz [33].[9] The power captured by the receiver antenna with a given aperture is proportional to both the total radiated power from the chip and directivity of the

[9]The effect of IR radiation was not observed during measurement. We also confirmed the observation during calibration of the heterodyne downconversion receiver setup in Fig. 28. The receiver was calibrated at each frequency using a custom sub-mmWave source and the EIRP of the radiated power was measured from the output spectrum using the calibrated set-up. The results follow very closely.

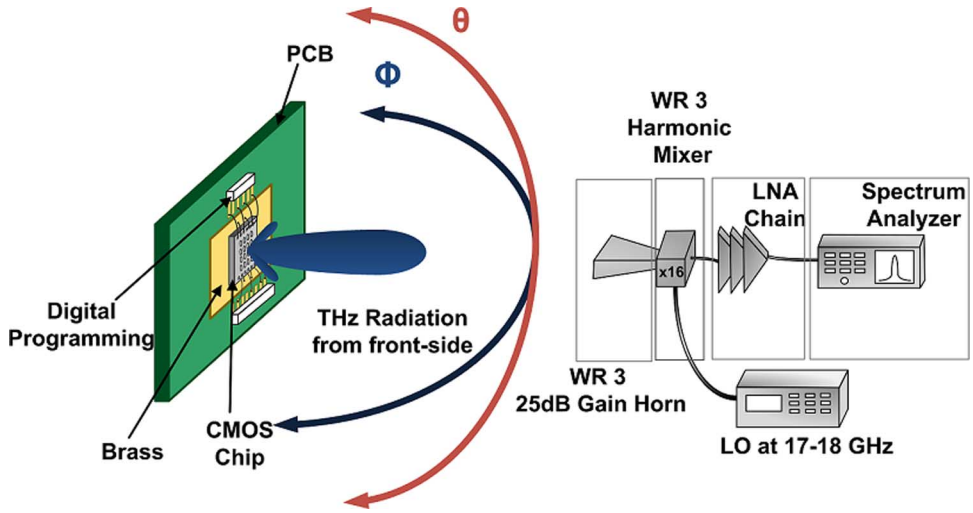

Fig. 28. Experimental set-up for measurement of the frequency of radiated signal and the 3D radiation pattern.

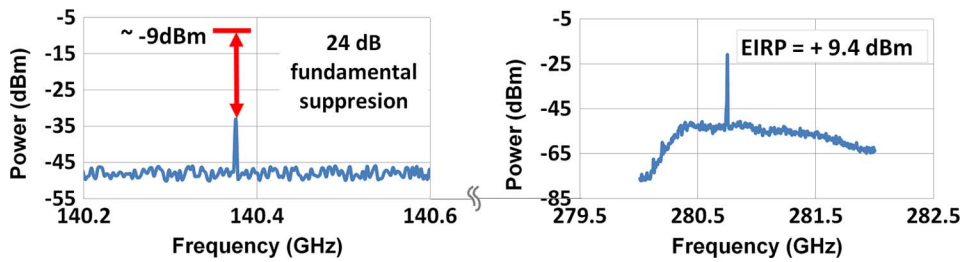

Fig. 29. Calibrated spectrum of the radiated signal at the broadside captured at a far-field distance of 50 mm. The spectrum shows almost 24 dB of fundamental signal suppression near 140.4 GHz and a +9.4 dBm EIRP at the second harmonic frequency of 280.8 GHz.

beam. This measure at any given direction, defined as the Effective Isotropic Radiated Power, is enumerated directly from the power captured by the receiver antenna connected to the Erickson power meter as shown in Fig. 27. For a receiver antenna with gain G_r, and received power P_r at a distance R, the transmitted EIRP is given by

$$\text{EIRP}\,(\theta,\varphi) = \left(\frac{4\pi R}{\lambda}\right)^2 \frac{P_r}{G_r} \tag{4}$$

where λ is the free-space wavelength at the measured frequency and (θ,φ) denotes the measurement direction in elevation and azimuth. Because of the traveling-wave nature of the surface currents in the DAR, the radiated fields are expected to be circularly polarized. This is experimentally verified by rotating the linearly polarized receiver antenna around its broadside axis. The power captured varies by less than 0.5 dB over the entire rotational angle, verifying the nearly circularly polarized nature of the radiation. When all the DARs are radiating in phase, the beam has the highest directivity near broadside. Calibrating for half the power lost due to polarization mismatch, the power captured at the far-field distance of 50 mm near the broadside direction is 8 μW at 281 GHz, which translates to an EIRP of +9.4 dBm. Near-field effects or standing wave formation can cause errors in power measurement. The receiver antenna is placed over a range of far-field distances and the received power followed $1/\mathrm{R}^2$ closely, and the measured EIRP remained constant.

The frequency of the radiated signal is measured by down converting the received signal with a harmonic mixer and

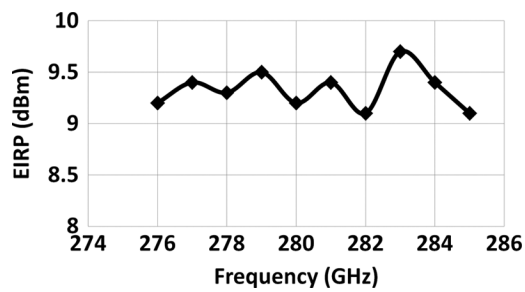

Fig. 30. Variation of measured EIRP at the broadside, as the frequency of the radiated signal is controlled using the central VCO varactor tuning setting.

then amplified by low noise amplifiers and observed in a spectrum analyzer. The entire receiver chain is calibrated between 110–170 GHz and 220–325 GHz using separate WR-6 and WR-3 sources and the Erickson power meter. The calibrated spectrum of the radiated signal near the broadside direction is shown in Fig. 29, for the central oscillator setting of $\mathrm{V_{tune}} = 1$ V. The figure illustrates a strong second harmonic signal at 280.8 GHz with EIRP of +9.4 dBm due to the efficient radiative behavior of DAR. It also shows the quasi-optical filtering effect at the frequency of oscillation, resulting in an estimated 24 dB fundamental power suppression at 140.4 GHz.[10] The frequency of the transmitted signal can be adjusted between 276–285 GHz, as the central VCO is tuned

[10]The fundamental suppression is estimated from a simulated value of RF power at the fundamental frequency injected into the resonator and the antenna aperture area corresponding to the physical chip dimensions.

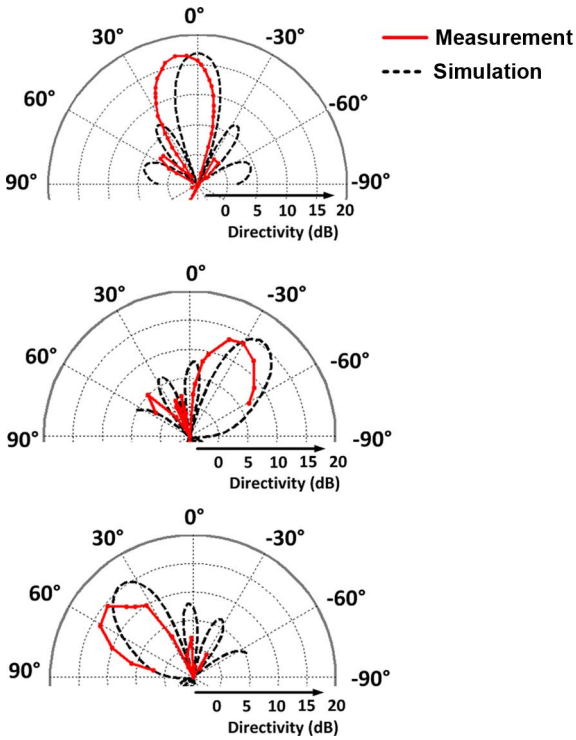

Fig. 31. Radiation pattern measured in the θ plane at 281 GHz showing a directivity of 16 dBi and total electronic beam-steering range of around 80° in the θ plane.

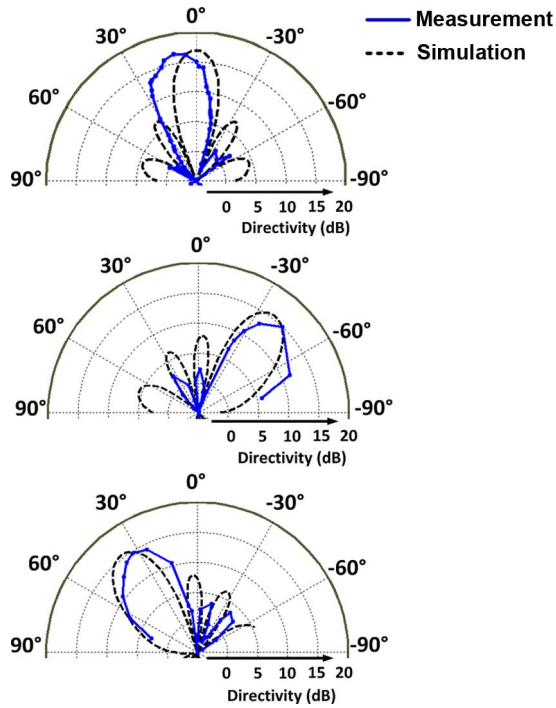

Fig. 32. Radiation pattern measured in the Φ plane at 281 GHz showing a directivity of 16 dBi and total electronic beam-steering range of around 80° in the Φ plane.

from 92–95 GHz. Since the frequency doubling happens only locally at the radiator cores themselves, the EIRP remains fairly constant and varies by less than 0.5 dB over the entire tuning range, as shown in Fig. 30.

To demonstrate electronic beam-steering, a progressive phase-shift between the adjacent radiators is created in each of the two orthogonal axes. This is achieved using the digital phase-rotation settings at the lower frequency of 47 GHz, which is up-converted in phase at the radiated frequency of 281 GHz. The radiation patterns are measured by rotating the Tx chip in three dimensional space as shown in Fig. 28. The measured radiation patterns at 281 GHz in azimuth and elevation are shown in Figs. 31 and 32. The clean array pattern with one major lobe indicates the effectiveness of surface wave cancellation in the silicon chip. While the gain of the array could not be measured because of the self-sustained oscillatory nature of the DAR, the directivity (shown in dB in Figs. 31 and 32) is enumerated by integrating the measured 3D profile of the radiation pattern. The rotational symmetry of the DAR results in a similar symmetry along the direction of maximum directivity in both the orthogonal planes. The maximum directivity is measured to be approximately 16 dB and the total radiated power is 190 μW for an EIRP of 9.4 dBm at 281 GHz. Figs. 31 and 32 show an approximately 80° of beam-scanning control in each of the 2D axes. To effect a beam tilt of $\Delta\alpha = 40^\circ$ from the broadside direction at 281 GHz, the phase shift, $\Delta\beta$, between adjacent radiators, separated by approximately 500 μm on-chip, is given by

$$\Delta\beta = 180^\circ \sin(\Delta\alpha) \times \frac{2.8.}{3.0} \approx 108^\circ \qquad (5)$$

Chip performance summary

Transmitter Performance	
Frequency of operation	276-285 GHz
Maximum broadside EIRP	+9.4dBm
Total radiated power (broadside)	190μW
EIRP variation with frequency	less than 1dB
Beam-steering	80° in in 2D space
Beam-steering resolution	limited by DAC res.
Side lobes ratio	>10dB
Central time-base VCO tuning range	90.2-98.5 GHz

Power consumption	
Central VCO and Buffers@1.1V	30mA
Divide-by-two elements (total of 8) @1.1V	8mA per element
Phase-rotators (total of 16)@1.1V	22mA per element
Triplers (total of 16) @1.1V	4mA per element
Distributed active radiators (total of 16) @0.8V	20mA per element

Fig. 33. Chip performance summary.

This implies a phase-difference of 18° at the sub-harmonic locking frequency of 47 GHz, which is easily achieved using the 6 bit control for the phase-shifters. The chip performance is summarized in Fig. 33.

VIII. Conclusions

A scalable transmitter architecture for power generation and beam-steering above $f_{\max}$ using a centralized frequency reference, sub-harmonic signal distribution, and local phase control is presented in this paper. We introduce the concept of *distributed active radiation* which combines circuits, electromag-

netics and radiation in a holistic fashion to achieve high efficiency conversion from DC power to radiated terahertz power above $f_{\max}$ of a technology. The design evolution of DAR follows from an inverse design approach where surface currents at different harmonics are formulated in the silicon chip for the desired electromagnetic field profiles. Circuits and passives are then designed conjointly to synthesize and control the formulated surface currents. The DAR consists of a single active-coupled electromagnetic structure achieving signal generation, frequency multiplication, radiation and filtration of undesired harmonics simultaneously in a small silicon footprint. In this paper, based on the DAR, we present a two-dimensional 4×4 radiating array in 45 nm SOI CMOS, which radiates with an EIRP of $+9.4$ dBm at 0.28 THz and beam-steers in 2D over 80° in azimuth and elevation. To the best of the authors' knowledge, this is the first reported integrated beam-scanning array at THz frequencies in silicon.

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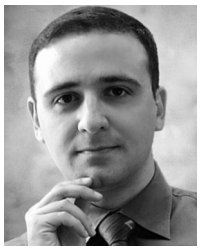

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