10.1 A 77GHz 4-Element Phased Array Receiver with On-Chip Dipole Antennas in Silicon

A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri

California Institute of Technology, Pasadena, CA

Achieving higher levels of integration has been the driving force behind the semiconductor industry. Silicon chips are assuming greater functionality at higher frequencies in a smaller area and at a lower cost. Millimeter (mm) wave applications such as short-range communications at 24GHz and 60GHz and automotive radar at 24GHz and 77GHz are the vanguard of the new generation of high-frequency wideband integrated circuit applications. However, a major challenge in such systems is the design of high-frequency interface to the off-chip components. In this paper, a fully integrated 4-channel phased-array receiver with four integrated dipole antennas, the complete RF signal path from 77GHz down to baseband, and an on-chip LO generation and distribution is presented. The antenna integration eliminates the need for the high-frequency interface to the off-chip elements.

Off-chip radiating elements suffer from additional interconnect losses and cannot duplicate the reproducibility of on-chip antennas. This is due to the extremely tight dimension control necessary in the off-chip radiators and their high frequency connections to the chip.

The small wavelength at mm-wave frequencies makes it possible to use on-chip metal layers to fabricate small integrated antennas. The primary challenge for an on-chip antenna is the high dielectric constant of silicon (ε_r=11.7) which absorbs most of the radiated power into the substrate instead of radiating it into space. For instance, a dipole antenna placed at the interface of semi-infinite regions of silicon and air radiates only 5% of the power into the air and the remaining 95% couples into the silicon. Shielding the antenna from the substrate is inefficient since in a typical silicon process, the small distance between the top and bottom metal layers corresponds to a small fraction of the wavelength in SiO_2 (roughly 0.01λ for 20μm at 77GHz). The first-resonance-mode radiation resistance of a dipole, 0.01λ away from the ground layer, is around 1Ω. In addition to the practical problems in driving such a low-impedance load, any parasitic resistance in the antenna metal significantly lowers the efficiency (*e.g.*, a factor of 2 for 1Ω ohmic loss).

The inevitable energy coupling into the substrate can be exploited by radiating from the backside of the chip. However, radiating from a planar backside suffers from energy coupling into substrate surface wave modes and is very inefficient [1]. Fortunately, this problem can be overcome by mounting the chip on a hemispherical piece of dielectric (a lens) with a similar dielectric constant as that of silicon to convert the surface modes into useful radiation power (Fig. 10.1.1).

In this work, dipole antennas are designed using the three bottom metal layers (each around 0.3μm thick). This design combined with the lens on the backside substantially improves the gain and increases the radiation resistance of the dipole antennas to 45Ω at their first resonance mode. To minimize the impact of substrate loss due to its conductivity, all four receive antennas are placed at the edge of the chip and a slab of undoped silicon of the same thickness of substrate is abutted to the substrate (see Fig. 10.1.1), maintaining the same dielectric constant with a lower loss. Each antenna occupies less than 0.02mm^2 of area.

The entire 4-element phased-array receiver operates differentially to minimize electromagnetic interference, substrate coupling, and common-mode oscillations. Each differential antenna drives a differential transmission line (t-line) which subsequently drives the input of one of the four on-chip LNAs. The two-stage differential cascode LNA uses single ended shunt and differential series t-lines for matching (Fig. 10.1.2). To maintain a high CMRR at mm-wave frequencies a common-mode resistance is placed at the base of the cascode transistors, suppressing the common-mode gain by 20dB.

Figure 10.1.3 shows the block diagram of the 77GHz phased-array receiver section of the chip. It integrates the complete signal path including four 77GHz RF front-ends, distributed signal combining at IF, LO generation and distribution, and local phase rotators. Each RF front-end consists of an on-chip dipole antenna, an LNA, a mixer, and a variable gain IF amplifier. The phase shifting is performed at the LO port of each mixer. The 26GHz IF signals are combined using a symmetric distributed signal combining amplifier. The combined signal is further down-converted using quadrature IF-to-baseband mixers. The first LO signal at 52GHz is generated using a VCO, which also generates the second LO via a quadrature divide-by-two block. The VCO can be locked to an external low-frequency reference using a frequency divider chain.

The four IF signals are combined through a distributed signal combining amplifier (Fig. 10.1.4). The differential transconductors with resistive degeneration at the IF increase the dynamic range. Their current outputs are symmetrically routed to the combining node via a two-stage binary structure. Common-base transistors are used at each combining junction to isolate the input and output ports. The total length of the differential routing t-line T_1 is 340μm and that of T_2 is 2.55mm.

The 77GHz phased-array system is designed and fabricated in a 120nm SiGe BiCMOS process with the BJT f_T of 200GHz. The phased-array receiver is implemented on the same die as the transmitter [2] and occupies roughly 9mm^2 of the 6.8mm×3.8mm chip.

The electrical performance of the receiver can be characterized by laser trimming the antennas and feeding the LNA inputs via waveguide probes. A 37dB single-path receiver gain is measured at 79.8GHz with a 2GHz bandwidth, corresponding to an inferred array gain of 49dB. Figure 10.1.5 shows the measured gain and NF of the complete receiver and the standalone LNA, which have minimum NF of 8.0dB at 79.2GHz and 5.7dB at 75.7GHz, respectively. The 4-element array can improve the SNR by up to 6dB for uncorrelated antenna noise. LNA peak gain of 23.8dB is measured at 77GHz with a 3dB bandwidth of more than 6GHz. Each LNA consumes 17.5mA and each down-conversion path (excluding LNA) dissipates 40mA.

The radiation performance of the complete receiver is measured using the setup shown in Fig. 10.1.1 where a PCB provides the supply as well as low frequency and digital control signals to the chip and takes the baseband signal out using wirebond connections. A W-band standard horn antenna irradiates the receiver. The peak measured antenna gain is +2dBi. This gain can be further improved by 4 to 5dB using a smaller lens with the quarter-wavelength matching layer. Figure 10.1.6 shows the measured E-plane single-chain receiver radiation pattern with and without the lens. The chip micrograph is shown in Fig. 10.1.7.

Acknowledgements:
The authors acknowledge T. Yu, D. Rutledge, S. Weinreb, and G. Rebeiz for their assistance and thank Ansoft, Zeland, and Integrated Engineering Software for software support.

References:
[1] D. B. Rutledge, *et al.*, "Integrated-Circuit Antennas," *Infrared and Millimeter-Waves*, New York: Academic, pp. 1–90, 1983.
[2] A. Natarajan, *et al.*, "A 77GHz Phased-Array Transmitter with Local LO-Path Phase-Shifting in Silicon," *ISSCC Dig. Tech. Papers*, Paper 10.2, Feb., 2006.

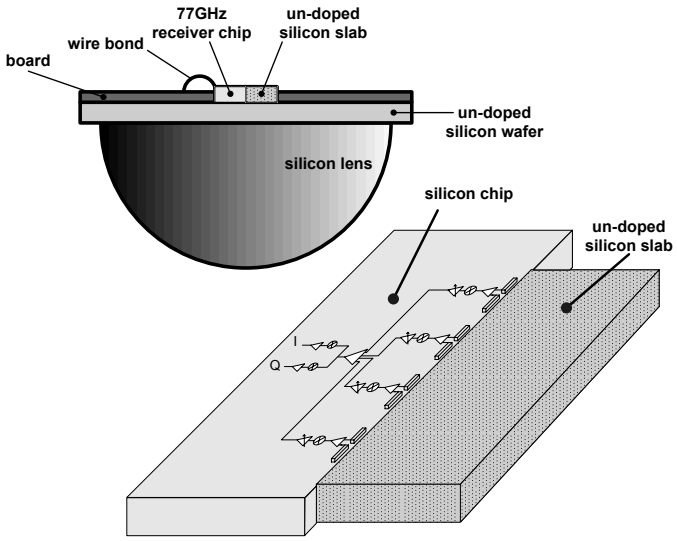

Figure 10.1.1: Chip, board, and lens antenna setup configuration.

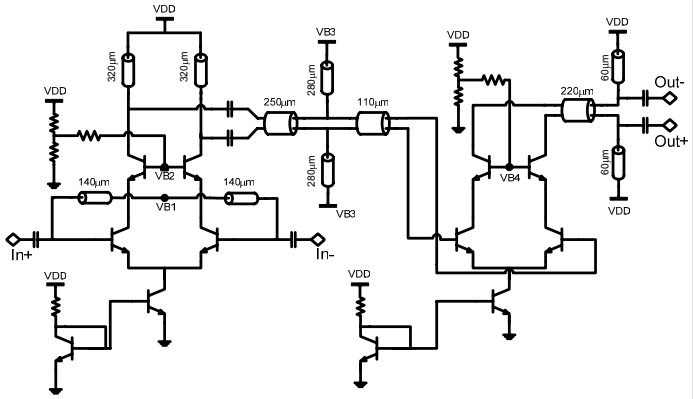

Figure 10.1.2: 77GHz LNA schematic.

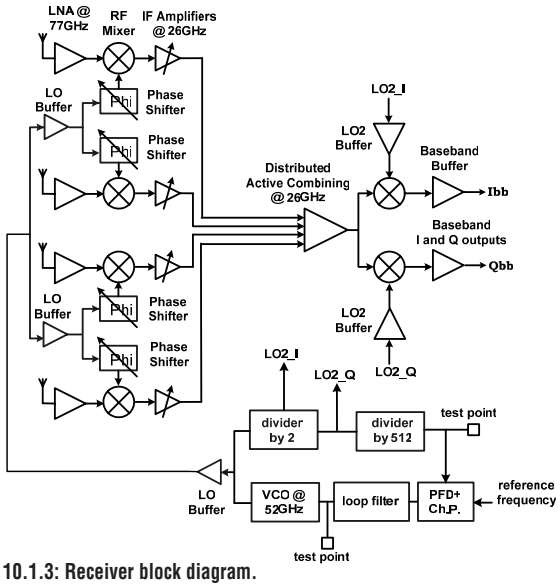

Figure 10.1.3: Receiver block diagram.

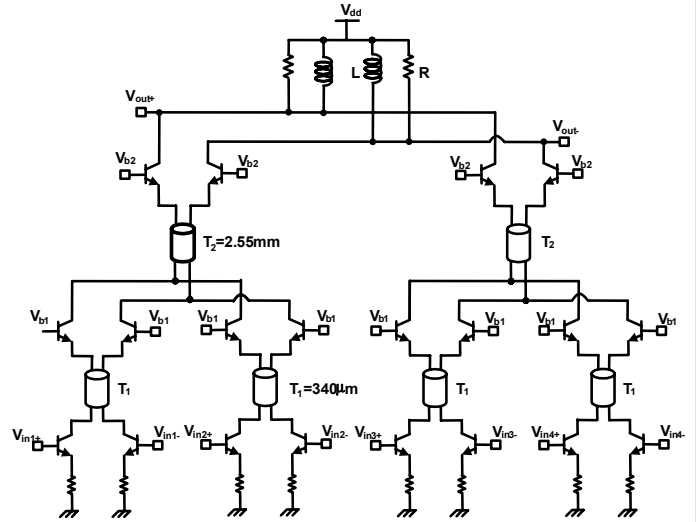

Figure 10.1.4: Schematic of the distributed active phase combining.

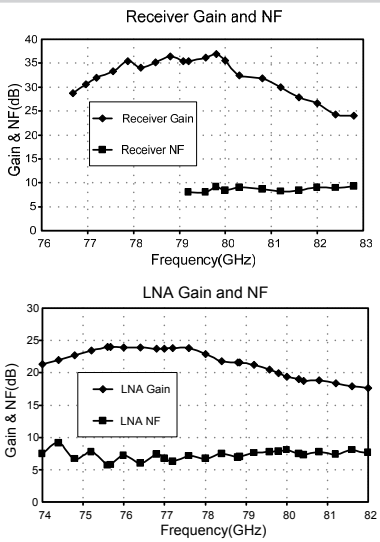

Figure 10.1.5: Gain and NF measurement results of LNA and receiver.

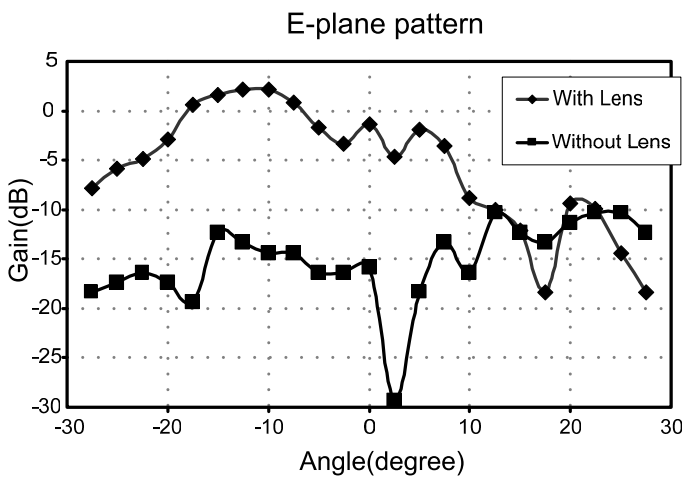

Figure 10.1.6: E-plane pattern of a single on-chip dipole.

Continued on Page

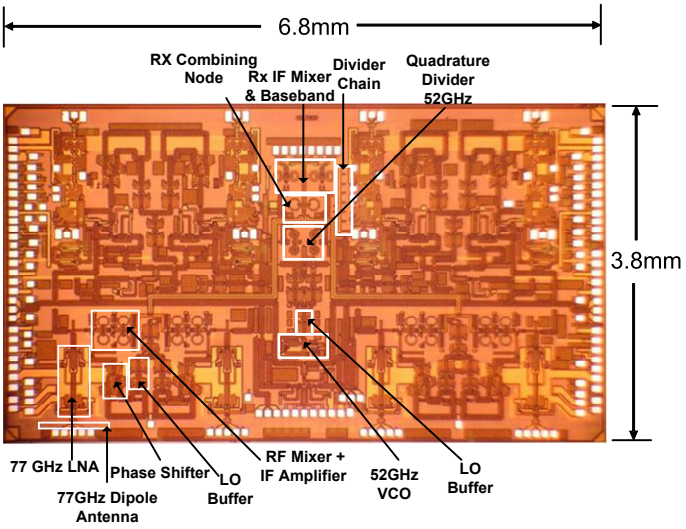

Figure 10.1.7: Chip micrograph.