Fully Integrated Frequency and Phase Generation for a 6-18GHz Tunable Multi-Band Phased-Array Receiver in CMOS

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***Abstract* — Fully integrated frequency-phase generators for a 6-18GHz wide-band phased-array receiver element are presented that generate 5-7GHz and 9-12GHz first LO signals with less than -95dBc/Hz phase noise at 100kHz offset. Second LO signals with digitally controllable four-quadrant phase- and amplitude spread with better than 3° resolution are generated and allow removal of systematic reference clock skew as well as accurate selection of the received signal phase. This frequency- and phase generation scheme was successfully demonstrated in a 6-18GHz receiver system configured as an electrical 4-element array.**

***Index Terms* — Array signal processing, CMOS, frequency synthesizers, phase control, phase locked loops, phase noise, phased arrays, radio receivers**

I. Introduction

Very large-scale phased-arrays covering a wide range of frequencies can provide exciting new opportunities for increased data rates, greater selectivity and greater system robustness for a host of applications such as radar and communications due to the array gain, noise reduction, and beam-forming capabilities offered. Traditionally, such systems were implemented in a module-based approach using compound semiconductor technologies. However, recent efforts have focused on integrating entire receivers/transmitters for phased-array applications in silicon based technologies to take full advantage of reduction in size, higher integration, and economies of scale that modern Si-based technologies offer [1].

Figure 1 shows a possible architecture for a phased-array system using monolithic receiver elements. We have developed a tunable, multi-band 6-18GHz CMOS receiver that integrates the necessary electronics for phased-array operation on-chip [2]. In this paper, we discuss the frequency- and phase generation for this system. In our approach, the second LO signal's phase and amplitude for the IF-to-baseband down-conversion mixer of each receiver is digitally controlled. In this LO-phase shifting scheme, the beam is formed by combining the output base-band signals in current domain.

Besides enabling the beam forming in base-band, independent and precise phase and amplitude control of all second LO signals also enables the removal of inevitable, absolute delay variations and mismatches in the frequency reference paths to the receivers, as well as any systematic

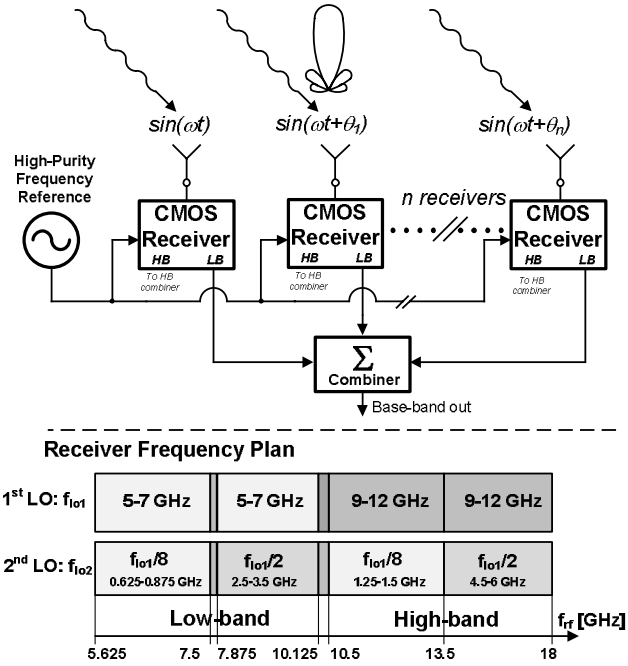

Fig. 1: Phased-array architecture based on individual receiver modules, receiver frequency plan. In the implemented receiver [2], the incoming RF signal is split into a low-band (6-10.5GHz) and a high-band portion (10.5-18GHz) inside the receiver, and two polarizations are supported simultaneously.

RF signal phase mismatches between individual receiver elements.

In a phased-array configuration, phase noise from *uncorrelated* sources is added in power at the output, whereas the output signals are added in amplitude in the beam-forming process. Hence, in a phased-array with N elements, the noise from such sources is reduced by $10 \cdot \mathrm{Log}_{10}(N)$ [dB] in the combined signal. In a very large array, then, the phase noise of the received signal is limited by the quality of the reference used rather than noise generated within each receiver element. Using our CMOS receivers, we have verified this reduction in an electrical 4-element array.

This paper is organized as follows: in section II, the frequency- and phase-generation schemes used in the receiver are described, including system- and circuit-level design considerations. Section III presents and discusses the circuit implementation as well as measured performance results.

II. CIRCUIT DESCRIPTION AND DESIGN CONSIDERATIONS

A. Block Level Description

To concurrently receive signals at two arbitrary frequencies in this receiver (one low-band and one high-band signal), two independently controlled fully-programmable LO frequencies are generated. Hence, two complete phase-locked loop frequency- and phase-synthesizers (FPSs) are implemented on the same chip as the rest of the receiver, covering the low- and high-band respectively, and allowing full digital control over the phase and amplitude of the second LO signal.

Figure 2 shows the block diagram of the phase-frequency generation scheme used for both the low-band (LB) and high-band (HB) FPS's of the receiver. A VCO is used for first LO signal generation, and is followed by static divide-by-two frequency dividers, implemented as master-slave D-flip flops in a feedback configuration. A MUX chooses between a divide-by-two and a divide-by-eight version of the VCO frequency for the second LO frequency generation. This scheme allows reducing the VCO tuning range without degrading the receiver frequency coverage. This, in turn, reduces the VCO gain and the free-running VCO phase noise. The static divide-by-two circuits also provide I- and Q-second LO components over an inherently wide bandwidth. The I- and Q-components are separately amplified by digitally controlled, variable-gain amplifiers, and the outputs are summed in current domain providing four-quadrant, full amplitude-spread phase generation [3] for the second LO signal. Figure 3 shows a simplified schematic of the VCO, static divider and the variable-gain amplifiers.

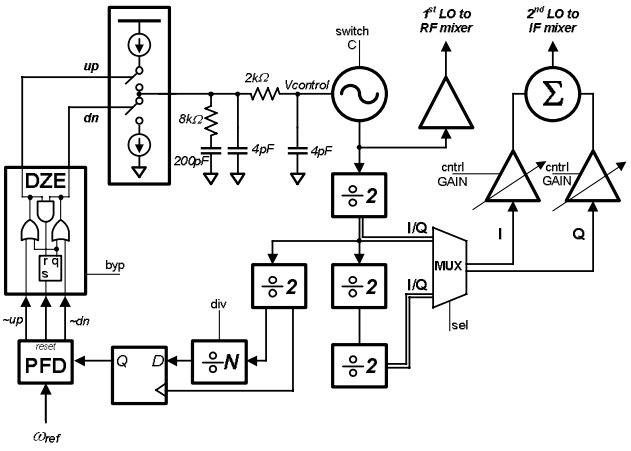

Fig. 2: Block diagram of the frequency- and phase-synthesizers. The two implemented synthesizers differ in the center frequency of the VCO and correspond to the low-band and high-band of the system.

The 2nd LO output signal is thus given by:

$$LO_2[t]=B\sin(\omega t+\phi) \quad (1)$$

where $B=(A_1^2+A_2^2)^{1/2}$ and $\phi=\cos^{-1}(A_1/B)$, A_1 and A_2 are the digitally programmed amplitudes of VGA outputs of the LO_2 I- and Q-components (cmp Fig.2). Hence, full amplitude and phase control is achieved.

A PLL determines the absolute frequencies of the first and second LO signals. A programmable divider using an architecture presented in [4] with some modifications is used to provide programmable division by an integer between 16 and 63 of the divided-by-four VCO signal. Its output is retimed in order to lower its noise contribution to the generated signal. The phase-frequency detector (PFD) is followed by a dead-zone elimination circuit (DZE), which prevents erratic drifting around the center frequency and a corresponding increase in output RMS jitter. Finally, a charge-pump and a third-order loop filter are used to close the loop.

B. Design Considerations

Over the bandwidth of the FPS, the VCO gain and division ratio vary significantly. This affects both noise performance and loop stability. To reduce the variability in the VCO gain and extend the VCO tuning range, MIM

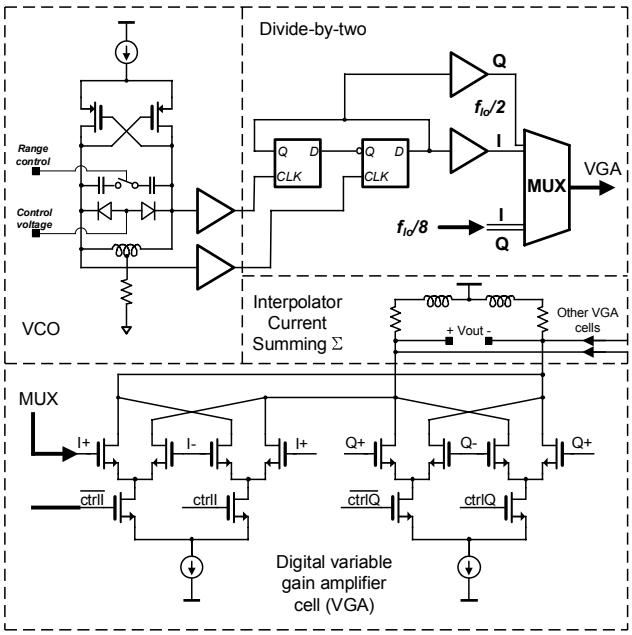

Fig. 3: Simplified schematic showing the VCO, the first divide-by-two circuit and one section of the variable gain amplifier. The output signal is summed in current domain.

capacitors in the VCO tank are digitally switched in or out to vary the center frequency and increase the tuning range. PMOS transistors rather than NMOS are used in the VCO core to reduce phase noise in the $1/f^3$ region. Large PMOS devices are also used on the reference signal input of the PFD in order not to degrade the phase noise of the frequency reference signal. To avoid unduly loading the VCO and degrade its performance and range, the output of the divide-by-*N* circuit is retimed to its own input rather than the VCO itself.

All divider circuits have significant margin on the maximum operating frequency, and customized current consumption to obtain an optimal trade-off between speed and power consumption.

To guarantee stability and low-noise performance of the PLL, the loop response is optimized using frequency domain simulations, taking into account the variations in the VCO gain and the division ratio, noise contributions of the loop filter and charge-pump headroom constraints. The worst case simulated phase margin is 45° over all values of VCO gain and division ratios. A third-order loop filter is chosen to provide some isolation between the VCO and the charge-pump output and additional filtering of undesirable spurious frequency feed-through at the control voltage node.

Two novel variable gain amplifiers (VGAs), whose design is insensitive to device modeling uncertainties and PVT variations, are used in the Cartesian second LO phase synthesis. Using differential design techniques, the VGA maintains a constant output DC bias point and AC response for arbitrary digital control bit settings.

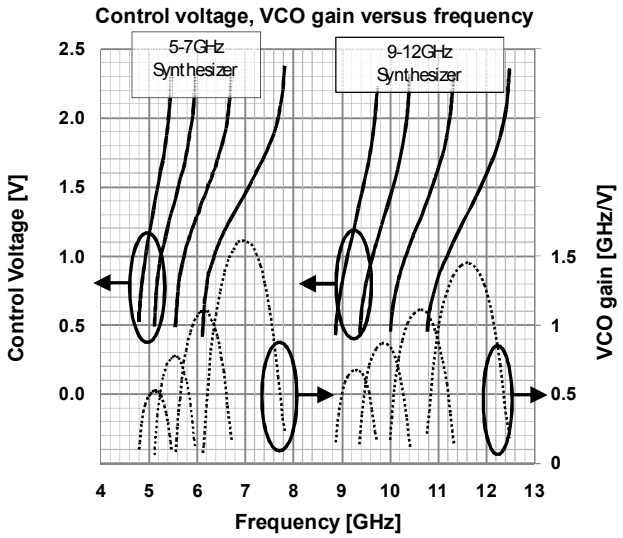

Fig. 4: Left axis: control voltage versus frequency for all four VCO tank capacitor settings. Right axis: corresponding VCO gain.

III. Implementation and Measurements

The circuit is fabricated in a 130nm CMOS process. Figure 4 shows the output frequencies as a function of VCO control voltages for the two synthesizers in the upper half of the plot, while the corresponding VCO gain curves are shown in the bottom half of the figure. The 10-bit Cartesian phase interpolation scheme achieves a maximum integral phase error (IPE) of 0.54º and a maximum differential phase error (DPE) of 0.74º for a 360º interpolation with a phase step of 11.25º (Figure 5). For a four quadrant continuous phase synthesis, the maximum phase error for generating an arbitrary phase signal is less than 2.5º across the range of operating frequencies. This enables digital calibration of inevitable phase skew in the reference signal paths and/or RF signal paths between different receiver elements in an array system.

Figure 6 shows a plot of measured close-in base-band phase noise of four individual modules configured as an electrical array as well as the overall array phase noise performance. As expected from theory, the electrical array has a 6dB improved output phase noise compared to the individual elements. Writing the output signal of the n^{th} module as

$$V_n[t] = V_{n,sig}[t] + v_n[t] \qquad (2)$$

where $v_n[t]$ is the noise term. The output SNR is the ratio of the rms value of the combined output signal, $V_{out,rms}$,

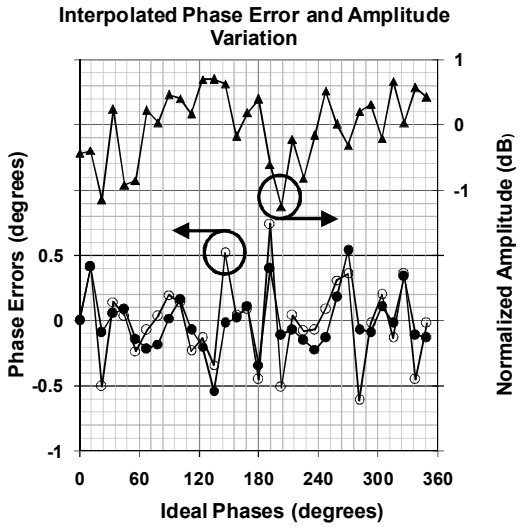

Fig. 5: Phase errors and amplitude variation at f_{LO2}=6GHz. Left axis: interpolated phase errors in degrees (dots for integrated- and circles for differential errors). Right axis: normalized amplitude in dB (filled triangles).

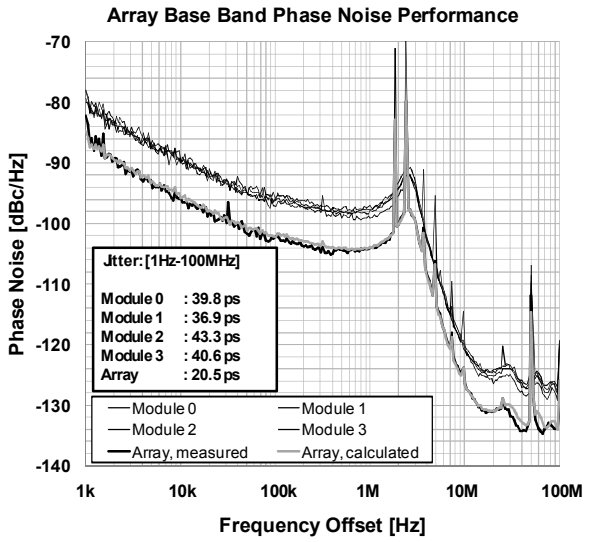

Fig. 6: Measured phase noise at 7.5GHz RF frequency of an *electrical* 4-element array and the individual modules. Spurious tones originate from two of the modules, and are likely related to the custom packaging. Base-band RMS jitter is also shown.

over the square root of the combined output signal noise power $E[v_{out}^2]$, which is, assuming coherent combining, equal base-band amplitudes and uncorrelated noise:

$$V_{out,rms}/(\sqrt{E[v_{out}^2]}) = n \cdot V_{sig}/\sqrt{(n\, v^2)} \qquad (3)$$

with $v^2=E[v_n^2]$ and $V_{sig}^2=E(V_{n,sig}^2)$ for all *n*. The improvement over a single receiver, then, is $\sqrt{n}$, or $10\cdot\log(n)$ [dB]=6dB for n=4 as measured.

The phase noise of a single synthesizer at 100kHz offset from the RF carrier stays below -95dBc/Hz over the entire range of output frequencies of 5-7GHz and 9-12GHz. Digitally bypassing the deadzone elimination for experimental purposes increases output RF RMS jitter from 364fs to 13.7ps for a VCO frequency of 9.4GHz.

TABLE I
PERFORMANCE SUMMARY

Current consumption	PLL core: 34mA (1.2V)
	VCO: 12mA (2.5V)
	Buffers: 19mA (1.2V), 64mA (2.5V)
	Phase Interpolator VGA:4.8mA (2.5V)
Frequency range	5-7GHz and 9-12GHz
Phase noise	-97dBc/Hz @100KHz typical
Max Phase Error. Step size: 11.25º	0.54º @ f_{LO2}=6GHz (integral) 0.74º @ f_{LO2}=6GHz (differential)
Max. Step for continuous interpolation.	3.0º @ f_{LO2}=6GHz

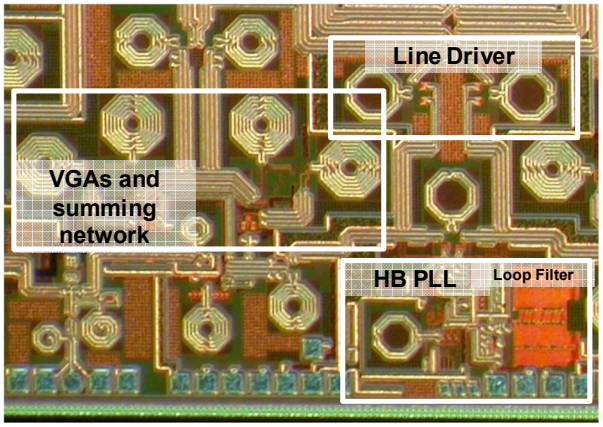

Fig. 7: Die photograph of the high-band synthesizer

Table 1 summarizes the important performance parameters of the frequency-phase synthesizer. Figure 7 shows the die photographs of the high-band synthesizer.

IV. CONCLUSION

To summarize, a 5-7 GHz and a 9-12GHz frequency- and phase-synthesizer for a 6-18GHz wide-band receiver have been presented. Important system-level decisions and block-level design considerations as well as our design approach have been discussed, supported by measurement results of the fabricated integrated circuits.

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