A Wide-Swing Low-Noise Transconductance Amplifier and the Enabling of Large-Signal Handling Direct-Conversion Receivers

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***Abstract*—In this paper, the design of a wide-swing low-noise transconductance amplifier (LNTA) is presented in the context of passive mixer-based direct-conversion RF receivers, noting that the compression performance of such systems is limited by the initial voltage-to-current conversion. The proposed LNTA utilizes a stacked PMOS/NMOS common-gate configuration with its input common-mode voltage maintained by a class-AB operational transconductance amplifier (OTA). Linearization mechanisms and design procedures are explained both quantitatively and intuitively. Simulations of the LNTA at the typical corner, when ideally loaded, show an IIP3 of +32.8 dBm extrapolated at a +12.5 dBm/−16.5 dBm CW blocking condition and an out-of-band 1-dB desensitization point of +22 dBm. These results are also shown to qualitatively agree with those extracted from an analytical model of the LNTA.**

***Index Terms*—Common-gate, low-noise amplier (LNA), low-noise transconductance amplifier (LNTA), RF receiver, wide-swing.**

I. General Design of a Large-Signal Handling Direct-Conversion Receiver

LARGE-SIGNAL handling receivers achieve appreciable sensitivity to a small desired signal in the presence of out-of-band interferers whose voltage amplitude approaches that of the supply rail. As depicted in Fig. 1, such receivers would find use in frequency-domain-duplexed (FDD) communications transceivers, in devices conducting wireless communications in the presence of wireless power transfer, and in military communications robust against hostile jamming interference used for countermeasures. Once it is determined that building such a receiver is a worthwhile goal, the natural question becomes how to generally approach the architectural design of the receiver.

Inevitably, the small-signal gain provided by a semiconductor device is a function of electric potential, not flow. For example, the boundaries of the three regions of operation of an ideal square-law MOS device are thresholds dictated by the terminal voltages, not currents. In principle, a large enough MOS device can pass any finite amount of current, but no MOS device can maintain appreciable small-signal current gain per unit quiescent current when the gate-to-source V_{GS} and drain-to-source V_{DS} voltages drop to zero. Therefore, operation of a receiver in the current domain is preferred when large-signal handling is required.

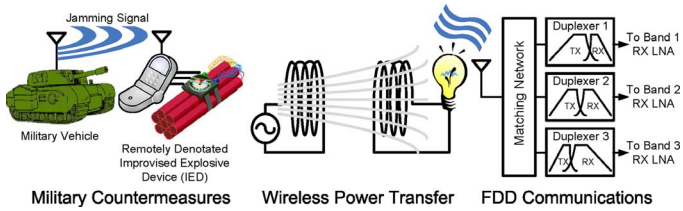

Fig. 1. Motivations for large-signal handling receivers: large potential out-of-band interferer sources.

Most radio receivers employ about three orders of magnitude of voltage gain between the antenna and ADC input. However, for an out-of-band blocker that is already nearly as large as the supply rails, *any* voltage gain would result in gain desensitization of the receiver. Although on-chip filtering at RF may be employed to attenuate the magnitude of out-of-band blockers with respect to in-band signals at a current-to-voltage conversion, such filtering is typically composed of a single RLC tank with only 3–7 dB of relative attenuation at a 100–200 MHz frequency offset.

Filtering of out-of-band blockers is performed far more efficiently at baseband. One way of seeing this is to note that monolithic baseband filtering is accomplished through frequency-selective impedance division between resistive and capacitive elements. For a given order filter, the maximum achievable attenuation is limited by the Q of the capacitor, which is normally several orders of magnitude higher than that of the inductor required for filtering at RF.

Based on these realizations, the design of an optimal large-signal handling direct-conversion receiver would operate primarily in the current domain at RF, with as few current-to-voltage conversions as possible. The principal current-to-voltage conversion should occur at baseband where a large filtering capacitor can result in a substantial attenuation of an out-of-band blocker relative to the desired signal.

Indeed, these sorts of current-mode RF techniques have recently enjoyed a renaissance in the form of passive mixer receiver architectures, an example of which is shown in Fig. 2. Such architectures utilize a low-noise transconductance amplifier (LNTA) to convert the receiver input voltage (or perhaps

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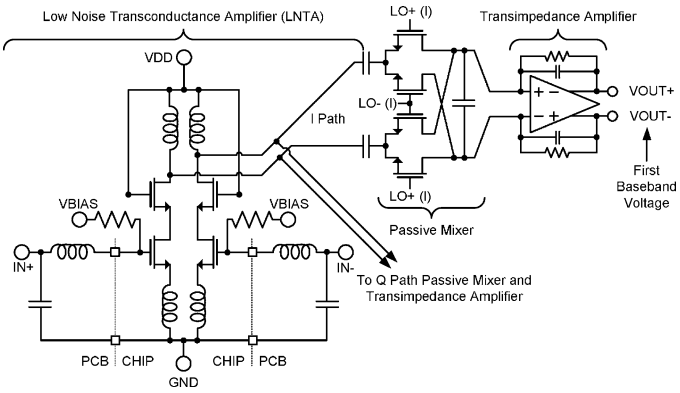

Fig. 2. Basic passive mixer-based receiver front-end architecture, showing inherent low-pass filtering prior to first baseband voltage.

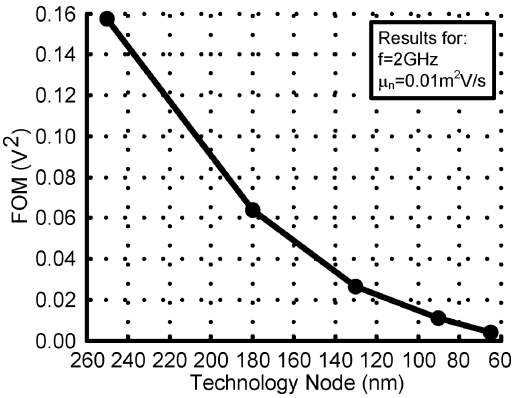

Fig. 3. Proposed passive mixer FOM as a function of technology node based on data from [1].

a subsequent RF voltage) into a current which is then commutated by a set of MOS pass transistors that perform the downconversion to baseband frequencies. It is worth pondering briefly why current mode passive mixer based systems have gained increasing prominence over the last decade. One reason is that scaling has considerably reduced the power required to fully transition a MOS device gate voltage from ground to supply. As the minimum device length shrank, the maximum achievable $\mathrm{W/L}$ ratio (corresponding to minimum achievable on resistance) increased for a given mixer driver power dissipation. This permitted the handling of larger ac currents while bounding the mixer input voltage swing to the level required to keep the LNTA cascode device in saturation. This effect can be captured in (1) in which a passive mixer figure of merit (FOM) is proposed which is composed of the product of the power required to drive a pair of I/Q passive mixers and the passive mixer on resistance. Clearly, a lower FOM is superior than a higher FOM in this case. The FOM is seen to reduce dramatically with technology node in Fig. 3:

$$\begin{aligned}\mathrm{FOM_{Passive\ Mixer}} &= \mathrm{P_{DRIVE}} \cdot \mathrm{R_{ON}} \\ &= \frac{8WLC_{ox}V_{DD}^2 f}{\frac{W}{L}\mu_n C_{ox}(V_{DD}-V_{TH})} = \frac{8L^2V_{DD}^2 f}{\mu_n(V_{DD}-V_{TH})}. \end{aligned} \quad (1)$$

In the context of a large-signal handling receiver, however, recently reported passive mixer-based receiver architectures remain limited in their signal handling capability by the initial V-I conversion in the receiver. The authors of [2] proposed the use of an inductively degenerated common-source LNA but did not build it. Later, the architecture proposed in [2] was implemented, both with a stacked NMOS/PMOS inductively degenerated LNA [3] and with a cascoded NMOS inductively degenerated LNA [4]. In the case of [3], large-signal operation was not reported. In [4] input $P_{-1\ \mathrm{dB}}$ was reported to be -14 dBm but it is unclear if this number corresponds to in-band signals. The receiver in [5] reports an out-of-band desensitization of -24 dBm at a 400-MHz LO offset frequency, with the performance improving to about 0 dBm by an offset of 2.4 GHz. It appears that in these cases that the LNA or LNTA is limiting the desensitization performance of the receiver to well below a magnitude commensurate with that of the supply rail. Hence, there exists a need to design an LNA or LNTA with which rail-to-rail input operation of the receiver may be achieved in order to fully enable the large-signal handling potential of passive mixer-based receivers.

II. Prior Art in PMOS/NMOS LNAs and LNTAs

Scaling has also permitted the utilization of PMOS/NMOS RF low-noise amplifiers in recent years. As such, there has been no shortage of activity in this area. Like PMOS/NMOS baseband "rail-to-rail" opamp architectures, such LNAs and LNTAs have the potential to operate over a wider input range than do amplifiers utilizing only one type of MOS device.

A. Current Sharing

Many PMOS/NMOS LNA or LNTA architectures present in the literature exploit the availability of both types of device to take advantage of the current sharing enabled by stacking two single-stage amplifiers operating in parallel from a small-signal perspective. For example, [3], [5]–[7] all stack NMOS and PMOS common-source (CS) amplifiers, while [8] stacks NMOS and PMOS common-gate (CG) amplifiers. The work in [9] exploits current sharing between parallel CS and CG stages, while the transconductor in [10] exploits current sharing within a cross-coupled CG/CS stage. The work in [11] utilizes a PMOS device as an active load in a current-sharing configuration with a CS amplifier in the final stage of a high voltage-gain LNA for UWB receivers.

B. IM2 Cancellation

Television tuners must process a signal spanning over a decade of frequency range with widely varying signal strength across the band at any given time. Because of this, not only is odd-order intermodulation distortion (IMD) important, but even-order IMD and harmonic distortion (HD) can show up almost anywhere within the signal band. Although differential circuits can improve the IIP2 performance of RF amplifiers, the single-ended cabling present in these systems necessitates at least one single-ended amplifier within the system. One solution to this problem is to place NMOS and PMOS CS stages in parallel without current sharing [12]. In this case, the parallel NMOS and PMOS stages behave as two halves of a differential circuit assuming that they can be matched. This concept has also recently been extended [13] to confer the benefit of IM2 cancellation on a CG/CS amplifier utilizing the noise cancellation concept described in [14]. The work

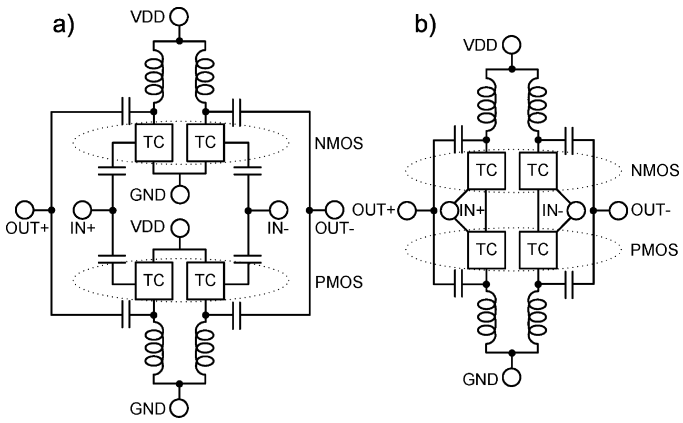

Fig. 4. General CMOS push-pull LNTA topology. (a) Parallel. (b) Stacked.

presented in [7] utilizes the characteristics of a PMOS CS stage to cancel the second-order nonlinearity of an NMOS CS stage within another noise-cancelling CG/CS LNA architecture.

C. IM3 Improvement in Common-Gate/Common-Source Noise-Cancelling LNAs

Noise-cancelling LNAs that combine the wideband input matching properties of the CG LNA with the high transconductance values associated with a CS LNA have been reported extensively since the work performed in [14]. Combined CG/CS LNA architectures can also be engineered such that nonlinear distortion components arising from the common-gate amplifier can be made to cancel [15]. The architecture of [16] exploits the fact that the derivative of the common-gate transconductance g'_m of NMOS and PMOS common-gate devices is different, while g_m and g''_m remain the same. This results in an extra degree of freedom by which additional suppression of third-order distortion may be achieved. However, this IM3 cancellation scheme is relevant only for blocker levels as large as -20 dBm, as higher-order distortion terms are not canceled.

Remarks

Despite the profusion of PMOS/NMOS LNA and LNTA architectures, none purport to exhibit any wide-swing or large-signal handling capabilities. Although the PMOS/NMOS push-pull LNAs that provide IM2 cancellation ameliorate the abrupt turn-off behavior of the MOS device, no evidence of odd-order IMD cancellation or large-signal handling is demonstrated or claimed for these architectures. However, it seems as if the input–output characteristic stitching behavior inherent in class-AB push-pull topologies is a promising path towards enabling high linearity performance for a large voltage signal at the receiver input. In order to enable highly linear behavior for an even larger input, the push–pull LNTA should comprise a differential topology, as depicted in Fig. 4. Missing in Fig. 4 are the actual transconductance (TC) elements to be used, which is the topic to be considered next.

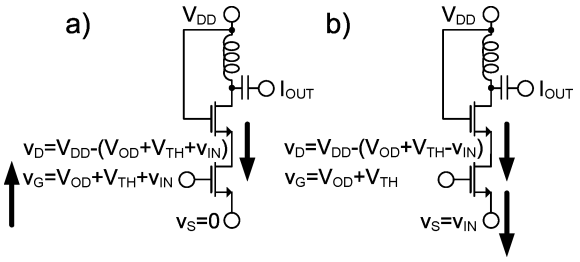

Fig. 5. Available signal swing of cascoded common-source and common-gate transconductors. (a) Common-source. (b) Common-gate.

III. Evolution of Wide-Swing PMOS/NMOS Common-Gate LNTA

A. Considering a Common-Source Push–Pull LNTA

In addition to providing a voltage-to-current conversion at the input, the LNTA should also provide a measure of buffering between the passive mixer and the antenna to prevent LO re-radiation. Using a cascode device to separate the transconductor from the passive mixer dramatically reduces the extent to which this phenomenon occurs. Unfortunately, the use of this technique is not consistent with the practical realization of a wide-swing common-source push–pull LNTA. To see why, one may consider as in Fig. 5(a) a simple cascoded common-source amplifier. In the typical case, the cascode device is sized to be the same as the input device in order to minimize the parasitic capacitance between the two nodes [17]. This design choice is applied to all designs considered in this manuscript. It can be shown using the square-law MOSFET I-V model that the voltage range over which the input device remains in the saturation region is given as

$$\frac{V_{DD}-V_{TH}}{2}-V_{OD}>v_{IN}>-V_{OD}$$
$$V_{OD}=V_{GS}-V_{TH}. \tag{2}$$

B. Considering a Common-Gate Push–Pull LNTA

By contrast to the common-source case, the transconductor drain voltage of the cascoded common-gate amplifier tracks the input voltage in the absence of the body effect, as depicted in Fig. 5(b). In this case, the device V_{DS} is roughly constant and it can be shown using the square-law MOSFET I-V model that the voltage range over which the input device nominally remains in the saturation region is given by (3). It can be seen that for a small V_{TH} and V_{OD}, the common-gate amplifier maintains nearly twice the available signal swing as does the common-source amplifier, making it more suitable for a large-signal handling LNTA;

$$V_{OD}>v_{IN}>2V_{OD}+V_{TH}-V_{DD}. \tag{3}$$

One disadvantage of the common-gate LNTA is the relatively high NF, traditionally expressed in simplified form as $1+\gamma_{\mathrm{Noise}}$. Another disadvantage of the common-gate LNTA is that the small-signal transconductance is fixed by the 50 Ω real impedance at the input that is required for optimal power matching to the driving source. The resultant 20-mS transconductance is 2–3 times less than what might be achieved in an

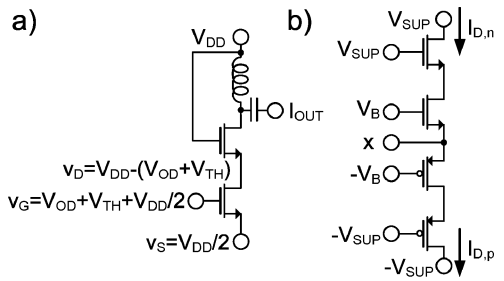

Fig. 6. (a) Biasing strategy for stacked class-AB common-gate LNTA. (b) Circuit structure utilized for quantitative analysis of LNTA.

inductively degenerated common-source amplifier. Choosing the common-gate LNTA topology thus places an atypically large noise burden on the passive mixer and baseband. However, for the purposes of the project reported in [18] for which this LNTA was intended, the capability of handling a large input signal was paramount. Simulations of the receiver blocks in [18] show that the small-signal NF is indeed dominated by the baseband circuitry blocks immediately following the passive mixer.

C. Device Sizing in a Stacked Topology

Given that a CMOS common-gate LNTA is most desirable for large input signal handling, the question remains whether to implement it in a parallel or stacked topology, as depicted in Fig. 4. The parallel topology clearly gives a wider signal swing, but the stacked topology results in quiescent current savings. It was decided here to obtain the best of both worlds by increasing the power supply rail voltage to allow for greater signal swing and by stacking the transistors. Once the decision to design with a stacked topology is made, the next design choice is to determine the approximate sizing and quiescent current consumption of the stacked structure. One obvious constraint is the requirement of a differential transconductance equal to about $g_m = 1/(50\ \Omega)$. The required single-ended, single-device transconductance is the same as this value. Employing the biasing strategy depicted in Fig. 6(a), it can be shown that when using low threshold MOS devices with $V_{TH} = 250$ mV and a supply voltage $V_{DD} = 1.5$ V, the requirement on V_{OD} is given by (4) and evaluates to 150 mV. Along with the g_m requirement, this dictates the device width sizing and sets a quiescent current per LNTA half of about 1.5 mA:

$$\frac{1}{2}\left(\frac{V_{DD}}{2} - V_{MG} - V_{TH}\right) = V_{OD}. \tag{4}$$

IV. General Theory of LNTA Operation

Visually considering the operation of a stacked push-pull LNTA of general transconductor as in Fig. 7 shows that each of the transconductors operates for slightly over one-half of a sinusoidal input cycle. The complete sinusoidal output is obtained by splicing together the ac output waveforms in the current domain via capacitive coupling. When the NMOS and

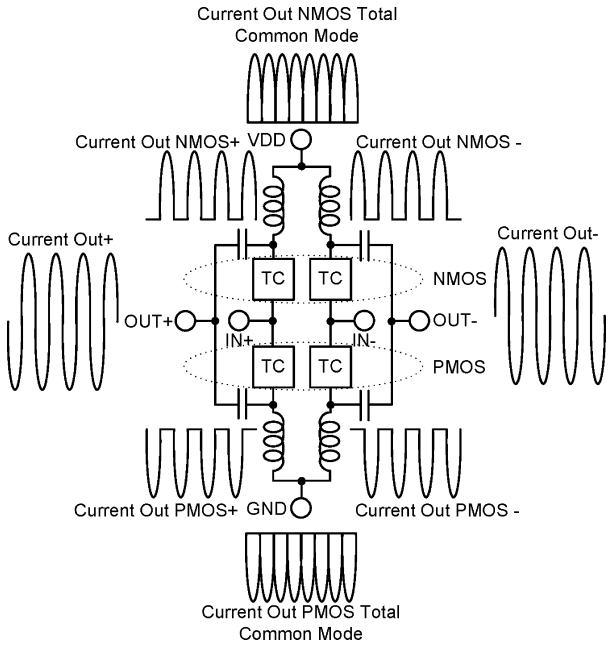

Fig. 7. Stacked push-pull LNTA large-signal current flows.

PMOS half-cycle currents are combined, the large even-order harmonics resulting from the turn-off of the transconductor devices are largely canceled. Although slightly imbalanced NMOS and PMOS devices result in some remaining even-order distortion products on each of the LNTA single-ended outputs, they are attenuated again by about an order of magnitude in the differential-mode output current due to their common-mode nature.

Whether implemented with common-source or common-gate devices, one important implication of utilizing a differential push-pull LNTA is the generation of low-frequency even-order (including dc) IMD current in the common-mode output, as depicted in Fig. 7. Both NMOS and PMOS transconductors conduct current primarily in one direction, realizing a strong second-order nonlinearity which gives rise to a dc component in the output current of each device. This current passes through the inductors to the supply rails where it results in a static power dissipation proportional to the amplitude of the input signal. In a more accurate sense it is not only dc but the low-frequency envelope which is generated by the second-order transconductor nonlinearity. Although matching the characteristics of NMOS and PMOS devices at the quiescent point is possible in principle via the use of separate constant-g_m biasing networks, maintaining exactly the same operation over the entire signal swing is in general not possible due to the different mobility degradation characteristics of the device types. In this case, the low-frequency large-signal envelope current generated by the NMOS and PMOS halves of the circuit may differ by 20%–30% even if the quiescent currents are matched. In order to regulate the common-mode input voltage, this difference current must be sourced by a common-mode feedback OTA itself class-AB in nature, as the OTA output stage current should only be large when the LNTA input signal is large.

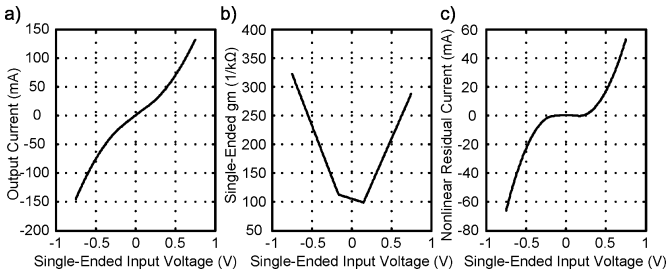

Fig. 8. Calculated output characteristics of the single-ended LNTA for square-law MOSFET model. (a) Output current. (b) Transconductance. (c) Nonlinear residual current after removal of small-signal linear fit.

V. Obtaining Near-Constant LNTA Transconductance

A. General Concept

Assuming that the MOSFET devices of the LNTA can be well-modeled by the long-channel square-law (5) and denoting the single-ended input voltage of the LNTA as the variable x, the I-V relation of one half of the LNTA can be expressed as in (6) and (7), where V_{DS} is treated as a constant. This expression assumes a split supply in order to exploit the symmetry of the stacked LNTA in the analysis. In this case, as illustrated in Fig. 6(b), $x = 0$ V in the quiescent condition, while $V_{SUP} = V_{DD}/2$. Both the I-V and g_m-V relations are plotted in Fig. 8, where the roughly constant region in the center predicted by (8) is tilted slightly due to the mismatched characteristics of the NMOS and PMOS devices:

$$I_{sq} = \frac{1}{2}\frac{W}{L}\mu_0 C_{ox}(v_{OD})^2(1+\lambda V_{DS}) \tag{5}$$

$$\begin{aligned} v_{OD} &= \max(V_G - v_S - V_{TH}, 0) \\ v_{OD,n} &= \max(V_B - V_{TH,n} - x, 0) \\ v_{OD,p} &= \max(V_B - V_{TH,p} + x, 0) \end{aligned} \tag{6}$$

$$\begin{aligned} I_{n,sq}(x) &= \frac{1}{2}\frac{W_n}{L}\mu_{n,0}C_{ox}(v_{OD,n})^2(1+\lambda_n V_{DS}) \\ I_{p,sq}(x) &= -\frac{1}{2}\frac{W_p}{L}\mu_{p,0}C_{ox}(v_{OD,p})^2(1+\lambda_p V_{DS}) \\ I_{tot,sq}(x) &= I_{p,sq}(x) + I_{n,sq}(x) \end{aligned} \tag{7}$$

$$g_{m,tot,sq}(x) \propto \begin{cases} K(V_B - V_{TH} - x) & x < -(V_B - V_{TH}) \\ 2K(V_B - V_{TH}) & -(V_B - V_{TH}) < x < V_B - V_{TH} \\ K(V_B - V_{TH} + x) & x > V_B - V_{TH} \end{cases}$$

$$K \approx \left(K_n = \frac{1}{2}\frac{W_n}{L}\mu_{n,0}C_{ox}\right) \approx \left(K_p = \frac{1}{2}\frac{W_p}{L}\mu_{p,0}C_{ox}\right). \tag{8}$$

In order to create a I-V characteristic that is roughly linear over the entire input span, it is required to reduce both the current (and equivalently, transconductance) as an increasing function of $\max(|x - V_{OD}|, 0)$. Multiplying the LNTA I-V characteristic by a function similar to that shown in Fig. 9 is a good way to accomplish this objective, especially given that nonlinear mobility degradation effects operating on the input devices in the LNTA already do this to a certain extent.

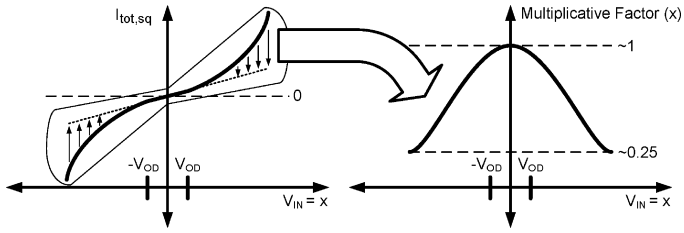

Fig. 9. Intuitive shape of multiplicative term required to linearize LNTA.

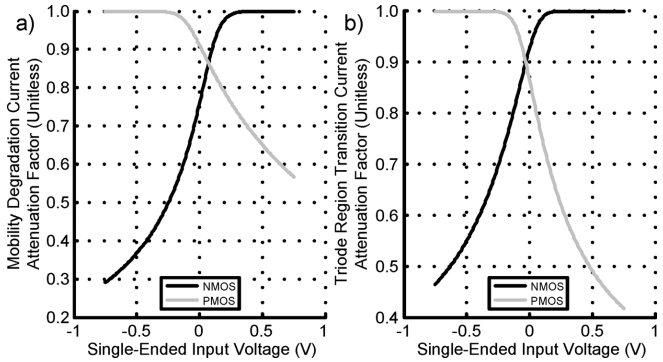

Fig. 10. Nonlinear effects contributing to the linearization of the LNTA for large signals. (a) Mobility degradation ($VS_n(x), VS_p(x)$). (b) Transition into triode region ($F_{s,n}(x)$, $F_{s,p}(x)$).

B. Mobility Degradation Effects

As described in [19, p. 589], both the horizontal and vertical electric fields in the drain-to-source channel reduce the carrier mobility within the MOSFET as a function of v_{OD} (9) and (10), where $v_{\rm sat}$ is the saturation velocity of carriers within the channel. For the purposes of the analysis here, this effect is consolidated into multiplicative factors $VS_n(x)$ and $VS_p(x)$ that are used to multiply each of the two device type currents in (7):

$$\mu_{\rm eff} = \frac{\mu_0}{1 + (\theta + C)v_{OD}} = \mu_0 VS(x) \tag{9}$$

$$C = \frac{\mu_0}{2L_{\rm eff}v_{\rm sat}}. \tag{10}$$

Due to the different scattering properties of holes and electrons, both μ_0 and θ differ considerably between NMOS and PMOS devices. As a result, VS_n and VS_p can differ considerably, lending an asymmetry to the large-signal operation of the LNTA half-circuit, alluded to earlier in Section IV. For $L_{\rm eff} = 70$ nm and $v_{\rm sat} = 1\times10^5$ m/s and for extracted values of θ_p, θ_n, $\mu_{0,n}$, and $\mu_{0,p}$, $VS_n(x)$ and $VS_p(x)$ are plotted in Fig. 10(a). Incorporating these effects into the MOS I-V relation yields the following:

$$I_{tot,md}(x) = I_{p,sq}(x)VS_p(x) - I_{n,sq}(x)VS_n(x). \tag{11}$$

Plotting (11) as a function of input voltage would yield a rather asymmetric transconductance curve. This asymmetry is

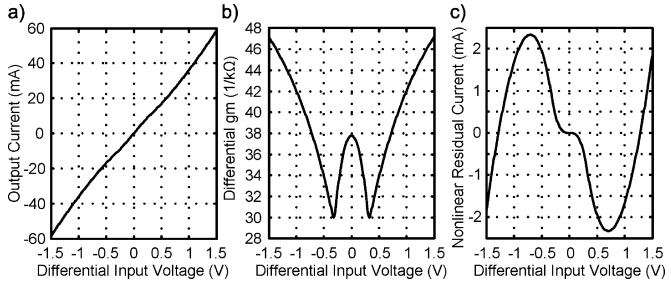

Fig. 11. Calculated output characteristics of the differential LNTA for MOSFET model incorporating mobility degradation effects. (a) Output current. (b) Transconductance. (c) Nonlinear residual current after removal of small-signal linear fit.

eliminated by taking the differential output current using the relation in (12) (which neglects the effects of mismatch), resulting in the curves shown in Fig. 11. As even-order distortion products are of minimal concern in the current output of the LNTA when used in the receiver described in [18], the relation in (12) is the one of immediate relevance to the design, as odd-order IMD products end up dominating the in-band output error:

$$I_{diff,tot,md}(x) = \frac{1}{2}(I_{tot,md}(x) - I_{tot,md}(-x)). \tag{12}$$

C. Transition Into Triode Region, Body Effect, and Subthreshold MOS Conduction

In addition to providing a significant measure of isolation between the receiver input and the passive mixer, the presence of the cascode devices also maintains a relatively constant V_{DS} across the input devices, as described in Section III-B. As the magnitude of the input voltage increases, increasing the V_{GS} of the input device, the input device begins to transition into the triode region of operation. Multiplying the I-V relation by a "saturation function" F_s [20] can account for the effect of this operating region transition on the drain current of the input transistor:

$$F_s = \frac{\frac{V'_{DS}}{V_{D,SAT}}}{\left(1 + \left(\frac{V'_{DS}}{V_{D,SAT}}\right)^{\beta}\right)^{1/\beta}}. \tag{13}$$

For the purposes of this analysis, β_p is taken to be 1.4 for PMOS devices and β_n to be 1.8 for NMOS devices as in [20]. Although in principle $V_{D,SAT} = v_{OD}/(1 + C(v_{OD}/(1 + \theta v_{OD})))$ to account for mobility degradation effects, it was found during the course of this study that modeling $V_{D,SAT} = v_{OD}$ produced a more faithful representation of the qualitative results obtained in simulation.

Due to the smooth transitioning of the input device into the triode region and due to the body effect of the cascode device, the V_{DS} of the active input device actually increases by a small amount as the input voltage magnitude approaches its maximum. It was found in simulation that incorporating this effect into the analytical model roughly entailed modifying (13) to (14), where $K = 0.2$. Replacement of V_{DS} with $V_{DS,Initial} \pm K \cdot x$ was also performed in the modeling of the channel-length modulation:

$$F_{s,n} = \frac{\frac{V_{DS,Initial} - K\cdot x}{V_{D,SAT}}}{\left(1 + \left(\frac{V_{DS,Initial} - K\cdot x}{V_{D,SAT}}\right)^{\beta_n}\right)^{1/\beta_n}}$$
$$F_{s,p} = \frac{\frac{V_{DS,Initial} + K\cdot x}{V_{D,SAT}}}{\left(1 + \left(\frac{V_{DS,Initial} + K\cdot x}{V_{D,SAT}}\right)^{\beta_p}\right)^{1/\beta_p}}. \tag{14}$$

Although the terms in (14) are of a different form than those in (9), when plotted as a function of x in Fig. 10(b), they have roughly the same qualitative behavior. Adding them to the total current equation yields the following:

$$I_{tot,triode}(x) = I_{p,sq}(x)VS_p(x)F_{s,p}(x) - I_{n,sq}(x)VS_n(x)F_{s,n}(x). \tag{15}$$

For even more accurate modeling, the body effect is added to the overall current equation through the substitutions as

$$V_{TH,p} = V_{TH,0,p} + \gamma_p[\sqrt{2\Phi_F + V_{SUP} - x} - \sqrt{2\Phi_F}]$$
$$V_{TH,n} = V_{TH,0,n} + \gamma_n[\sqrt{2\Phi_F + V_{SUP} + x} - \sqrt{2\Phi_F}]. \tag{16}$$

Infinite derivatives of the g_m-V curve as seen in Fig. 11(b) cannot exist in a physical device. Properly modeling this section of the curve requires a smooth transition of the MOS region of operation from strong to weak inversion. This can be done by dividing I_{sq} by n and replacing v_{OD} with the expression in (17) [21], where the value of n represents the subthreshold parameter and can be modeled as $1 + \gamma/2\sqrt{2\Phi_F - V_{BS}}$ [22]. For the low-V_{TH} transistors used in the LNTA design, $n \approx 1.05$ and is only a very weak function of the value of x:

$$v_{OD,n} = 2nV_t \ln\left(1 + \exp\left(\frac{(V_B - V_{TH,p} + x)}{(2nV_t)}\right)\right)$$
$$v_{OD,p} = 2nV_t \ln\left(1 + \exp\left(\frac{(V_B - V_{TH,n} - x)}{(2nV_t)}\right)\right) \tag{17}$$
$$V_t = \frac{kT}{q}. \tag{18}$$

With these changes made to the model, the differential I-V and g_m-V curves appear as in Fig. 12. In this case, the transconductance is constant to within $+/-10\%$ over the entire input range. It is important to note that while the effects due to mobility degradation in the MOS devices are mostly predetermined due to the constraint that the device lengths (especially those of the PMOS) must be near the minimum allowable by the process lithography, the properties of $F_{s,p}$ and $F_{s,n}$ may be engineered in order to achieve quasi-linear results similar to those depicted in Fig. 12 by altering the abruptness of the transition of the triode region.

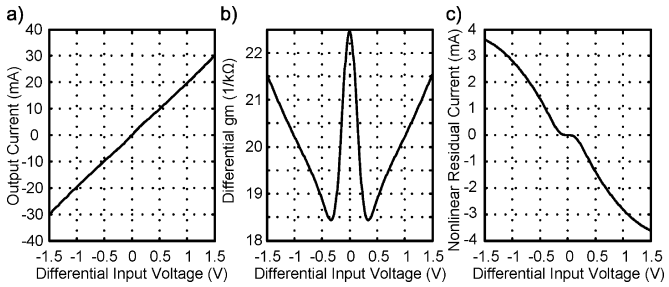

Fig. 12. Calculated output characteristics of the differential LNTA for MOSFET model incorporating all listed effects. (a) Output current. (b) Transconductance. (c) Nonlinear residual current after removal of small-signal linear fit.

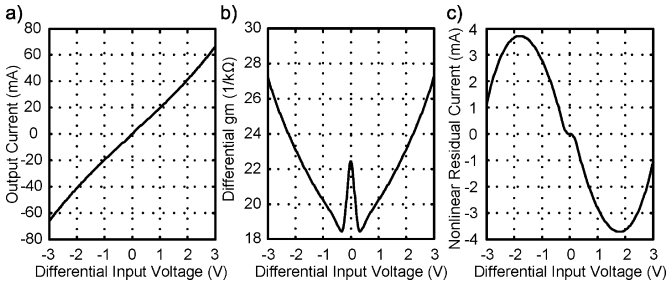

Fig. 13. Calculated output characteristics of the differential LNTA for MOSFET model incorporating all listed effects, for wide input range. (a) Output current. (b) Transconductance. (c) Nonlinear residual current after removal of small-signal linear fit.

D. Total IMD Product Error as Function of Input Voltage Magnitude

Maintaining a relatively constant g_m in the LNTA in the manner described above substantially reduces the magnitude of the composite IMD products generated when large signals are applied. One way to think about this is to consider that the shape of the LNTA g_m-V curve starts out very similar to a pure second-order function (implying a pure third-order nonlinearity). Therefore, in a swept-amplitude IIP3 simulation using CW tones, the input-referred IMD power will begin rising with a slope of 3. As the amplitudes of the input blockers approach the minima of the g_m-V curve, the rate of increase in IMD product amplitude will decrease such that the input-referred IMD power curve begins to flatten out. Since the W-shape of the g_m-V curve implies a sinusoid-like nonlinearity, the terms of the Taylor series which approximate the nonlinearity alternate in sign, providing for a degree of cancellation of correlated IMD terms of higher order.

Eventually as the input signal voltage magnitude increases, it traverses the outer tails of the W-shaped g_m-V curve. When zoomed out, as in Fig. 13, the W-shape again appears to be roughly a pure second-order function. Therefore, it is expected that the input-referred IMD power rises at a slope of 3 again. In fact, this predicted behavior is observed in Fig. 14(a), where two equal-amplitude CW blockers have been applied to the I-V model in Fig. 13 via a differential 50-Ω source impedance. It can be seen in Fig. 14 that the input-referred IMD power under large blocker application is about 40 dB less than if it had continued to rise at a slope of 3 for the entire sweep.

Another very important type of blocking condition is that of asymmetric blocking. This situation wherein the blocking scenario is dominated by one very large jamming signal arises frequently in applications such as FDD communications (where the TX leakage dominates), in implantable biomedical circuits requiring both power and data wireless links (where the power link dominates)[23], and in military environments where large jammers used to prevent enemy communications result in co-location interference for friendly communications. In this case, a very large CW blocker is applied to the transfer function in Fig. 13 along with a smaller CW blocker of 29 dB lower power. It is shown in Fig. 14(b) that the conclusions of the symmetric blocking condition also hold here.

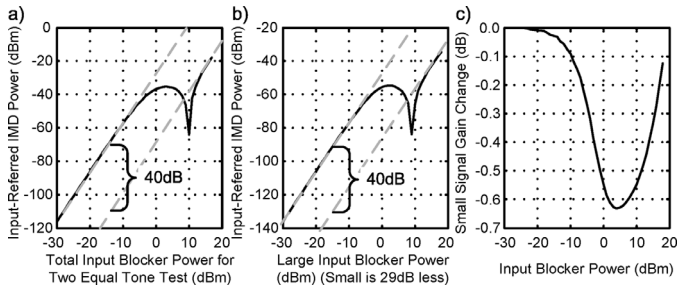

Fig. 14. Calculated input-referred upper-sideband IMD products for two-CW-tone blocking scenario with slope-of-3 labels. (a) For two equal magnitude CW blockers. (b) For asymmetric CW blockers. (c) Desensitization test result: small-signal gain change as function of input blocker power.

E. LNTA Compression

A relatively constant g_m in the LNTA also directly implies that its small-signal gain compression is bounded, at least for the foregoing models. To see why, one may consider an input consisting of one large blocker and one small desired signal. In this case, the Taylor series of the nonlinear I-V curve may be taken with respect to the small desired signal and the output expressed as

$$i_{OUT}(t) \approx g_m(v_{\mathrm{BLOCKER}}(t))v_{\mathrm{DESIRED}}(t). \qquad (19)$$

The change in average LNTA transconductance as a function of input voltage can then be computed as (20).

$$\Delta g_m = E[g_m(v_{\mathrm{BLOCKER}}(t))] - g_m(0). \qquad (20)$$

Using (20) with reference to Fig. 13(b), it is intuitively expected that the LNTA experiences a reduction of gain as the amplitude of the blocker encompasses the two dips of the g_m-V curve but then sees a gain expansion as the amplitude of the blocker increases past these points. In fact, this behavior is seen in Fig. 14(c) where the desensitization test is performed (via numerical computation) by applying the small desired signal and large blocker to the LNTA input in series with a differential 50-Ω source resistance. The small desired signal power at the input of the LNTA is kept constant and changes in the output rms current level are reported in Fig. 14(c). In this particular case, the 1-dB desensitization point *does not exist*. The ultimate limiting mechanism for the LNTA desensitization will be discussed in Section VI-C.

F. Modeling Thermal Effects

Although the foregoing analysis is presented in a didactic sense primarily to show which nonlinear effects contribute to

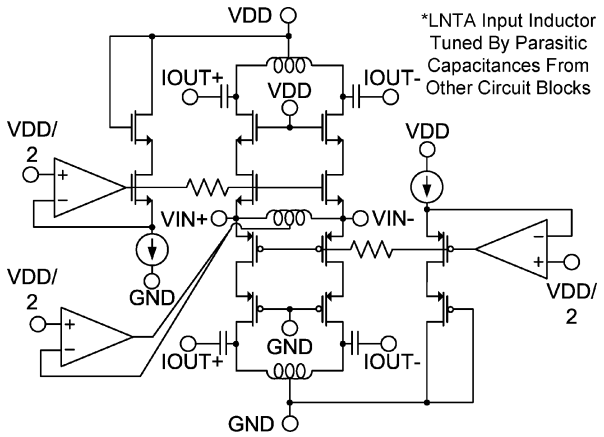

Fig. 15. Simplified schematic of implemented LNTA.

the overall quasi-linear behavior of the proposed LNTA structure, it may also be desirable to incorporate temperature-dependent effects. The two primary temperature-dependent effects in a MOSFET device are a reduction in threshold voltage V_{TH} and carrier mobility μ as temperature is increased [24, p. 189]. A simple way to incorporate these effects into the foregoing analysis is to make the substitutions below (21) where $\mathrm{K} = -2$ mV/°C (within a factor of 2) [24, p. 189]. The reader may note that due to the constant current replica biasing utilized in Fig. 15, V_B will track with any V_{TH} changes, but the quantity $V_{DS,Initial}$ will change by $-\Delta V_{TH}$:

$$\mu(T) \approx \mu(T_0)\left[\frac{T}{T_0}\right]^{-3/2}$$
$$V_{TH} \approx V_{TH}(T_0) - K(T - T_0). \tag{21}$$

It is also worthwhile to consider the effects of self-heating on the desired LNTA behavior. To estimate the temperature change in response to a large signal, the power dissipated per device and worst case device thermal resistance must be determined. Because the LNTA is quadrilaterally symmetric, with similar V_{DS} on all devices, approximately 1/8th of the total input power is dissipated in each device. Being smaller, the NMOS has higher thermal resistance than the PMOS. The average temperature rise within an NMOS device can be estimated using the expression (22), which incorporates the thermal resistance of a single finger R_{th} along with cross-heating terms for all other local device fingers, which are taken to be point heat sources for simplicity [25]. In the LNTA fabricated as part of the receiver described in [18], both the input and cascode devices were laid out immediately adjacent to one another. Based on the layout, the cascode devices will experience the largest temperature increase, and will therefore be examined below.

In (22), $k_{Si} = 1.5 \times 10^{-4}$ W/(μm°C), while the sizing of each of the 64 individual device fingers is given by $W = 0.52$ μm, $L = 70$ nm. The quantity $n = 32$ represents the number of fingers in a given sub-array. The abbreviations "O.C.F" and "I.F." stand for "other cascode fingers" and "input fingers," respectively

$$R_{th,casc} = \frac{1}{4k_{Si}\sqrt{WL}}$$

$$\Delta T_{avg} = P_{casc}R_{th,casc} + \frac{1}{2\pi k_{Si} n} \cdot \left(\sum_{i=1}^{n} \sum_{j \in O.C.F.} \frac{P_{casc}}{\sqrt{(x_i - x_j)^2 + (y_i - y_j)^2}} + \sum_{i=1}^{n} \sum_{j \in I.F.} \frac{P_{in}}{\sqrt{(x_i - x_j)^2 + (y_i - y_j)^2}} \right). \tag{22}$$

For a +20 dBm (100 mW) input signal, the power dissipated per device finger is 12.5 mW/64. Based on (22), this power dissipation, and the layout of the LNTA in [18], the average local temperature rise in the NMOS devices is about 9°C. This temperature rise is small and will have little effect on the nonlinear behavior of the LNTA, as will be evident from the temperature corner simulation results in the next section of this paper.

VI. Implementation and Simulation Results

Based on the foregoing calculations and intuition, a stacked push-pull common-gate LNTA was designed to operate under a nominal supply voltage of $1.5\ \mathrm{V} + / - 0.1$ V using low-threshold voltage devices in a 90-nm RF CMOS process. Shown using a simplified schematic in Fig. 15, the gate voltages of the input devices are defined with replica bias loops that ensure that the quiescent current flowing through the structure is proportional to the input bias current. The source voltages of the input devices are defined at $V_{DD}/2$ by a class-AB OTA. This LNTA design was eventually fabricated as part of a completely integrated receiver front end that was reported in [18] and [26]. To the knowledge of the authors of this paper, neither this LNTA structure nor its large-signal handling capabilities had been reported in the literature prior to the publication of [26]. Although the LNA architecture described in [8] also employed stacked common-gate devices, in the case of [8] the shared stacking node was the device drain, rather than the source as in Fig. 15. The architecture described in [16] does use stacked common-gate devices joined at the source node as part of a combined CG/CS architecture. However, the architecture in Fig. 15 differs from the common-gate section in [16] due to the use of cascode devices as linearizing elements, its differential nature, its input–output characteristic stitching in the current domain, and its explicit large-signal push–pull operation enabled by the class-AB OTA.

A. Noise Performance of Proposed LNTA

The total simulated small-signal NF of the LNTA is 1.8 dB at the tuned center frequency of 2.14 GHz. It is acknowledged that this represents a low NF for a CG amplifier and that if measured the NF might be somewhat higher. For example, even CG LNAs using g_m-boosting [27] and feedback [28] to improve the NF only obtain a measured NF of about 2.5–2.8 dB. One reason that the simulated NF may be low is that the extracted $\gamma_{\mathrm{Noise},\{n,p\}} = \{0.5, 0.4\}$ for the input devices, which may reflect a modeling inaccuracy.

However, the extracted values for γ_{Noise} may not be significantly far off. Reports of $\gamma_{\mathrm{Noise}} \approx 0.66$ in deep submicrometer devices [29], [30] do exist in the literature. Furthermore, the input devices of the LNTA are operated in moderate inversion, which may push the effective γ_{Noise} towards 0.5 [31]. As

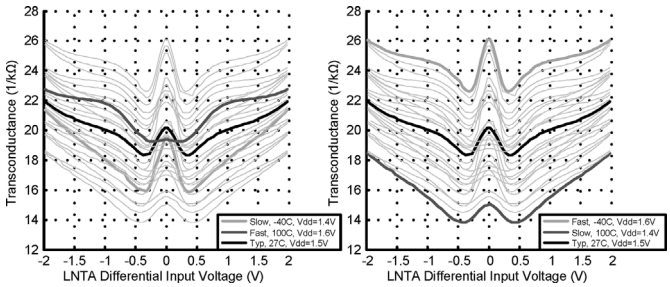

Fig. 16. Static LNTA simulation: transconductance as function of differential input voltage over corner. (Extreme corners highlighted.)

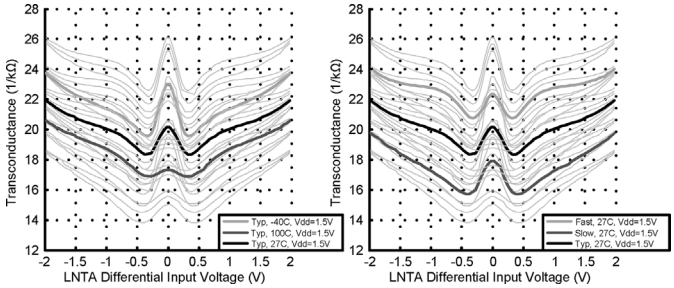

Fig. 17. Static LNTA simulation: transconductance as function of differential input voltage over corner. (Corner deviation from typical case highlighted.)

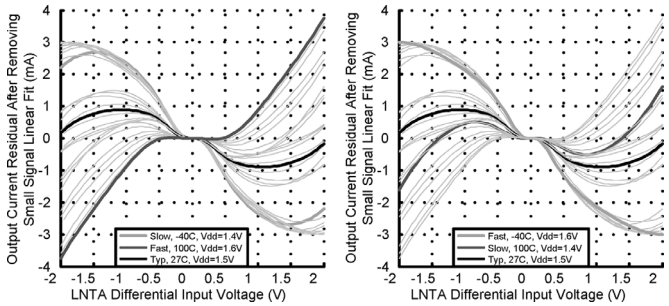

Fig. 18. Static LNTA simulation: nonlinear residual current as function of differential input voltage over corner. (Extreme corners highlighted.)

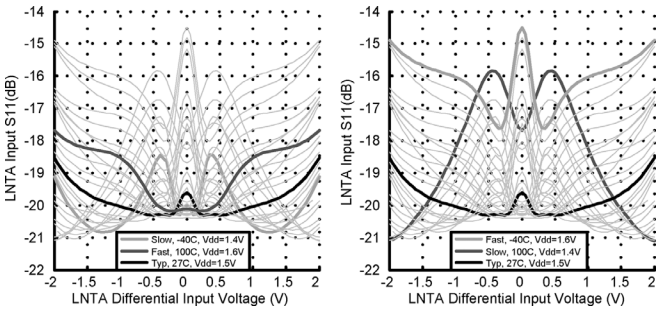

Fig. 19. Static LNTA simulation: S_{11} as function of differential input voltage over corner at 1.9 GHz. (Extreme corners highlighted.)

the input devices are operated with low V_{GS} and V_{DS}, $\gamma_{\rm Noise}$-increasing velocity saturation and hot carrier effects are expected to be quite small.

It can be shown that the small-signal NF of the proposed LNTA due to the MOSFET devices is given by (23), where $g_{m,LNTA}$ is the differential input transconductance of the LNTA, while $g_{d0,\{n,p\}}$ and r_o correspond to parameters of individual devices. In this case, $g_{m,LNTA}$ is somewhat larger than g_{d0} due to the various effects described in Section V, particularly channel length modulation. Furthermore, the feedback associated with the device drain–source resistance $r_o \approx 380\ \Omega$ is significant in the input devices used. These two results may help to explain the low simulated NF:

$$NF = 10\log_{10}\left(1 + \frac{\gamma_{\rm Noise,n} g_{d0,n} + \gamma_{\rm Noise,p} g_{d0,p}}{2g_{m,LNTA}\left(1 + \frac{1}{g_{m,LNTA} r_o}\right)^2}\right)$$
$$g_{d0} = \frac{W}{L}\mu_0 C_{ox} V S(0) v_{OD}(0). \quad (23)$$

B. Static (DC) Swept Input Simulations

The static current and transconductance of the LNTA in Fig. 15 are obtained by removing the ac-coupling capacitors from the output terminals and replacing them with ideal voltage sources that monitor the output current. Although memory effects are not taken into account in this simulation, it is found that the results gleaned from this simulation correspond well to the results involving the application of high-frequency signals to the LNTA while producing a reassuring correspondence with the memoryless analytical results presented earlier. Furthermore, ideally terminating the LNTA output reflects the fact that the frequency-translated baseband impedance seen at the output of the LNTA by large out-of-band blockers in a real receiver implementation is very small so long as large passive mixer switches and a large baseband filtering capacitor are used to realize a low impedance at the blocker baseband offset frequency.

Subtracting the currents from the two halves of the LNTA and dividing by two yields the differential output current and removes the second-order nonlinear terms from the I-V characteristic. Taking the derivative of the output I-V characteristic yields the g_m-V characteristic, which is plotted in Figs. 16 and 17. Removing the linear fit at the quiescent point from the output I-V characteristic also yields the residual-V characteristic, plotted in Fig. 18.

It is important to note that the constant-g_m behavior of the LNTA also guarantees a good 50-Ω match to the antenna over input signal swing. This is tested during the static (dc) sweep by performing an ac analysis at each point of the sweep to determine the return loss experienced by a small desired signal. The results of this test shown in Fig. 19 reveal that the S_{11} varies only a few dB from a minimum of -20 dB over the typical case rail-to-rail signal swing and never exceeds -14 dB. The S_{11} as a function of frequency for the typical and worst case corners are plotted in Fig. 20. The reader may note that although the LNTA is tuned to 2.14 GHz, it is operated with a receiver whose LO frequency is 1.9 GHz in [18].

The foregoing simulation results were obtained via constant-current biasing over 3-σ MOS device corner, temperature variation, and supply voltage variation. Even if all three parameters are simultaneously varied to their extremes, the defining characteristics of the LNTA are still present, namely a relatively constant g_m-V curve and a nonlinear current residual that is on the order of a magnitude less than the peak output current of 30

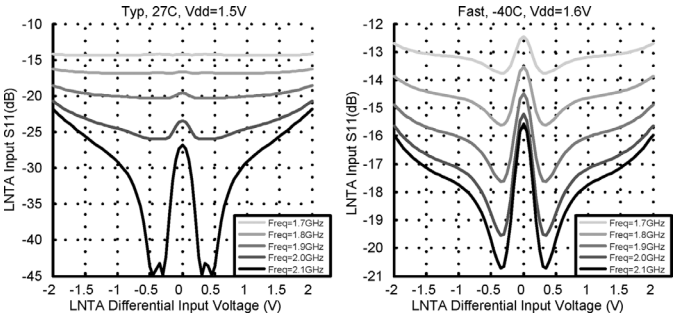

Fig. 20. Static LNTA simulation: S_{11} as function of differential input voltage over frequency.

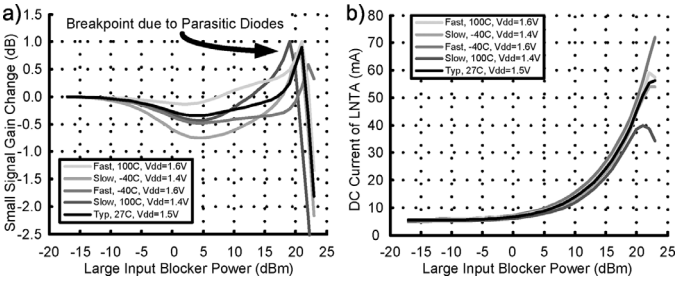

Fig. 21. Dynamic LNTA simulations using QPSS. (a) Small-signal gain change. (b) Quiescent current.

mA. With reference to Section V-F it can also be seen in Fig. 17 that the sensitivity of the g_m-V curve to temperature is relatively small.

C. Dynamic Swept Input Simulations

In order to confirm the link between the static swept input simulation and actual operation, several QPSS simulations were performed to examine the dynamic performance of the LNTA. In this case, the ESD typically present at the input of the LNTA is removed, although an ideal capacitor modeling the total capacitive load at the LNTA/chip input is utilized. Furthermore, the LNTA output capacitors are reattached and terminated to small-signal ground with the current outputs monitored. Each simulation result was run over the five extreme corners highlighted in Fig. 16. The differential input to the LNTA was applied in series with a 50-Ω source resistance.

1) Desensitization Simulations: Using a QPSS simulation, the small-signal transconductance gain of the LNTA is determined by applying a small desired CW signal at 1.9 GHz along with a large blocker CW signal at 1.81 GHz (a 90-MHz offset). At about $+21$ dBm (for the typical corner), the input voltage swing becomes clamped by the parasitic source terminal diodes to substrate/n-well of the NMOS and PMOS input devices, respectively. The sharp turn-on characteristics of the diodes result in abrupt limiting behavior, resulting in a very sharp drop in small-signal gain, registering a 1-dB desensitization point of $+22$ dBm for the typical corner.

2) DC Current Simulations: As described in Section IV, a large input signal is rectified by the second-order nonlinearities present in the LNTA devices and its dc component shunted to the supply rails through the output inductors. This effect is quantified in Fig. 21(b), where the LNTA quiescent supply current of 5.4 mA (including biasing) increases to 17.2 mA and 34.7 mA for $+12$ dBm and $+18$ dBm CW input blockers, respectively.

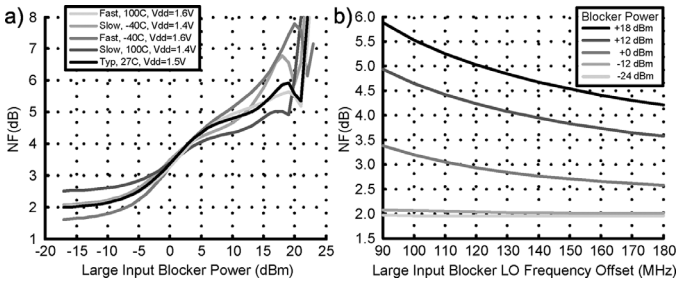

Fig. 22. Dynamic LNTA noise figure simulations as function of input blocker power using QPSS/QPNOISE. (a) Also over extreme corners. (b) Also over blocker offset frequency from LO (typical corner).

3) Noise Simulations: Performing a QPNOISE analysis while sweeping a single input blocker amplitude results in the curve shown in Fig. 22(a). In this case, the noise output was taken from 1.9 GHz with a blocker offset frequency of 90 MHz to reflect the measurements performed in [18]. It is seen at the typical corner that the NF rises from about 2.0 dB to 4.9 dB at $+12$ dBm blocker input power. Although this is a relatively large increase, it should be taken into the context that most wireless communications standards effectively allow for a 3-dB increase in input-referred error power under blocking conditions and that the total receiver small-signal noise figure is not likely to be dominated by that of the LNTA. The 1-dB NF increase point for this particular LO frequency/blocker offset frequency pair at the typical corner is -2 dBm.

This phenomenon of noise increasing with blocker amplitude is primarily due to upconversion of low-frequency flicker ($1/f$) noise from the input devices at moderate to large blocker amplitudes and to a lesser extent due to flicker and thermal noise from the cascode devices at the largest blocker amplitudes. Therefore, the upconverted noise falling within the desired signal bandwidth reduces as the large blocker frequency offset from the LO frequency is increased, as seen in Fig. 22(b).

4) Intermodulation QPSS Simulations: In order to confirm that the reduction in IMD at large signal amplitudes still holds for high-frequency inputs, two-tone blocking scenarios were applied to the LNTA, with the results shown in Fig. 23. For the asymmetric blocking condition, the larger/smaller CW blocker was placed at a 90/180 MHz LO offset. The equal-amplitude two-tone blocking condition is also tested with the same frequency offsets. Although the deep notch present in Fig. 14 has been noticeably attenuated, the reduction in IMD at large signal amplitudes is still about 40 dB over what would be predicted from extrapolating the slope-of-3 characteristic from smaller blocker power levels. It is likely that the presence of memory effects do not permit the precise cancellation of IMD products required to produce the deep notch.

It may also be noted that the simulated input-referred IMD power of the typical corner is about 10 dB less than the results shown in Fig. 14. Accounting for 6 dB is the fact that the peak-to-peak deviations of the simulated transconductance and nonlinear residual current in Figs. 16 and 18 are about half those in Fig. 12. Another 3 dB is due to the fact that the features of the curves in Fig. 12 are compressed along the x-axis by 1 dB with respect to those present in Figs. 16 and 18.

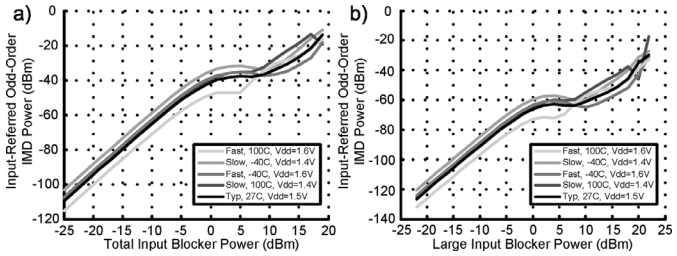

Fig. 23. Dynamic LNTA odd-order two-tone IMD simulations using QPSS. (a) For two equal magnitude CW blockers. (b) For two asymmetric blockers (second tone 29 dB less than large tone).

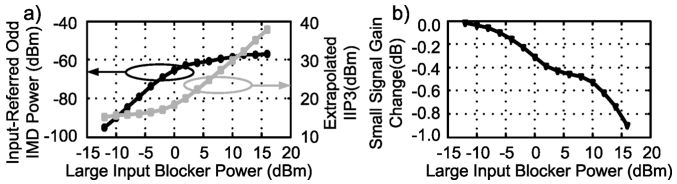

Fig. 24. LNTA+passive mixer two-CW tone IIP3 simulations (typical corner): (a) input-referred odd IMD, extrapolated IIP3, and (b) out-of-band small-signal gain desensitization.

Historically, integrated CMOS receivers were designed to handle blockers far smaller than those large enough to be considered "rail-to-rail." In this case, it made sense to quantify the linearity performance of the receiver as a metric (IIP3) extrapolated from the small-blocker slope-of-3 region of the IMD curve. However, with the advent of distortion-cancelling receiver architectures [18], [32], the possibility arose to operate the receiver in the presence of much larger blockers and to cancel any resultant distortion later in the signal path. In this case, it makes sense to utilize the IIP3 metric in such a way that sets an upper bound on the total input-referred IMD error. This information is important because it determines the dynamic range requirements of the nominally linear (main) receiver path that must process in-channel IMD products prior to cancellation at digital baseband. By extrapolating a slope-of-3 line from each point in the curve of Fig. 23, an individual IIP3 metric may be defined for each point. Assuming that the maximum blocker is a "rail-to-rail" $+12.5$ dBm signal, the upper input-referred IMD error bound is -57 dBm for the typical corner, corresponding to an large-signal extrapolated IIP3 value of $+32.8$ dBm.

The proposed LNTA is also simulated while terminated with the two 1/4-phase passive mixers described in [18] with the results shown in Fig. 24. For added accuracy, the LNTA and passive mixers are augmented with back-annotated layout parasitic capacitances prior to simulation. The passive mixers were loaded at baseband with the lumped frequency-dependent impedance presented by the receiver baseband circuitry. In order to permit accurate simulation results in a reasonable time, the passive mixer driving circuitry and LNTA internal opamps were made ideal in the simulation. It was confirmed that idealization of these subcircuits does not significantly perturb the results.

It can be seen that both of the principal findings of the stand-alone LNTA still hold here. The same asymmetric blocking conditions used to generate Fig. 23(b) were used here, resulting in a large-signal extrapolated IIP3 of $+33.0$ dBm at a $+12.5$ dBm large input blocker power. The 1-dB desensitization point is still very high, although for the particular passive mixer sizing implemented in [18] it is now dictated by perturbations of the 1/4-phase mixer duty cycle caused by the large-signal current. It can be shown that the net effect of the small shifts in duty cycle is to decrease the desired signal current flow to the baseband circuitry as the large blocker current is increased.

VII. Robustness of Constant-Transconductance Behavior Over PVT Variations

Referring to the results of previous section, especially Figs. 16 and 17, it is seen that while the absolute value of the g_m-V curve varies over PVT corners, it remains roughly constant and retains its W-like shape for a given realization. This behavior can be explained using the relations developed in Section V.

A. Invariance of Linearization Effects Over PVT

As described in Section V, the primary linearization mechanisms operating on the input devices of the LNTA are carrier mobility degradation and the transition into the triode region. In a deep submicrometer process, the mobility degradation is largely a result of normal-field effects that depend on the well-controlled thickness of the MOS oxide layer [33] and is hence relatively unaffected by PVT variations. The transition into the triode region depends on V_{DD}, V_{TH}, and V_{OD}. Using the relation (14) as a proxy, we see that its initial behavior is determined by $V_{DS}/V_{D,SAT}$. Relating $V_{DS}/V_{D,SAT}$ to the aforementioned quantities results in (24), where the body effect is neglected and the approximation is made that V_{GS} of the cascode device tracks that of the input device:

$$\frac{V_{DS}}{V_{D,SAT}} \approx \frac{V_{DD} - V_{GS} - \frac{V_{DD}}{2}}{V_{GS} - V_{TH}} = \frac{\frac{V_{DD}}{2} - V_{TH}}{V_{OD}} - 1. \quad (24)$$

In general, the supply voltage is well-regulated and does not vary much, while the value of V_{OD} for large input signals is dominated by the input signal itself. However, the transition into the triode region does depend on V_{TH}, which in turn depends on temperature, as described in Section V-F.

B. Variation Over Process Corner

Given that linearization effects remain roughly constant over variations in process corner (i.e., μ_0) and that $g_m \propto \mu_0$ in (8), it is expected that the g_m-V curves merely experience y-axis shifts with little shape change as the process varies. Examining Fig. 17 shows that this is indeed the case.

C. Variation Over Temperature

Like process corner variation, an increase in temperature results in a decrease in μ_0 and a negative y-axis shift of the g_m-V curve. In this case, however, V_{TH} also decreases, increasing the value of (24). This decreases the attenuation of the triode-region transition effect at large signal amplitudes, causing the outer edges of the g_m-V curve to increase in value relative to the center. Examining Fig. 17 shows that this is also indeed the case.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH RECENT WORK

Parameter	This Work (Simulated LNTA)	[5] (Simulated LNTA)	[9] (Measured LNA)	[16] (Measured LNA)	[35] (Measured LNA)
g_m (mS)(Half/Full-circuit)	40/20	100/50	N/A (LNA)	N/A (LNA)	N/A (LNA)
Power Gain (dB)	2.75	17	13	14.5	15.5
NF (dB)	1.8	<3	4	2.6	1.65
IIP3 (dBm)	+32.8 (Large-Signal)	+17	-10.2	+16	+22
IIP3 Notes	(+15.5 Small-Signal)	(R_L=10Ω)			
1-dB Desensitization (dBm)	+22	<+1	<-21	Not Reported	Not Reported
Desensitization Notes	(Typical Corner)	($B_{1dB} < P_{1dB}$-3dB)	($B_{1dB} < P_{1dB}$-3dB)		
Quiescent Power(mW)	8.1@V_{DD}=1.5V	16.8@V_{DD}=1.2V	0.72@V_{DD}=1.2V	17.4@V_{DD}=1.5V	24.2@V_{DD}=2.6V
FOM	862[1]	150	2	79	503
CMOS Technology (nm)	90	65	130	130	250

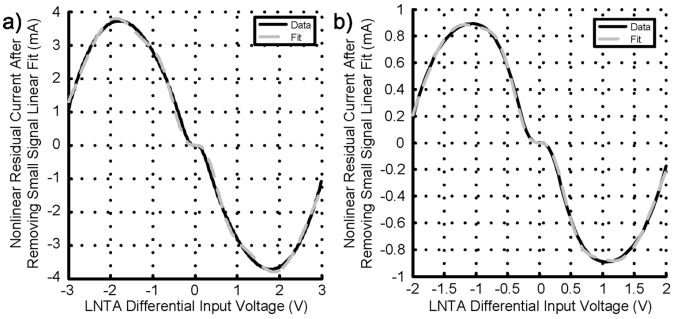

Fig. 25. Cubic-Gaussian basis fit to nonlinear residual current curves. (a) Fitting to calculated model. (b) Fitting to simulated model.

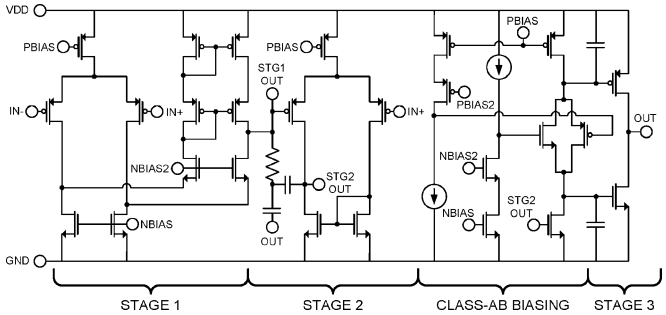

Fig. 26. Simplified schematic of implemented class-AB OTA for LNTA common-mode voltage maintenance.

VIII. HEURISTIC MODELING OF LNTA NONLINEARITY

When fully expanded, the analytical relations used to model the I-V characteristic of the LNTA in Section V are rather unwieldy. A fitted model may be more desirable for proper behavioral simulations. A clue to a possible basis set of low cardinality for fitting the LNTA transfer characteristic can be seen from the curves shown in Fig. 9. In this case, the original I-V characteristic is largely cubic in nature. This cubic relation is then multiplied by two relations of form similar to (9). Multiplying the two linearizing relations together yields a curve that looks very similar to a Gaussian function. Therefore, it is proposed here to model the LNTA nonlinearity with a set of functions of the form (25).

$$f(x,a,k) = ax^3 e^{-|k|x^2}. \tag{25}$$

For example, the I-V curve (in units of mA and V) of the calculated model nonlinear residual current in Fig. 13 can be well-represented by the summation of the functions $f(x, 0.01593, 0)$, $f(x, -2.442, 0.405)$, and $f(x, -12.63, 2.3)$, as shown in Fig. 25(a). The I-V curve of the simulated static nonlinear residual current (typical corner) can be well-represented by the summation of the functions $f(x, 0.03545, 0)$, $f(x, -1.736, 0.836)$, and $f(x, -8.867, 4.05)$, as shown in Fig. 25(b).

IX. BIASING OTA IMPLEMENTATION

Central to maintaining the proper input common-mode voltage of the LNTA is a class-AB biasing OTA. Assuming that the maximum input power required is +12.5 dBm, the maximum current to be sourced is 2 mA. In order to maintain a degree of margin, the OTA was designed to both sink and source up to 8 mA. Because the real part of the load impedance to be driven by the OTA is nominally 12.5 Ω (due to the two input terminals of the LNTA being shorted at low frequencies), to obtain an appreciable degree of loop gain for a small quiescent power draw, a multi-stage OTA topology is required. A three-stage reverse-nested-miller-compensated (RNMC) OTA topology [34] was sufficient to meet the requirements of this design and its schematic is shown in Fig. 26. It consumes a quiescent current of 900 μA.

X. LNTA SUMMARY AND RECEIVER MEASURED RESULTS

The simulated performance summary of the proposed LNTA is shown and compared to other works in Table I,[1] where a standard LNA FOM is utilized (26) [35]. In the case of the proposed LNTA, the power gain was obtained by performing a small signal simulation of the LNTA at the tuned output frequency 2.14 GHz with a differential output load of 200 Ω. In the case of the LNTA of [5], the power gain was obtained by multiplying the full-circuit g_m^2 by $\mathrm{R}_L = 200\,\Omega$ and $\mathrm{R}_S = 100\,\Omega$, which neglects any power loss at the output. It can be seen that the FOM of the proposed LNTA exceeds even those of [16] and [35], which require precise bias point tuning in order to achieve high IIP3 values:

$$\mathrm{FOM_{LNA}} = \frac{\mathrm{IIP3(mW)} \cdot \mathrm{Power\ \ Gain}}{\mathrm{P_{DC}(mW)}\left(10^{\mathrm{NF(dB)}/10} - 1\right)}. \tag{26}$$

The LNTA presented in this paper was incorporated into a radio receiver previously described in [18]. As in other passive mixer-based receivers, the odd-order nonlinearity performance of the receiver with respect to out-of-band blockers is dominated by the LNTA. In this case, measurements made on the receiver can be used to qualitatively corroborate the simulation results presented in Section VI-C. The characteristic behavior predicted by simulations of the proposed LNTA is seen clearly in Fig. 27, where the input-referred IMD power remains roughly constant as the large blocker power is increased from +0 to +12.4 dBm.

[1]If NF were equal to 3 dB, $\mathrm{FOM} = 445$

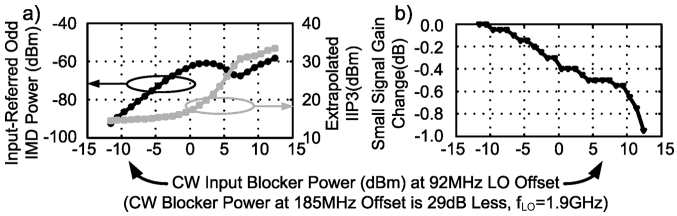

Fig. 27. Receiver two-CW tone IIP3 measurements: (a) input-referred odd IMD, extrapolated IIP3, and (b) out-of-band small-signal gain desensitization.

Furthermore, the large-signal extrapolated IIP3 of +33.5 dBm at a +12.4 dBm large blocker input power agrees well with the +33.0 dBm value obtained in simulation. The receiver small-signal gain drops by slightly less than 1 dB for a +12.4 dBm CW blocker input, resulting in a desensitization point a bit lower than but consistent with the foregoing simulation results with the passive mixers in place.

XI. Conclusion

This paper has described a novel wide-swing PMOS/NMOS LNTA that presents a roughly constant 50-Ω input impedance to the antenna over a rail-to-rail differential input swing. When ideally loaded, the LNTA was shown to have a simulated large-signal extrapolated IIP3 of +32.8 dBm and an out-of-band 1-dB desensitization point of +22 dBm, the latter of which is dictated by the input device parasitic source diodes. Robustness of the large-signal linear I-V characteristic was demonstrated in simulation over PVT corner simulations. Finally, a functional basis set was proposed to model the LNTA in a mathematically concise fashion. It is expected that the use of such an LNTA in conjunction with a passive mixer-based downconverter will enable the widespread implementation and adoption of large-signal handling CMOS RF receivers.

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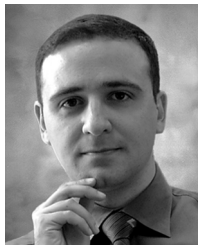

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