

## 22.2 An Octave-Range Watt-Level Fully Integrated CMOS Switching Power Mixer Array for Linearization and Back-Off Efficiency Improvement

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Non-constant envelope modulation schemes have become commonplace in cellular applications due to their higher spectral efficiency. Linear PAs driven by an RF transmitter are usually used to generate these signals faithfully at the expense of power efficiency. Separate processing of amplitude and phase information (e.g., EER or polar modulation) has been proposed [1] as a way of improving the system power efficiency. However, many of these schemes require an efficient high-power low-frequency supply modulator to reconstruct the amplitude information. This can be done, for instance, using a switching DC-to-DC converter with its own limitations in efficiency, bandwidth, and area that also requires an external inductor [2]. Even for an ideal supply modulator, the amplitude dynamic range of the PA itself is limited by the gate-to-drain feedthrough and its associated AM-to-AM and AM-to-PM conversion. (For example, in [3] a 10dB change in the supply results in a 5° phase shift at the output.) Although a digitally-modulated polar PA [4] has been shown as a possible solution at lower power levels, its implementation in a wideband watt-level fully-integrated CMOS PA for non-constant modulation has not yet been demonstrated.

The power mixer array, shown in Fig. 22.2.1, overcomes these problems by selectively applying the LO signal to a sufficient number of individually-linearized power mixers, (Fig. 22.2.2), to generate the necessary output power while maintaining linearity and high back-off efficiency. A current-commuting mixer has a high power efficiency, since the lower-tree common-source transistors ( $M_1$  and  $M_2$ ), driven by the LO, switch between triode and cut-off modes [5]. The power mixer utilizes a double cascode with thick-gate-oxide top transistors ( $M_7$  and  $M_8$ ) [6] to increase the maximum drain voltage swings without long-term stress-induced degradation. The baseband (BB) signals are applied to the middle-tree differential pairs ( $M_3$ ,  $M_4$ ,  $M_5$ , and  $M_6$ ), rendering a separate supply modulator unnecessary. As a result, the proposed system can have small die area, high efficiency, and large signal bandwidth. It should be noted that the power mixer array subsumes some of the blocks typically implemented on the transceiver chip (e.g. upconversion mixers).

In this implementation, the output currents of sixteen power mixer cores are combined at their drains, where the non-constant envelope RF signal is regenerated (Fig. 22.2.1). The resultant non-constant envelope current is impedance transformed to drive the external 50Ω load using an on-chip tuned transformer that maintains the linearity of the current-domain signal. The phase-modulated LO signal is buffered and selectively applied to the desired number of power mixer cores by the digital LO distributor. The choice of how many and which power mixers receive the digital LO is controlled by an on-chip digital controller. The differential BB envelope signal is linearized by analog BB replica linearizers (Fig. 22.2.2) and then applied to the power mixer cores via an analog BB distributor. The analog BB distributor can connect each unit power mixer core to any of the differentially linearized BB (LBB) signals while it feeds back the mixer's common-mode (CM) information to the analog replica linearizers.

A replica differential pair is used to model the nonlinearity of the voltage-to-current conversion of the power mixer core (Fig. 22.2.2). The BB replica amplifier is placed inside a resistive feedback loop with another amplifier. The feedback linearizes the transfer function from the  $BB_{in}$  inputs to the  $BB_{out}$  outputs and in the process generates a differential signal LBB at the input of the replica, which produces an output signal linearly related to the  $BB_{in}$  signal. This LBB differential signal is then applied to the gates of the middle-tree power-mixer cores ( $M_3$ ,  $M_4$ ,  $M_5$ , and  $M_6$ ), as shown in Fig. 22.2.2. To accurately compensate the nonlinearity of the power-mixer core, we need to account for the switching nature of the common-source transistors ( $M_1$  and  $M_2$ ) driven by the LO. In the switching mode, the drain RF current of these transistors,  $I_{RF}$ , is proportional to the source DC voltages of  $M_3$  and  $M_4$  (node X) to the first order. An additional common-mode (CM) feedback mechanism is used to dynamically match the voltage of node X to its replica equivalent voltage Y (sources of  $M_{10}$  and  $M_{11}$ ) to maintain linearity. We refer to this mode of operation as the Linearized Analog (LA) mode.

Alternatively, linearization can also be achieved using the Linearized Segmented (LS) mode shown in Fig. 22.2.3. In the LS-mode the BB input of all but one ( $n-1$ ) of the power mixer cores can be either at zero or at maximum levels to represent an  $n$ -level thermometer code. The transition between these discrete BB

levels can be pulse-shaped appropriately to minimize the in- and out-of-band aliasing and spurious generation. The remaining power mixer core ( $PM_n$ ) can be used to capture the analog residue, if necessary. Note that in the LS-mode, to avoid linearity degradation due to output impedance variations (both resistive and capacitive parts), the LO signal is applied to all of the power mixer cores. This maintains similar output impedances for different power levels.

In the case of a non-constant envelope modulation, the number of power mixer cores that receive the LO signal for a given symbol can be dynamically adjusted to improve the overall efficiency for the symbols that do not need the full power and thus improve the efficiency. We refer to this dynamic activation of different power mixer cores as the Efficient Segmented (ES) mode. This mode of operation can also be used on slower time scales to improve the back-off efficiency.

A prototype was fabricated in a standard 0.13μm CMOS process. Figure 22.2.4 shows the measured maximum output power and PAE of the power mixer array. The PAE is greater than 40% between 1.6 and 2GHz with a peak of 43% at 1.6GHz, and the output power is greater than 1W over an octave from 1.2 to 2.4GHz. This wideband impedance transformation can be attributed to the high coupling coefficient ( $k=0.8$ ) of the on-chip transformer. The power mixer has an LO-to-RF power gain of +28.4dB. It produces the maximum output power of +31.3dBm with a BB input voltage swing of 450mV.

Figure 22.2.5 shows the measured PAE and conversion gain vs. the output power at 1.8GHz for four different modes of operation. The performances have been measured for all four different operation modes, and the Baseline-Analog (BA) mode, which bypasses the analog BB replica linearizer to directly apply to BB signal to all the mixers, is included. With none of the linearization modes active, the output 1dB compression point ( $OP_{1dB}$ ) in the BA-mode power mixer is +28.2dBm. In the Linearized Analog (LA) mode the  $OP_{1dB}$  is simply +31.3dBm since the gain compression is less than 0.4dB even for the maximum output power of +31.3dBm. The LA mode is the most linear for large output powers. The Linearized Segmented (LS) mode exhibits a gain variation of less than 0.9dB for output power levels greater than +20dBm. The Efficient Segmented (ES) mode is most efficient for the reduced output power levels, where it clearly demonstrates an improved efficiency.

To demonstrate the validity of the power mixer array for linearization and back-off efficiency improvement, the spectrum and constellation of a 16-QAM modulated signal with 4MSym/s and 100kSym/s at 1.8GHz are measured in the ES and LA modes, respectively, as shown in Fig. 22.2.6. In the ES-mode, cores are activated in units of 4, and the measured PAE is dramatically improved to 19% with an average output power of +26.0dBm and an EVM of 4.9% despite the 16-QAM non-constant envelope with a peak-to-average power ratio of 6.7dB. In the LA-mode, an EVM of 3.8% is measured with an average output power of +27.3dBm and an overall PAE of 16%. The EVM of a  $\pi/4$ -DQPSK signal is also measured for the LA and ES modes. In the LA-mode, an average output power of +29.0dBm is achieved with an EVM of 3.4% and a PAE of 25%. In the ES-mode, a PAE of 25% is maintained with an EVM of 4.1% even at a smaller average output power of +28.0dBm. All the reported efficiency numbers include the power consumption of all on-chip elements, such as the power mixers and distributors. Hence, they compare even more favorably with a linear PA implementation where additional power is consumed in the transmitter to perform these functions. Figure 22.2.7 shows the die micrograph of the prototype. The entire chip occupies an area of 1.6x1.6mm<sup>2</sup>.

### Acknowledgement:

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### Reference:

- [1] L. Kahn, "Single-Sided Transmission by Envelope Elimination and Restoration," *Proc. Institute of Radio Engineers*, pp. 803-806, July 1952.
- [2] D. Su and W. McFarland, "An IC for Linearizing RF Power Amplifiers Using Envelope Elimination and Restoration", *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252-2258, Dec. 1998.
- [3] S. Hietakangas, T. Rautio, T. Rahkonen, "Feedthrough Cancellation in a Class-E Amplified Polar Transmitter", *European Conference on Circuit Theory and Design*, pp. 591- 594, Aug. 2007.
- [4] A. Kavousian, D. Su and B. Wooley, "A Digitally Modulated Polar CMOS PA with 20MHz Signal BW", *ISSCC Dig. Tech. Papers*, pp. 78-79, Feb. 2007.
- [5] E. Klumperink, S. Louwmsma, G. Wienk, and B. Nauta, "A CMOS Switched-Transconductor Mixer", *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1231-1240, Aug. 2004.
- [6] T. Kuo, and B. Lusignan, "A 1.5W Class-F RF Power Amplifier in 0.2μm CMOS Technology", *ISSCC Dig. Tech. Papers*, pp. 154-155, Feb. 2001.

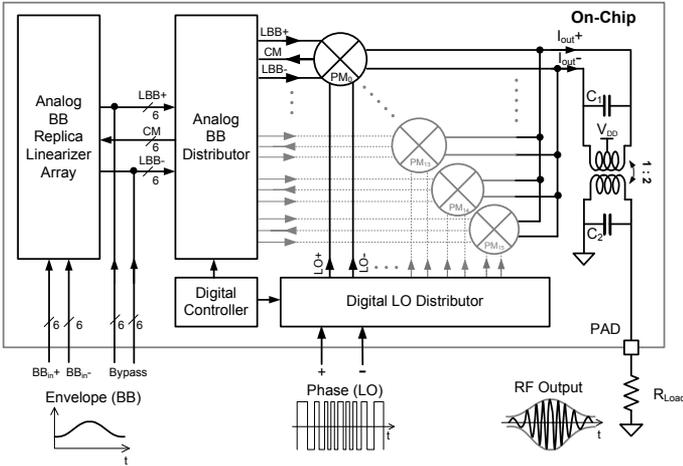


Figure 22.2.1: Block diagram of proposed power mixer array system.

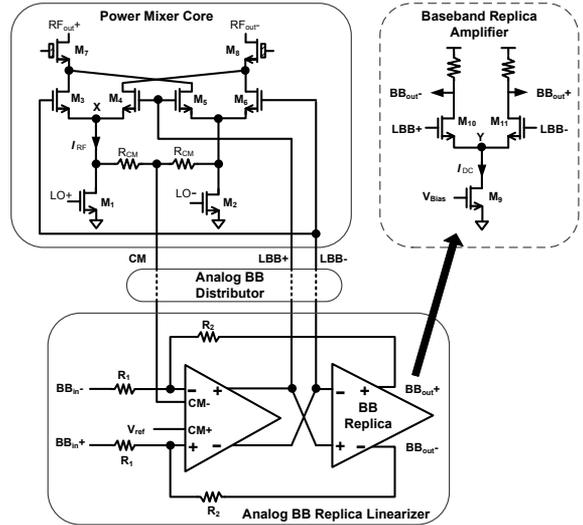


Figure 22.2.2: The schematic of the power mixer core and Analog BB replica linearizer.

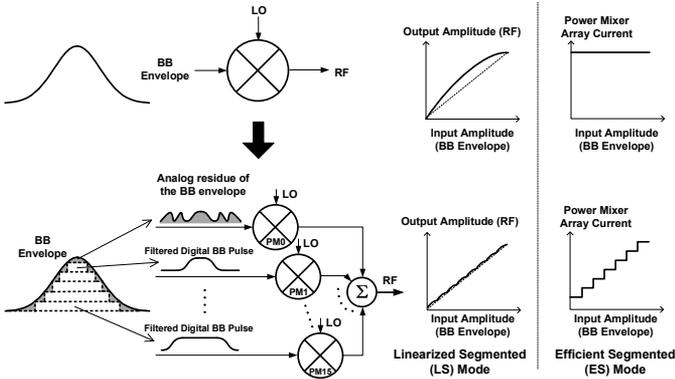


Figure 22.2.3: The Linearized Segmented (LS) mode and Efficient Segmented (ES) mode.

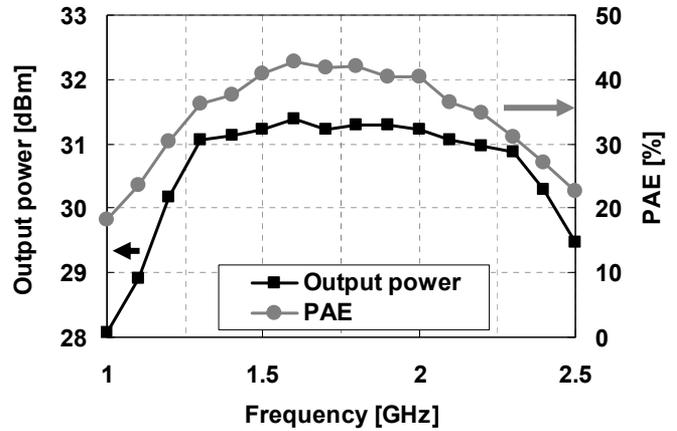


Figure 22.2.4: The measured frequency dependence of maximum output power and peak PAE.

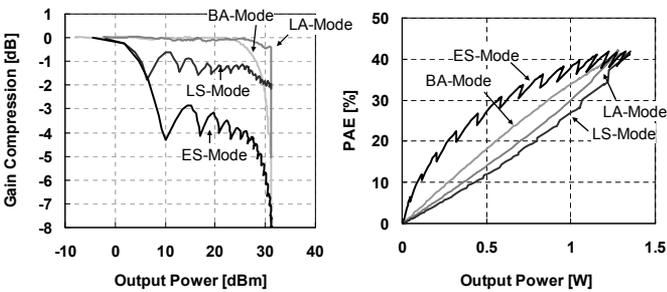


Figure 22.2.5: The measured output power vs. conversion gain and PAE.

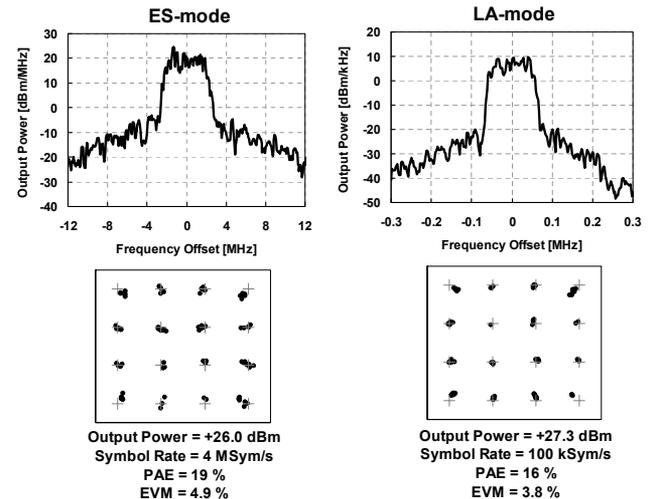


Figure 22.2.6: The measured spectrum and constellation of 16-QAM in the Efficient Segmented (ES) and Linearized Analog (LA) modes.

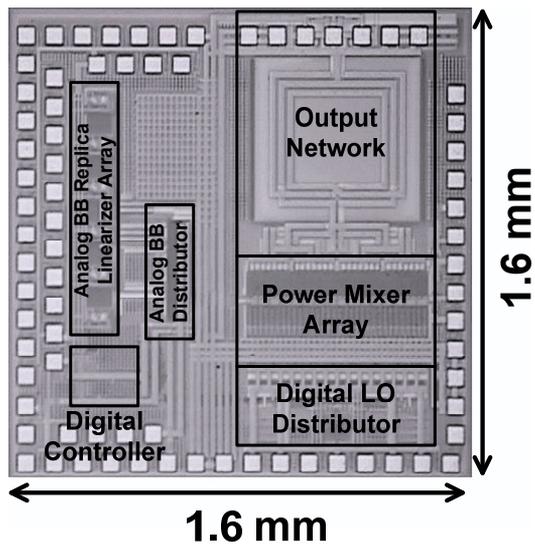


Figure 22.2.7: Die micrograph.