

# Multi-Pole Bandwidth Enhancement Technique for Transimpedance Amplifiers

Behnam Analui and Ali Hajimiri

California Institute of Technology, Pasadena, CA 91125 USA

Email: behnam@caltech.edu

## Abstract

A new technique for bandwidth enhancement of amplifiers is developed. Adding several passive networks, which can be designed independently, enables the control of transfer function and frequency response behavior. Parasitic capacitances of cascaded gain stages are isolated from each other and absorbed into passive networks. A simplified design procedure, using well-known filter component values is introduced. To demonstrate the feasibility of the method, a CMOS transimpedance amplifier is implemented in 0.18 $\mu\text{m}$  BiCMOS technology. It achieves 9.2GHz bandwidth in the presence of 0.5pF photo diode capacitance and a trans-resistance gain of 0.6k $\Omega$ , while drawing 55mA from a 2.5V supply.

## 1. Introduction

The ever-growing demand for higher information transfer rates has resulted in a rapid emergence of highly integrated communication systems. Silicon integrated circuits are the only candidate that can achieve the required level of integration with reasonable speed, cost, and yield and have thus been pursued to a great degree in recent years. In particular, full silicon-based integration of optical-fiber-based data communication systems, such as 10-GB/s (OC192) and 40-GB/s (OC768) SONET or gigabit ethernet systems, can be of great interest for these reasons. However, silicon-based integrated circuits implementing such systems face serious challenges due to the inferior parasitic characteristics in silicon-based technologies, complicating the procedure for a wide-band design.

Wide-band amplifiers are one of the most critical building blocks at the electro-optical interface on both receiver and transmitter sides. Wideband operation is an inseparable part of any baseband communication system such as non-return-to-zero (NRZ) amplitude shift keying (ASK) common to optical fiber communications due to the signal's spectral content down to very low frequencies. Particularly, all amplifiers in the path should have enough bandwidth with minimum variations in the passband and constant group-delay to avoid distortion in the signal.

The inherent parasitic capacitors of the transistors are the main cause of bandwidth limitation in wideband amplifiers. Several bandwidth enhancement methods have been proposed in the past. First order shunt peaking is used to introduce a resonant peaking at the output when the amplitude starts to roll-off at high frequencies [1][2]. Traditionally it has been done by adding a series inductor with the output load that increases the effective load impedance as the capacitive reactance drops at higher fre-

quencies. Capacitive peaking [3] is a variation of the same idea that can improve the bandwidth.

A more exotic approach to solving the problem was proposed by Ginzton *et al* using distributed amplification [4]. Here, the gain stages are separated with transmission lines. Although the gain contributions of the several stages are added together, the parasitic capacitors can be absorbed into the transmission lines contributing to its real part of the characteristic impedance. Ideally, the number of stages can be increased indefinitely, achieving an unlimited gain bandwidth product. In practice, this will be limited to the loss of the transmission line. Hence, the design of distributed amplifiers requires careful electromagnetic simulations and very accurate modeling of transistor parasitics. Recently, a CMOS distributed amplifier was presented [7] with *unity-gain* bandwidth of 5.5 GHz.

This work introduces a new multi-pole bandwidth enhancement technique for wide-band amplifier design. It is based on turning the entire amplifier into a low-pass filter with a well-defined pass-band characteristic and cut-off frequency. The inevitable parasitic capacitances of the transistors are absorbed as part of the low-pass filter and hence, affect the bandwidth of the amplifier in a controlled fashion.

In the rest of the paper, we first discuss the details of the bandwidth enhancement technique starting with a brief background and following with the design methodology. Then, we show implementation of CMOS transimpedance amplifier as a design example and conclude this paper with its measurement results.

## 2. Bandwidth Enhancement Theory

The limitation on the gain bandwidth product (GBW) of conventional amplifier structures has been known for over half a century [9]. It was first studied in the context of broadband matching, where lossless passive networks are used to optimally match specific loads to source impedances over a wide range of frequencies. Bode has shown that there exists a maximum GBW product for such a system regardless of the network used [8]. Fano and Youla, further generalized the theory for a larger class of load impedances. The same theory can be applied to a simple single-stage amplifier, with the unilateral small signal model and a passive load impedance  $Z(j\omega)$  shown in Fig. 1a. For such an amplifier, it can be shown that [5] the maximum gain bandwidth product is given by:

$$(GBW)_{max} = \frac{g_m}{\pi \cdot C} \quad (1)$$

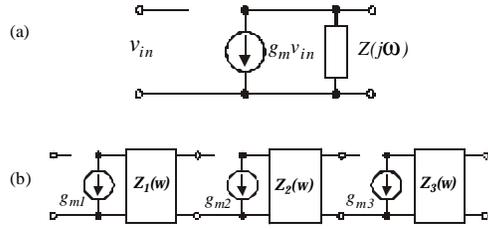


Fig. 1 (a) A general small signal model of an amplifier with an arbitrary passive load (b) isolation of cascaded passive networks

where  $g_m$  is the device transconductance and  $C$  is defined as:

$$C = \lim_{\omega \rightarrow \infty} \left( \frac{1}{j\omega Z} \right) \quad (2)$$

However, the upper-bound in (1) is not valid for amplifiers, where the load does not satisfy the conditions of an impedance function<sup>1</sup>. In other words, if the overall transfer function of an amplifier is of the form:

$$A_v(j\omega) = g_m \cdot Z(j\omega) \quad (3)$$

and  $Z(j\omega)$  is not an impedance function, then Bode-Fano limit in (1) need not be satisfied. It will be shown that distributing passive structures between gain stages can result in such transfer function. Therefore, the GBW product can potentially be higher. This is one of the major contributions of this paper.

A more rigorous study on broadband matching circuits for amplifiers is developed in [10]. There, the matching networks exist at the input and output of a single stage amplifier simultaneously. Although, this can result in larger GBW products than (1), the need for the amplifier two-port parameters complicates the proposed design method. Moreover, the procedure emphasizes single stage, two-port amplifiers, which limits its applications. Based on these methods, passive structures have been used for input broadband matching and bandwidth enhancement [12].

## A. Methodology

Practical amplifiers are more complicated than the model in Fig. 1a. They have several stages with more nodes controlling the transfer function shape. The new technique introduced in this paper, proposes deploying distributed passive networks in between the gain stages of the amplifier to tailor the frequency response shape. The distribution of the passive networks will result in a frequency dependent transfer function which need not be in form of an impedance function as in (3). *Therefore, the Bode-Fano limit does not apply to the complete amplifier and can be overcome in practice.*

Fig. 1b shows small signal model of cascaded transistor gain stages and passive networks using unilateral approx-

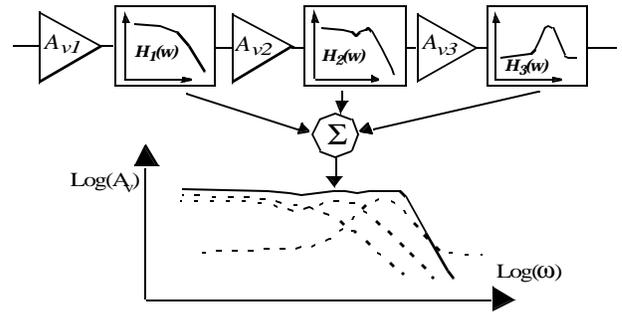


Fig. 2 Stagger tuning for designing wideband amplifiers

imation for the transistors. If some number of stages with the same simple model of Fig. 1a are placed in series, gain stages separate different networks due to the internal isolation of the active devices. Using parameters in Fig. 1b, the over all transfer function can be written as:

$$A_v(j\omega) = G_m \cdot Z_{21}(j\omega) \quad (4)$$

where:

$$G_m = g_{m1} \cdot g_{m2} \cdot g_{m3} \quad (5)$$

$$Z_{21}(j\omega) = Z_{21,1}(j\omega) \cdot Z_{21,2}(j\omega) \cdot Z_{21,3}(j\omega) \quad (6)$$

and  $Z_{21,i}(j\omega)$ 's are the forward impedance parameters of the two-port networks and can be designed independently. From (4) and (6) it is clear that  $Z_{21}(j\omega)$  is the product of three different impedance functions and therefore need not be an impedance function itself. For instance,  $Z_{21}(j\omega)$  is still a rational function, but the numerator polynomial can be more than one degree higher than the denominator one. As a result, although (4) is in form of the overall gain in (3), *it is not limited by the upper-bound set in (1).*

One design approach for such cascaded transfer functions is stagger tuning of the frequency responses, such as the one shown symbolically in Fig. 2. An early amplitude roll-off due to a low frequency pole in one structure can, then, be compensated for, with a peaking in the next stage. Similarly, the overall phase response of passive structures can be properly controlled. However, this requires careful calculation of *exact* transfer functions based on the component values that can be used as design equations. If not accurate, undesirable peaking may be introduced to the overall transfer function.

In the design of such networks, well-known *low-pass filter* structures with known response characteristics can be used instead. Since, in this procedure, it is desired to achieve a particular response shape, which resembles low-pass filter responses with known characteristics, the same component values as the ones in the filter can be used for the passive network elements. Therefore, the design procedure will be much more simplified. Additionally, absorbing the capacitive parasitic components of the gain stages (transistors) into the passive networks will turn the transistor into a gain stage with infinite bandwidth. Thus, the frequency-dependent behavior will completely rely on the passive structures. In his approach one can resort to passive networks with low sensitivity to component values. The design procedure based on this new practical technique will follow.

1. An impedance function in the complex frequency domain, is a rational function (ratio of two polynomials with real coefficients) of frequency with no singularities in the interior of the right half-plane. Additionally, the numerator polynomial should be of at most one degree higher than the denominator one. The conditions for impedance function can be found in [5].

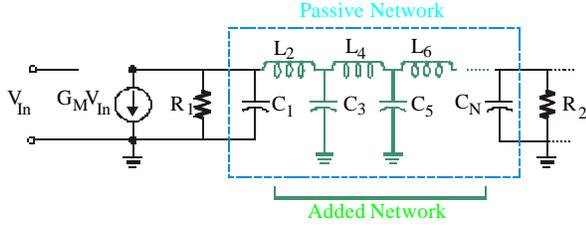


Fig. 3 Inserting a ladder structure between the gain stages

## B. Design Procedure

Different passive structures can be inserted between gain stages. However, using a standard network configuration for which the component value equations are already known, will simplify the design. A small-signal model of two cascaded gain stages is shown in Fig. 3 after adding a standard ladder configuration. By choosing the desired frequency response shape and hence the filter type, the element values can be generated using standard network synthesis methods [11]. The order of the passive network,  $n$ , is an additional design parameter. Using higher orders will improve the response; however, the components will take some impractical values and the number of inductors will also increase resulting in an unrealistic design. As an example, to achieve a maximally flat frequency response for a 3rd order ladder network, such as the one in Fig. 3, values from butterworth filter components can be used as follows:

$$C_1 = \frac{1}{R_1(1-\delta)\omega_c} \quad (7)$$

$$L_2 = \frac{2}{(1-\delta+\delta^2) \cdot \omega_c^2 \cdot C_1} \quad (8)$$

$$C_3 = \frac{1}{R_2(1+\delta)\omega_c} \quad (9)$$

where  $\delta$  is an indication of impedance transformation between  $R_1$  and  $R_2$  and is defined as:

$$\delta = \sqrt[n]{\frac{R_1 - R_2}{R_1 + R_2}} \quad (10)$$

and  $\omega_c$  is the 3-dB cut-off frequency of the network. Note that  $C_1$  and  $C_3$  are the transistor parasitic capacitances absorbed into the passive structure. The design procedure is to first optimize the original amplifier with no additional components. As a result, component values for  $R_1$ ,  $R_2$ ,  $C_1$ , and  $C_3$  will be known. Using either of (7) or (9), the new value for  $\omega_c$  can be derived. Then, the value of the inductor can be calculated from (8), knowing all the other parameters. If the analysis is done for the output structure,  $R_2$  should be replaced with  $R_L$  which is the load resistance.

If we define the bandwidth enhancement ratio ( $BWER$ ) as the ratio between the old (before adding any passive component) and new 3-dB bandwidth of the amplifier, we can show:

$$BWER \equiv \frac{\omega_{c, new}}{\omega_{c, old}} = \frac{1}{1-\delta} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{C_1 + C_3}{C_1} \quad (11)$$

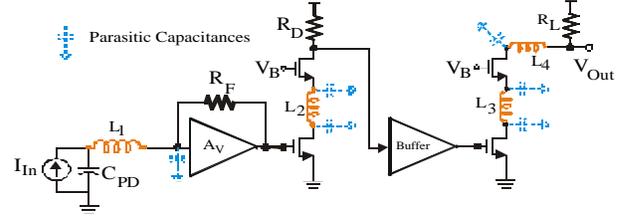


Fig. 4 Simplified schematic of the TIA with parasitic capacitances and additional inductors.

This expression can be used as a guideline in designing the amplifier, before adding the passive network. For instance, adjusting for larger  $\delta$  with proper choice of load resistors will result in a better bandwidth enhancement ratio after inserting the network.

If the analysis is to be carried out for the input stage of a transimpedance amplifier with a current input signal,  $R_1$  is infinity due to the large equivalent resistance of the reverse biased photo diode. However, it can be shown from (11) that for fixed  $C_1$ ,  $C_2$ , and  $R_2$ , there exists a value  $R_1$  (i.e.,  $R_1 = 2.05R_2$  resulting in  $\delta = 0.7$ ) that maximizes the  $BWER$  for the input stage. Therefore, the same procedure can be used, without including  $R_1$  in the network. Enhancement ratio in (11) should also be modified for the input passive structure as:

$$BWER = \frac{1}{1-\delta} \cdot \frac{R_2}{R_1} \cdot \frac{C_1 + C_3}{C_1} \quad (12)$$

## 3. Design example and simulation results

To demonstrate the effectiveness of the developed methodology, a CMOS transimpedance amplifier (TIA) is designed. The simplified schematic of the circuit including the added passive components is shown in Fig. 4. It is a single-ended design consisting of three gain stages. The first stage is a shunt-shunt feedback transimpedance stage that provides a low input impedance. This will reduce the dominant effect of the input pole due to the large photo diode junction capacitance ( $C_{PD}$ ). The next two stages are cascode configuration and are isolated using a source follower buffer.

Four passive networks are inserted in the critical nodes of the structure to relocate the poles and therefore, enhance the bandwidth. The input network, separates the photo diode capacitance and the parasitic capacitance of the input stage. Adding one inductor will turn it into a 3rd order ladder structure, which can be designed as explained in the previous section. The next two networks are also of 3rd order and are placed between the cascoded transistors. The output network isolates the load resistance from the last stage and is a 2nd order network. However, adding explicit capacitors (including bonding-pad capacitance) can turn it into a 3rd order structure.

With this choice of networks, only inductors are to be added to the configuration. The capacitors (as shown with dotted line in Fig. 4) are the parasitics from the devices. A final optimization is done to include the bilateral effects. Note that the output network is different from a conventional shunt-peaking approach. For a photo diode capacitance of 0.5pF, circuit achieves over 9GHz

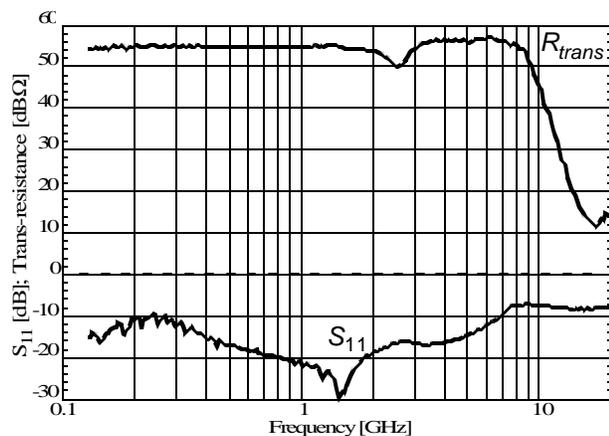


Fig. 5 Trans-resistance gain of the TIA with 0.5pF photo diode capacitance

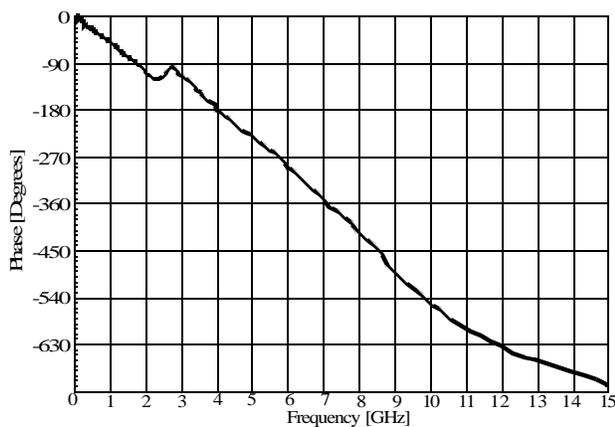


Fig. 6 Phase response of the TIA

bandwidth. This is 2.4 times larger than the bandwidth achieved using same circuit with no additional passives.

#### 4. Measurement results

The transimpedance amplifier was implemented using 0.18 $\mu\text{m}$  MOS transistors in a BiCMOS process technology. It draws 55mA from a 2.5V power supply. The amplitude and phase response of the implemented TIA, extracted from measurement data are shown in Fig. 5 and Fig. 6. Here the photo-detector capacitance is  $C_{PD}=0.5\text{pF}$ . The bandwidth is 9.2GHz and the transimpedance gain is 54dB $\Omega$ . This is the fastest 0.18 $\mu\text{m}$  CMOS transimpedance amplifier to this date to the authors' knowledge. The input reflection coefficient,  $S_{11}$ , remains below -10dB up to 7GHz. The dip in the frequency response of the transimpedance can be traced back to a resonance mode between the on-chip supply by-pass capacitor and wirebond and supply line inductance as changing those parameters directly affects its depth and frequency. Simulated average equivalent input noise current is  $17\text{pA}/\sqrt{\text{Hz}}$ . This results in total input noise current of 1.6 $\mu\text{A}$ . The amplifier core occupies  $0.8 \times 0.8\text{mm}^2$  of area as shown in Fig. 7.

#### 5. Conclusions

In this paper, we address the gain-bandwidth (GBW) limitation problem and introduce a new practical methodology that can be used to design wide-band amplifiers with specified desired characteristics for its transfer function. In a simple design procedure, parasitic capacitances of

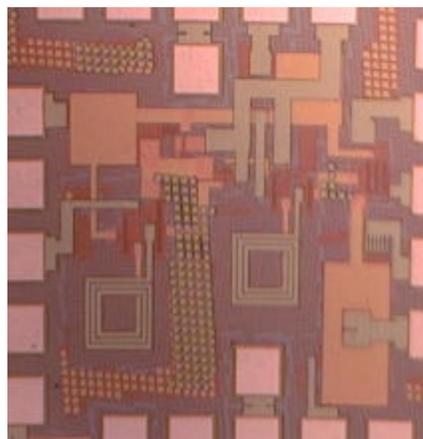


Fig. 7 The die photo of the 10GHz Trans-impedance Amplifier

transistors can be absorbed into passive networks, inserted between the gain stages. The component values can be calculated based on standard low-pass filter structures. A prototype CMOS TIA implemented using the developed technique achieves over 9GHz bandwidth and 54dB $\Omega$  transimpedance gain from a 0.5pF photo-diode capacitance.

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