A 24GHz CMOS Front-end

Xiang Guan and Ali Hajimiri
Department of Electrical Engineering
California Institute of Technology
[xiangg,hajimiri]@caltech.edu

Abstract

This paper reports the first 24GHz 0.18-μm CMOS front-end. It down-converts an RF input at 24GHz range to an IF of 5GHz range with a power gain of 27.5dB and an overall noise figure of 7.7dB. It achieves an input return loss, S_{11} of -21dB drawing 43mA from a 1.5V supply. The LNA achieves a voltage gain of 22dB and a noise figure of 6dB consuming 16mA of dc current. This performance is achieved through an analysis of the LNA showing that the NF and gain of the common-gate stage scale more gracefully with frequency and hence it is the topology of choice for very high frequency front-ends.

1. Introduction

The rapid evolution of the wireless communication world has resulted in a tremendous amount of research on building high-performance RF circuits in various technologies. Among many contenders, CMOS is particularly attractive for its low cost and high level of integration. Meanwhile, the growing demands for larger bandwidth motivate integrated circuits to move toward higher frequencies. Recent works have shown that CMOS is a promising medium for implementing RF circuits for applications in the low-GHz range. However, the performance, or even the possibility of CMOS tranceivers for applications over 20GHz is rarely investigated. The purpose of this work is to develop a CMOS receiver front-end operating at frequencies above 20GHz such as 24-24.25GHz industrial, scientific and medical (ISM) band.

While the lower frequency bands (*e.g.*, 2.4 and 5GHz bands) are being extensively explored for various applications, there are several potentially significant advantages to operation at much higher frequency. One obvious advantage is the larger available bandwidth at high frequencies that is extremely important for wideband wireless communications. Silicon-based technologies, particularly CMOS are good candidates for highly-integrated solutions at such frequencies.

A simplified block-diagram of a 24GHz receiver is shown in Fig. 1. In this architecture, the first amplification and down-conversion stages are the most critical to the system performance and the most difficult to implement in CMOS technology. In this example, a high-frequency 1st IF of 5GHz is chosen to improve image rejection. In the following section, the trade-offs involved in the implementation of an ultra-high frequency CMOS front-end are analyzed.

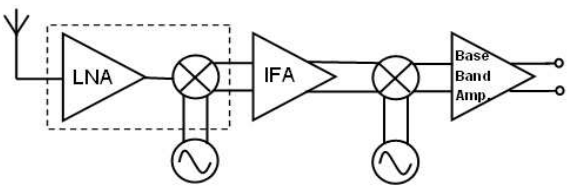

Figure 1. Block diagram of a 24GHz receiver

2. Input Stage Analysis

The input stage of the LNA sets the limit on the sensitivity of the receiver. The input stage should achieve high gain and low noise while providing a well-defined real input impedance. Therefore, a careful analysis and comparison of various gain stages must be carried out to choose the right topology for this crucial cell.

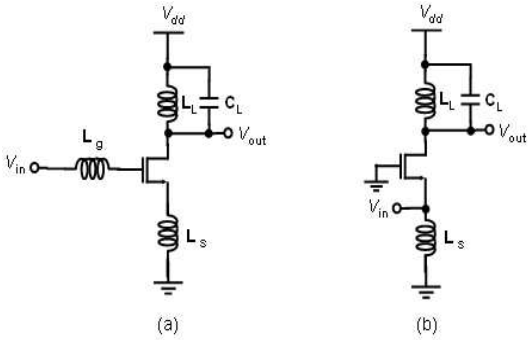

Figure 2. Input Stage (a)common-source with inductive degeneration. (b)common-gate.

The common-source stage with inductive degeneration of Fig. 2 (a) has been commonly used in CMOS LNA implementations. In this common-source topology, the source degeneration inductor introduces a real part into the input impedance seen looking into the gate. This impedance is used to match the amplifier to the source impedance, R_S. The real part of the input impedance, R_{in} is given by:

$$R_{in} = \frac{g_m}{C_{gs}} L_s \tag{1}$$

where g_m is transistor's transconductance, C_{gs} is the gate-source capacitor, and L_s is the source inductor. For an input power match R_{in} must be equal to R_S. The reactive part can be compensated at the frequency of operation, ω_0, by selecting the gate and drain inductors, L_g and L_s such that:

$$\omega_0 = \sqrt{\frac{1}{(L_s + L_g)C_{gs}}} \tag{2}$$

When the input impedance is matched to R_s, the effective transconductance of the stage is related to the transistor's cut-off frequency, ω_T, through: [1]

$$G_m = \frac{1}{2R_s} \frac{\omega_T}{\omega_0} \tag{3}$$

The minimum achievable noise figure can also be estimated by applying constant-power optimization method [1], resulting in:

$$F_{min} \approx 1 + 1.426\sqrt{\delta\gamma}(\frac{\omega_0}{\omega_T}) \tag{4}$$

where γ and δ are the channel thermal noise and gate noise coefficients.

Equations (3) and (4) indicate that common-source LNA is well suited for applications where the working frequency is well below ω_T. However, the performance of common-source LNA degrades substancially when ω_0 becomes comparable to ω_T, since F and G_m are linearly related to ω_0 and $1/\omega_0$ respectively,

In contrast, in common-gate LNA, the gate-source and gate-drain parasitic capacitances of the MOSFET can be absorbed into the LC tank and resonated out. Therefore, to the first order, the noise and gain performance of the common-gate stage is independent of the operation frequency.

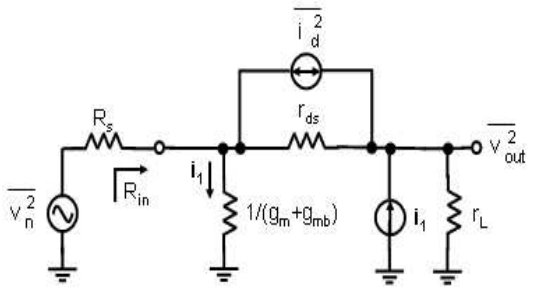

Figure 3. Small-signal model for analyzing the common-gate LNA

It is easy to show that the noise factor of common-gate LNA has a lower bound of $1 + \gamma$ if an infinite transistor output resistance, r_{ds}, is assumed. However, in practice, especially in short-channel MOSFET case, where r_{ds} is small, the effect of a finite r_{ds} has to be taken into account. In common gate topology, r_{ds} forms a positive feedback around the amplifier and increases the input resistance. Applying nodal analysis to the small-signal equivalent circuit shown in Fig. 3, we obtain the following equation:

$$R_{in} = \frac{1}{g_m + g_{mb}} (\frac{r_{ds} + R_L}{r_{ds}}) \tag{5}$$

where R_L is the equivalent shunt resistance introduced by the finite quality factor, Q, of the resonant load. If R_{in} is matched to R_s, neglecting the noise generated by inductor loss and taking the body effect into account, G_m and F of the common-gate stage can be shown to be:

$$G_m = \frac{1}{2R_s} \tag{6}$$

$$F = 1 + (\frac{\gamma}{\alpha})(\frac{1}{1+\chi})(\frac{r_{ds}}{r_{ds} + R_L}) \tag{7}$$

where α is the ratio of the transconductance to zero V_{DS} channel conductance, *i.e.*, g_m/g_{d0}, and χ is the ratio of the backgate transconductance to that of the MOS transistor, *i.e.*, g_{mb}/g_m. If $r_{ds} \to \infty$, $F = 1 + \gamma/(\alpha(1+\chi))$, which is consistent with the classical result. However, if $R_L \to \infty$, $F \to 1$. Therefore, the noise figure of common-gate LNA is not lower bounded by 2.2dB as claimed by many previous publications if the effect of finite r_{ds} is taken into account.

For a given drain current, I_D, Substituting $r_{ds} = 1/(\lambda I_D)$ into this equation results in:

$$F = 1 + (\frac{\gamma}{\alpha})(\frac{1}{1+\chi})(\frac{1}{1 + R_L \lambda I_D}) \tag{8}$$

which indicates theoretically that we can reduce noise figure of a common-gate LNA by dissipating more power without bound. In practice, R_L is limited by Q of the planar inductors and I_D is limited by the dc power budget and the size of the inductor.

The above analysis of common-gate stage doesn't account for transistor gate noise. However, gate noise originates from the capacitive coupling between the channel and the gate. In a common-gate stage, the channel and the gate of the transistor are decoupled at the resonant frequency. Therefore, the gate noise contribution to the common-gate stage output noise power seems to be negligible.

Based on this argument, at frequencies closer to ω_T, the common-gate LNA provides a similar gain as common-source LNA but with a lower noise figure. In addition, the signal feed-through due to the gate-drain capacitor further degrades the gain and the noise figure of common-source LNA at high frequency. The common-gate LNA avoids this problem because the transistor gate is bypassed to ground.

Furthermore, the common-gate stage has a low sensitivity of its input match to parameter variations at high

frequencies. Particularly, if L_s and C_{gs} deviate slightly from their nominal values, $|\Delta S_{11}|$ is given by:

$$|\Delta S_{11}| = \frac{1}{2R_s\omega C_{gs}}(\frac{\Delta L_s}{L_s} + \frac{\Delta C_{gs}}{C_{gs}}) \qquad (9)$$

As can be seen, the sensitivity of the input matching to the capacitor and inductor values is inversely proportional to the operation frequency. For instance, at 24GHz, if both L_s and C_{gs} have $+10\%$ deviation from their nominal values, a -15dB S_{11} can still be achieved assuming a C_{gs} of 0.1pF.

In summary, compared to common-source degenerated topology, common-gate topology provides a smaller achievable noise figure and similar gain at frequency close to ω_T of the transistor. Moreover, the input match of common-gate stage has a low sensitivity to parameter variations at high frequencies. Therefore, common-gate input stage is employed in this work.

3. Circuit Design

3.1. Low Noise Amplifier

Fig. 4 shows the LNA topology. It consists of three stages. The first stage is a common-gate amplifier with a shunt inductor, L_2. The second and the third stage are both common-source degenerated amplifiers which are used to enhance the overall gain. AC coupling is employed between the stages.

The analysis in the previous section ignores all the substrate effects. However, in the 24GHz range, capacitive coupling and resistive loss through the substrate have tremendous influence on the circuit performance. A simplified substrate network model for MOS transistor [2] is shown in Fig. 5. In common-gate stage, the substrate parasitic components form a T-network which is included in the positive feedback path. This feedback harms the input match and noise figure. L_2 is added between the drain and source to resonate the capacitive part and thus reduce the capacitive coupling between drain and source through the substrate.

Inductors L_4 and L_6 are implemented as slab inductors. All the other inductors are spirals.

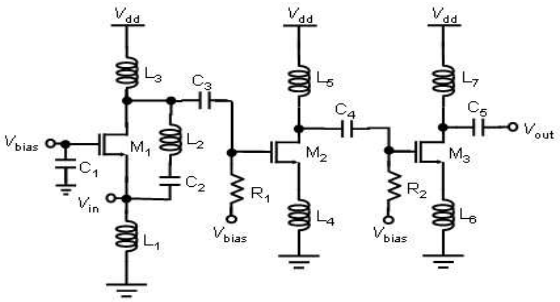

Figure 4. Schematic of LNA

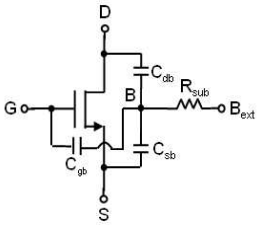

Figure 5. MOSFET substrate network model

3.2. Down Conversion Mixer

The schematic of the mixer is shown in Fig. 6. The core is a single-balanced Gilbert cell. The differential output is provided by two cascode amplifiers. The output-match is realized through the LC network. Again, L_0 is a slab inductor. All the other inductors are spirals.

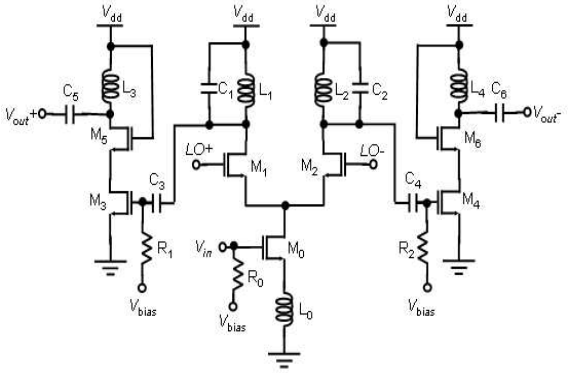

Figure 6. Schematic of Mixer

4. Experimental Results

The circuit has been fabricated using 0.18-μm CMOS transistors and occupies an area of $0.8 \times 0.9mm^2$. The die micrograph is shown in Fig. 7 . The front-end is tested

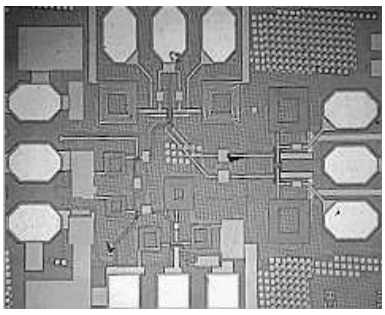

Figure 7. Die Micrograph

by probing the input, outputs, and LO ports. The power and ground pads are wire-bonded to the testing board. The measurement results are summarized in Table 1.

Fig. 8 shows the measured input and output reflection coefficients, S_{11} and S_{22}. The RF input and the IF output are well matched at the respective frequencies.

Table 1. Performance Summary of the front-end

Parameters	Measurement
S_{11}	-21dB
S_{22}	-10dB
Frequency of Maximum Power Gain	21.8GHz
Maximum Power Gain	27.5dB
Maximum Voltage Gain	35.7dB
Maximum Voltage Gain of LNA	22dB
LNA Noise Figure	6.0dB
Overall Noise Figure	7.7dB
LNA Power Consumption	24mW
Total Power Consumption	64.5mW
Supply Voltage	1.5V
Chip Area	$0.8 \times 0.9mm^2$

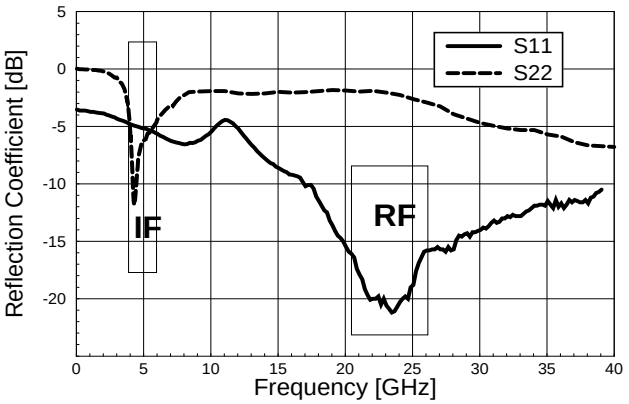

Figure 8. Measured input and output return losses

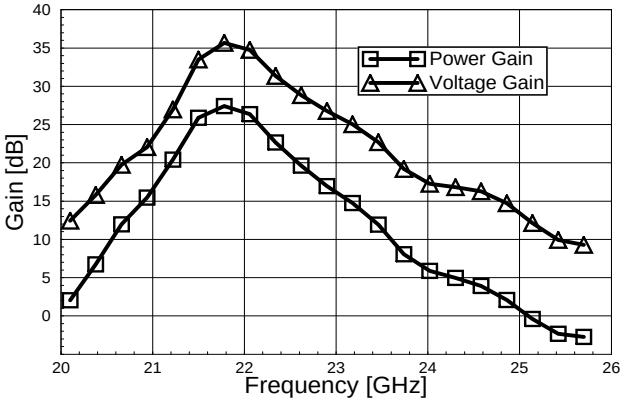

Figure 9. Power gain and voltage gain (LO frequency = 16.9 GHz)

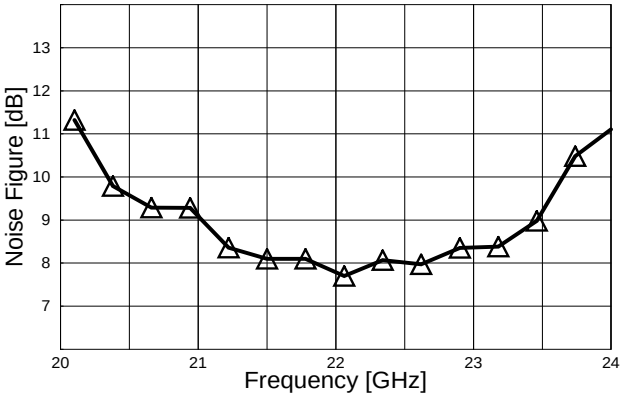

Figure 10. Noise figure (LO frequency = 16.9 GHz)

The measurement shows that the maximum power gain appears for an RF of 21.8GHz and an IF of 4.9GHz. Fig. 9 shows the measured power gain and extracted voltage gain with a 16.9GHz LO frequency. The frequency offset from the 24GHz is likely due to inaccurate modelling of MOS transistor and planar inductor at high frequencies.

The measured noise figure is shown in Fig. 10. A minimum noise figure of 7.7dB is achieved for the combined LNA and mixer at 22.08GHz.

5. Conclusion

The design issues and experimental results of a 24GHz CMOS front-end are presented. This work demonstrates that CMOS technology is a viable candidate for building fully integrated receivers at frequencies higher than 20GHz.

6. Acknowledgements

The authors would like to thank Conexant Systems for fabrication of the front-end in their sbc18 process. They are grateful for the support of Lee Center, NSF-ERC and NSF. They are especially grateful for the help and advice of M. Racanelli, S. Stetson and A. Karroy of Conexant, H. Hashemi, H. Wu, D. Lu, D. Ham, I. Aoki, S. Kee, L. Cheung, B. Analui, and A. Natarajan of Caltech.

7. References

[1] D. K. Shaeffer, and T. H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*, Kluwer Academic Publishers, Boston, 1999.

[2] S. F. Tin, A. A. Osman, K. Mayaram and C. Hu,"A simple subcircuit extension of BSIM3v3 Model for CMOS RF Design" *IEEE J. Solid-State Circuits*,vol.35, pp. 612-624, April 2000