

Electronic Laser Phase Noise Reduction

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Abstract—The first integrated wideband laser phase noise reduction scheme is presented where the laser phase noise is first detected using a photonic chip, processed using an electronic chip, and subtracted from the laser phase in a feed-forward manner. The proof-of-concept experiments on a commercially available 1553nm distributed feedback laser show linewidth reduction from 6MHz to 250kHz equivalent to 14dB phase noise improvement. The hybrid integration of the photonic and electronic chips enables dramatic power consumption and area reduction compared to bench-top designs. This feed-forward scheme performs wideband phase noise reduction independent of the light source and, as such, it is compatible with several types of lasers.

Index Terms—integrated optoelectronics, phase noise, high speed integrated circuits.

I. INTRODUCTION

Phase noise reduction of lasers has important applications in optical communications, ranging, THz signal generation, electro-optical oscillators, and spectroscopy. Although bench-top power-hungry semiconductor laser linewidth reduction schemes using feedback [1] and feed-forward architectures [2] have been demonstrated, a chip-based solution leveraging the integration for power and size reduction has not been demonstrated to this date. In this paper, modern RF techniques and architectures are used to integrate the electronic circuitry of a laser phase noise reduction system on a 65nm CMOS process. Hybrid integration of this electronic chip with our fabricated SOI photonic chip results in significant power and area reduction compared to typical bench-top laser phase noise reduction systems. As indicated in [2] and [3], feedback based laser phase noise reduction schemes typically are not capable of offering large phase noise reduction bandwidth due to the feedback loop stability issue. On the other hand, feed-forward schemes can reduce the phase noise over larger bandwidth.

II. INTEGRATED FEED-FORWARD PHASE NOISE REDUCTION OF LASERS

Figure 1(a) shows the conceptual block diagram of a feed-forward laser phase noise reduction scheme, where the laser phase noise is first measured and then is fed forward to an optical phase modulator (OPM) to reduce the phase fluctuations of the laser. Figure 1(b) shows our proposed realization of the feed-forward phase noise

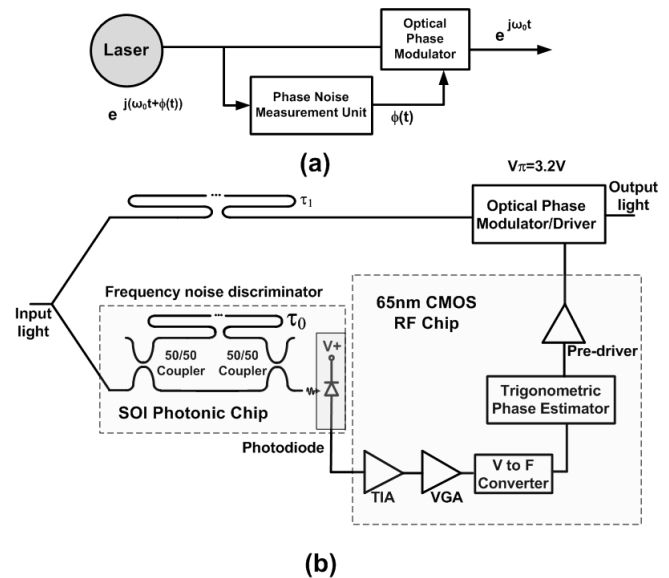


Fig. 1. (a) The conceptual block diagram of a feed-forward laser phase noise reduction, and (b) the block diagram of the proposed phase noise reduction scheme.

reduction scheme. The laser source output is split into two branches. The bottom branch is coupled into the photonic frequency discriminator that uses a grating coupler serving as an optical pad. The photonic frequency discriminator generates an electrical current proportional to the frequency noise of the source [2]. This frequency noise is the derivative of phase noise of the source within the bandwidth of the discriminator (over 1GHz in our design.) The RF chip is wire-bonded to the back-side-coupled photo-diode at the output of the discriminator to receive the small current representing the frequency noise.

To suppress the phase fluctuations of the source, the OPM should be driven by a properly conditioned signal, representing the source phase noise, $\phi(t)$. However, to obtain this proper $\phi(t)$, one must perform an ideal integration and appropriate scaling of the frequency noise signal generated by the frequency discriminator. Despite its conceptual simplicity, this task presents a significant practical challenge due to the unbounded nature of phase noise. This is because $\phi(t)$, essentially being the integral of white

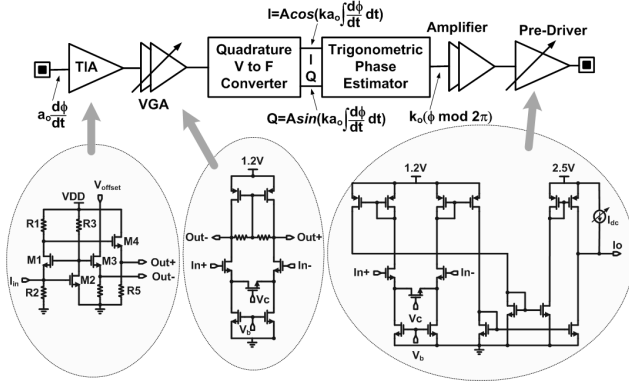


Fig. 2. The block diagram of the proposed architecture implemented in a CMOS RF chip.

noise, closely follows a Brownian motion, whose variance increases linearly with time. Therefore, its corresponding voltage increases indefinitely with time and at some point either saturates the electronic circuitry or damages the off-chip OPM. Hence, an alternative non-saturating integration mechanism followed by a properly scaled phase wrapping process is required.

A. Electronic quadrature trigonometric wrapping integration

To overcome the challenging constraints imposed by the unbounded nature of $\phi(t)$, we propose a quadrature trigonometric wrapping integration scheme. This architecture is implemented in a CMOS RF chip, whose block diagram is shown in Fig. 2. The photo-current is received and amplified by an integrated trans-impedance amplifier (TIA) and converted to a voltage that is fed to a variable gain amplifier (VGA). The TIA is based on a regulated cascode structure.

To achieve wrapping integration with proper scaling, a voltage-to-frequency converter followed by a trigonometric phase estimator block is used. Fig. 3 shows the block diagram of a direct V-to-F converter [4]. It consists of two loops. One loop converts voltage to frequency and the other loop adjusts the amplitude. Assuming ideal integrators and multipliers, the outputs of such a system can be written as

$$I_{out} = A \cos\left(\int v_{in} dt\right), \quad Q_{out} = A \sin\left(\int v_{in} dt\right). \quad (1)$$

This architecture emulates a VCO with a free-running frequency of zero. However, in a practical system with non-zero input offset, the center frequency of the V-to-F converter is nonzero. The schematic for the two integrators in Fig. 3(a) indicates that the integration is approximated by a low-pass filter created by lowering the output pole of an OTA. The amplitude restoration loop in the V-to-F

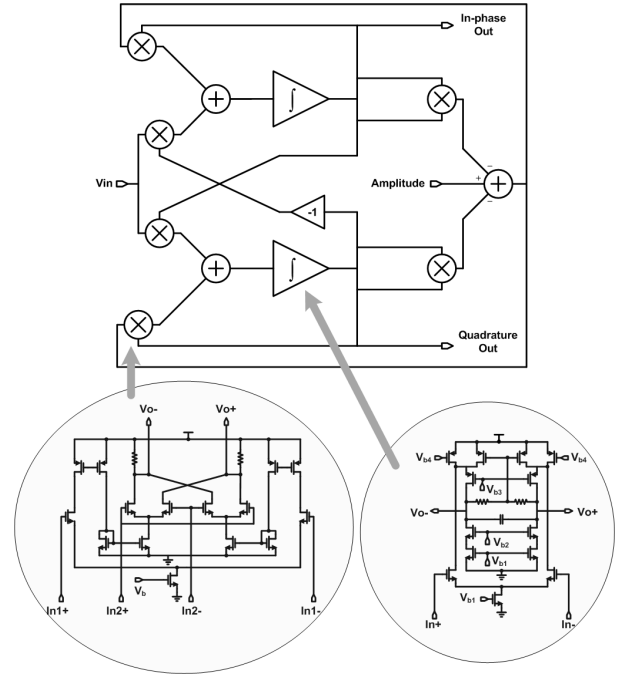


Fig. 3. (a) The block diagram of a direct voltage-to-frequency converter, (b) the folded balanced Gilbert cell multiplier, and (c) the non-ideal integrator.

converter brings the pole of this low-pass filter close to zero frequency, thus emulating an ideal integrator.

The trigonometric phase estimator takes the in-phase and quadrature signals generated by the V-to-F converter and calculates their phases. Its operation is based on the following robust phase approximation:

$$\phi \approx \frac{3.73 \sin(\phi)}{1.68 \cos(\phi) + \sqrt{\sin^2(\phi) + 4.5}}. \quad (2)$$

By using a simple sign detection scheme, Eqn. 2 can be used to estimate all values of $\phi \bmod 2\pi$. One main advantage of this approximation is that it can be implemented using only three basic functions, namely, a current divider, a squarer, and a square-rooter. The circuit schematic of these blocks are depicted in Fig. 4. The operation of the squarer and square-rooter circuits is based on the assumption of long channel length transistors operating in pinch-off. The sum and difference of the drain currents of M2 and M8 are proportional to the square of the differential signal applied between the gates of M4 and M5, and the square root of the drain current of M1, respectively. The current divider is designed based on the trans-linear circuits principle described in [5].

The modulator pre-driver in Fig. 2 is a V-to-I converter with adjustable gain and output DC voltage level.

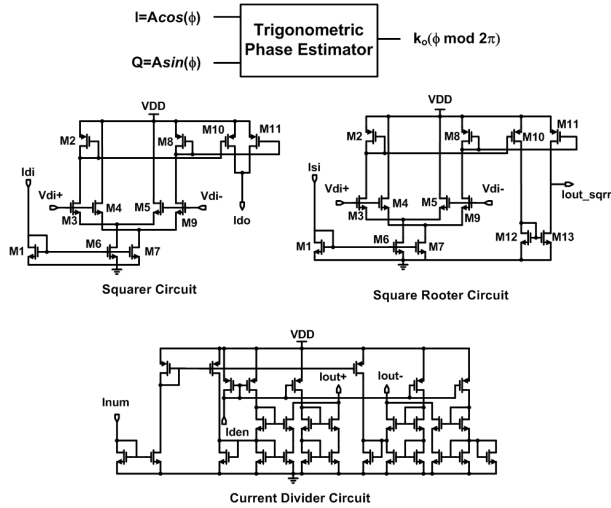


Fig. 4. The schematics of the squarer, the square-rooter, and the current divider as the building blocks of the trigonometric phase estimator are shown.

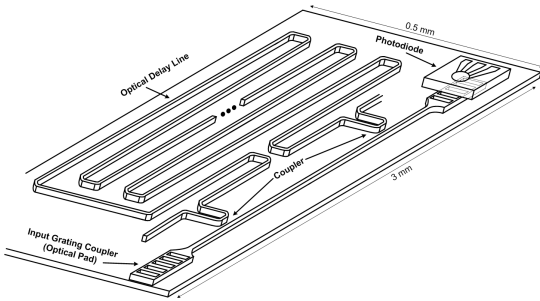


Fig. 5. The integrated frequency noise discriminator implemented in IMEC SOI process.

B. Photonic frequency noise discriminator

Figure 5 shows the integrated frequency noise discriminator implemented in IMEC SOI process with minimum feature size of 100nm. An integrated Mach-Zehnder interferometer (MZI) with delay difference of 400ps between its two arms is used to create interference between the coupled light and its time delayed version. This MZI is formed using SOI waveguides with 500nm width and 220nm heights. The directional couplers at the input and output are designed as 50/50 power splitter/combiner. The output of the MZI is backside-coupled to a photodiode forming a frequency noise discriminator. Grating couplers with loss of about 3dB are used as optical pads.

III. MEASUREMENT RESULTS

Figure 6 shows the micro-photograph of the RF chip fabricated in a 65nm CMOS process and the hybrid integration with photonic SOI chip (with 100nm minimum feature size) and the photodiode.

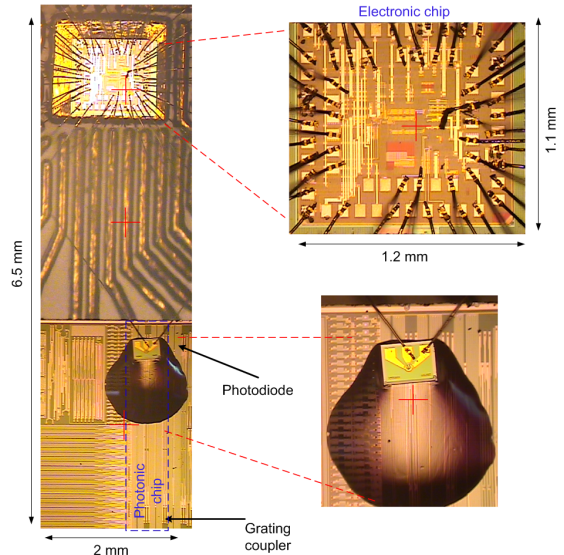


Fig. 6. The micro-photograph of the RF chip (fabricated in a 65nm CMOS process) and the hybrid integration with photonic SOI chip (with 100nm minimum feature size) and the photodiode.

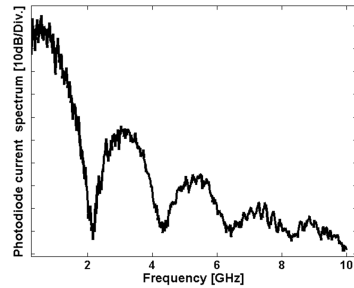


Fig. 7. The output frequency spectrum of the photonic frequency discriminator chip.

First, by coupling the output of a conventionally available DFB laser emitting 10mW optical power at 1553nm to the photonic chip the response of the photonic frequency noise discriminator is measured. Figure 7 shows the frequency spectrum of the photodiode current after electrical amplification. The response follows closely the behavior predicted in [2] and the null-spacing in the response represents 400ps of delay difference between MZI arms.

Figure 8(a) shows the measurement setup for the stand-alone RF chip. A noise source in conjunction with a 5kΩ resistor at the chip input provides a current noise with 10μA amplitude to the RF chip. This noise level is in the same order as the typical DFB laser discriminated frequency noise. The output of the RF chip pre-driver is captured using a real-time oscilloscope. As shown in Fig. 8(b), the input noise and the ideal derivative of the output (after about 4ns delay adjustment) are in close agreement

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

Ref.	Laser type	Phase noise reduction bandwidth	Linewidth original-reduced	Power consumption	Area	Method
[1]	External cavity	<1MHz	100kHz-1Hz	N/A	Bench-top	Electrical feedback
[2]	DFB	330MHz	2.6MHz-160kHz	>30W	Bench-top	Feed-forward
[3]	DFB	200MHz	7.5MHz-1.8kHz	>25W	Bench-top	Feed-forward
This work	DFB	200MHz	6MHz-250kHz	160mW*	Electronic chip: 1.32mm ² Photonic chip: 1.5mm ²	Feed-forward

*570mW including the external modulator driver.

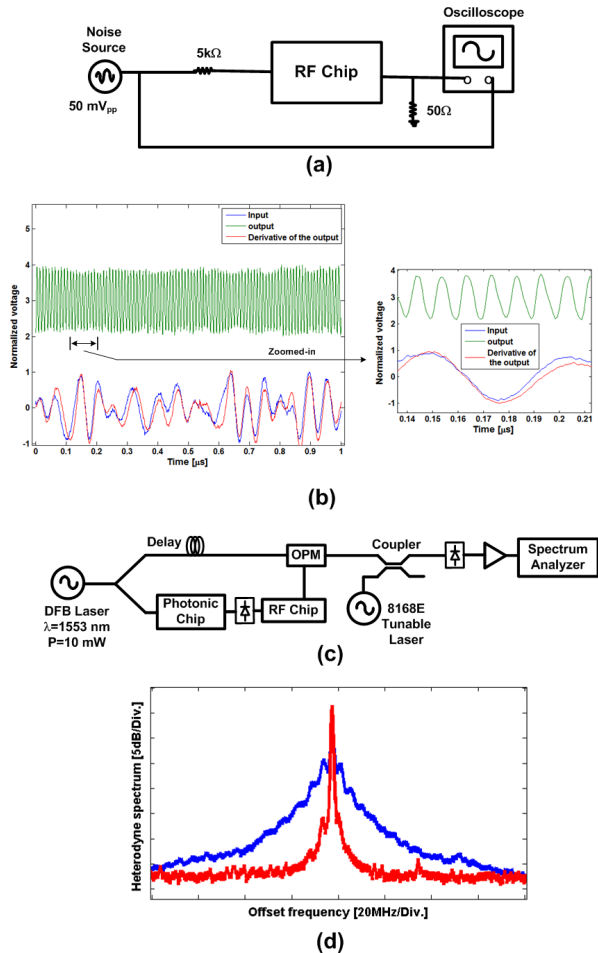


Fig. 8. (a) The RF chip stand-alone measurement setup, (b) the measured integration and wrapping performance of the RF chip, (c) the laser phase noise reduction measurement setup, and (d) the measured laser spectrum before and after phase noise reduction.

suggesting a close-to-ideal integration performed by the RF chip. The phase wrapping process can also be observed from the zoomed-in version of the pre-driver output.

Figure 8(c) shows the phase noise reduction measurement setup. The output of the OPM is down-converted to electrical domain by beating it with a tunable laser (with a

linewidth less than 50kHz) and monitoring the heterodyne spectrum. The heterodyne laser spectrum before and after phase noise reduction was measured, as depicted in Fig. 8(d). This measurement shows that the original linewidth of the laser is reduced from 6MHz to 250kHz, which is equivalent to approximately 14dB improvement in the phase noise. The performance of this work is compared with that of a few published works in Table I.

IV. CONCLUSION

In this paper, the first integrated laser phase noise reduction scheme is presented where RF techniques and architectures together with hybrid integration of the photonic and electronic chips enable dramatic power consumption and area reduction compared to bench-top designs. Using the proposed architecture, the phase noise of a commercially available 1553nm distributed feedback laser is improved by 14dB. This feed-forward phase noise reduction scheme is compatible with several types of lasers and performs wideband phase noise reduction over a 200MHz frequency range.

ACKNOWLEDGMENT

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