A 19.1dBm Segmented Power-Mixer Based Multi-Gbps mm-Wave Transmitter in 32nm SOI CMOS

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***Abstract* — A high-power, fully-integrated, mm-wave power mixer based transmitter capable of generating high-speed, complex non-constant envelope modulations is implemented in a 32nm SOI CMOS process. Segmented power generation approach is shown to be suitable for direct digital modulation as well as efficiency improvement at back-off power levels. The transmitter has a peak output power of 19.1dBm at 51GHz with a drain efficiency of 14.2% and a peak PAE of 10.1%. Measurements results show high-speed modulations for BPSK, QPSK, ASK, m-ASK and 16-QAM. Reliability of the transmitter has also been verified against worst case segmentation at 30% higher supply voltage.**

***Index Terms* — mm-wave, , Power Mixer, CMOS Power Amplifiers, Non-constant Envelope Modulation.**

I. Introduction

Energy- and spectrally-efficient mm-wave CMOS transmitters offer a compelling solution to address the insatiable demand for the ever increasing data-rates in portable high-speed systems. High output power levels are desirable for such systems to obtain reasonable range and data rates in practice [1]–[3]. Producing such large output power at high frequencies often requires combining power from a large number of amplifying stages, each of which can only handle small voltages and currents in these deeply scaled CMOS technologies. This necessitates a power combining strategy conducive to an integrated setting. However, many of the commonly used power combining strategies require a large die area or multiple chips, leading to excess cost and larger footprints that make them less attractive for most commercial applications.

Non-constant envelope modulation schemes rely on using both phase and amplitude modulation to achieve higher spectral efficiency. Although traditional transmitter architectures based on linear up-conversion and amplification are capable of handling such signals at power levels sufficiently below saturation, this comes at a significant efficiency penalty. Linearization schemes, such as polar modulation have been extensively studied at lower RF frequencies (i.e., several GHz) to utilize the high efficiency of a switching power amplifier, while transmitting non-constant envelope signals. The complexity and phase matching issues of such systems have limited their usage in mm-wave transmitters. Although some Cartesian architectures based on free-space signal combining have been proposed to avoid the efficiency hit due to on-chip power combining, they require a large chip area and complex system design in a practical setting [2].

In this paper a compact, high data-rate, integrated mm-wave transmitter has been demonstrated which maintains efficiency over a broad range of output power levels. Output power from multiple segmented power mixers [4] are combined using an energy- and area-efficient dual-primary distributed active transformer (DAT) [5]. Each power mixer segment is maintained at or near saturation leading to higher efficiencies during non-constant envelope modulation through segmentation.

II. Transmitter Design

A. System Architecture

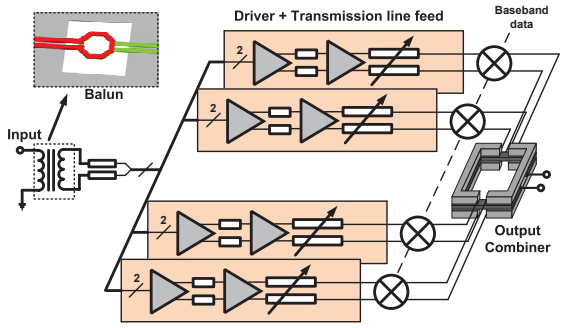

Fig. 1. System architecture of power-mixer based transmitter.

The overall system architecture of the power mixer transmitter is shown in Figure 1. A single-ended LO signal is first converted to a differential signal using an on-chip transformer and then distributed to four differential power mixers through driver stages. Each power mixer is segmented into 8 segments controlled by digital baseband bits. Depending on the desired instantaneous power level, one or more mixer segments are selectively activated, thereby eliminating unnecessary DC power consumption while generating various power levels that can be used for modulation and/or power control. The power mixer performs modulation/up-conversion and power amplification within the same block, which also eliminates the additional

power and area overhead of the matching networks between the up-conversion mixer and the power amplifying stage. The four power mixer elements are symmetrically power combined using a dual-primary DAT. It must be noted that while single-primary DAT based mm-wave power amplifiers have been reported [6], a dual-primary DAT allows convenient power combining of four elements while significantly reducing complexity of the input drive network. To maintain drive symmetry of the DAT, the two power mixers driving each primary utilize the same segmentation control. However, each primary can be driven with different segmentation levels at any instant, enabling 64 possible segmented output power levels by combining output powers from the two primaries. In order to mitigate any potential phase mismatch between the power mixer elements at these frequencies, the LO distribution paths are equipped with optional controllable delay lines, as shown in Figure 1.

B. Power Mixer Design

Figure 2 shows the circuit schematic of the output power-mixer stage and the interconnection between the segments of each power mixer. The power mixer elements are implemented as Gilbert cell stages with the mm-wave LO driving the bottom thin-oxide transistors (160μm/40nm). The output transistors are implemented with thick-oxide devices (120μm/100nm) to handle large output swings at the drain. Contrary to conventional segmented power generation where supply modulators are commonly used, direct amplitude modulation in this architecture is achieved by baseband signals applied to the gates of these output transistors. Efficient power generation

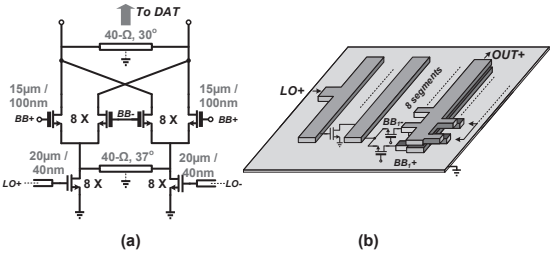

Fig. 2. (a) Power mixer circuit schematic and (b) interconnection between different segments.

through this segmented architecture requires careful device and interconnect modeling, as shown in Figure 2(b), where the drain nodes of the LO drivers as well as the baseband stages are connected over a distributed transmission line structure. High output power at mm-wave frequencies is achieved by combining output powers from four such stages, each delivering nearly 14dBm of saturated power.

C. Distributed Active Transformer

The output power combining of four power mixers is achieved through a low-loss dual-primary DAT based combiner, shown in Figure 3, which also achieves output impedance transformation through current combining. While such combining methodology has been demonstrated at low frequencies to be extremely efficient on-chip power combiners with convenient supply connectivity through virtual ground nodes, at mm-wave frequencies the complexity of input signal distribution limits its use for combining more than 2 differential power stages. In the present design, the secondary is sandwiched between the two primaries for maximum electromagnetic coupling (Fig. 3). Simulated maximum combining efficiency at 50GHz was 85.4%.

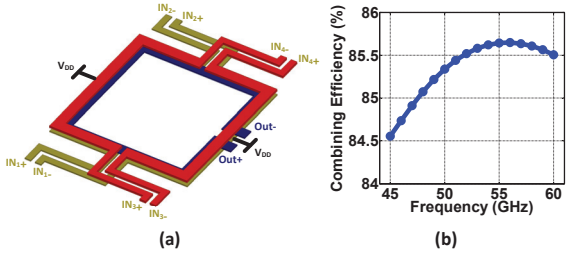

Fig. 3. (a) Dual-primary distributed active transformer (DAT) and (b) simulated power combining efficiency over frequency.

D. Input distribution and Driver Stage

The input balun is implemented using the top two metal layers placed directly on top of each other. Simulated excess insertion loss (in addition to the 3dB splitting factor) of the balun was 2.6dB at 50GHz. The driver stage is composed of several cascaded CMOS push-pull stages. To ensure proper mixer operation, these driver stages need to provide maximum voltage swing to the power mixer stage. Any mm-wave system composed

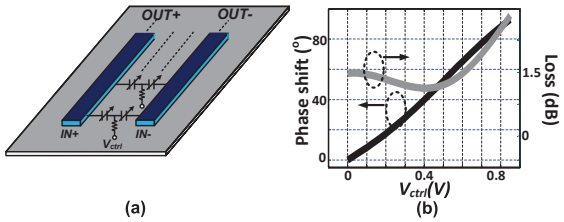

Fig. 4. (a) Distributed varactor based transmission line and (b) simulated phase shift and loss.

of several power combined unit cells is susceptible to phase mismatch between the stages thereby leading to load mismatch which in turn reduces the overall efficiency of the power combiner. To compensate for these inevitable phase mismatches due to process variations in the distribution network, optional phase shifters in the form of varactors (Fig. 4(a)) are incorporated into the transmission lines driving the power mixers. The controllable delay line achieves more than 90^o of phase shift at 50GHz over the control voltage range in simulation (Fig. 4(b)).

Measurement results show a degradation of output power by 1.1dB due to phase mismatch, which can then be reclaimed by tuning the varactor control voltages.

III. Measurement Results

A. Power and Segmentation Measurements

The transmitter is fabricated in a 32nm SOI CMOS process with two 1.2μm Cu and one 2.2μm Al levels with a core circuit area of 0.51mm^2 including the input and output pads, the input balun, and the DAT power combiner. Figure 5(a) shows the output power against input power measured by a single-ended power meter with the other output port terminated. The measured saturated output power of the transmitter is +19.1dBm at 51GHz and drain efficiency of 14.2% with a PAE of 10.1%. The power mixer has a maximum LO-to-RF gain of 16.2dB with 7dB gain in saturation, including the loss due to the input balun.

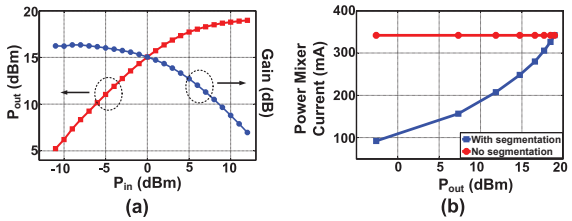

Fig. 5. (a) Transmitter output power and gain and (b) DC power savings in segmeneted operation.

An important functional characteristic of the segmented power mixer architecture is that the DC power drawn scales with the output power, which leads to higher efficiencies at back-off, as demonstrated in Figure 5(b), showing the DC current drawn by the output stages plotted against output power for two cases: one where input power is backed off for lower output power and the second where segmentation is applied to control power levels. Significant reduction in DC current was observed across all power levels, with a 40% reduction between the two cases at 12dBm output power. It must be noted that because the power mixer elements are switched on and off depending on the power requirement, the effective efficiency during non-constant envelope modulation is much higher compared to conventional transmitter systems. For example, the average DC current drops by 29% during binary-ASK modulation.

B. Modulation measurements

Figure 6 shows the measurement setup for high-speed modulation measurements. An arbitrary-waveform-generator (AWG) is used to generate phase modulation at a carrier frequency as well as the segmentation bits, enabling direct digital modulation. The IF signal is then up-converted using an LO of 50GHz and fed into the chip through a GSG probe. The differential output of the transmitter is probed using an SGS probe with one output terminated. An identical mixer then down-converts the signal using the same LO and demodulation is performed using MATLAB.

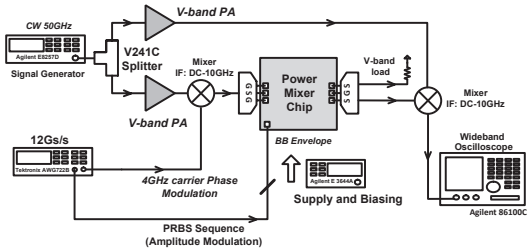

Fig. 6. Measurement setup for modulation measurements.

High data rate modulation is demonstrated at data rates of 4Gbps both for BPSK and QPSK with a 50GHz carrier. Figure 7(a) shows eye-diagrams for 2Gbps and 4Gbps BPSK without any equalization. Recovered constellation for QPSK modulation at 4Gbps is depicted in Figure 7(b) with an error vector magnitude of -15.56dB, a significant portion of which (67%) is contributed by the AWG sampling itself excluding the mixers.

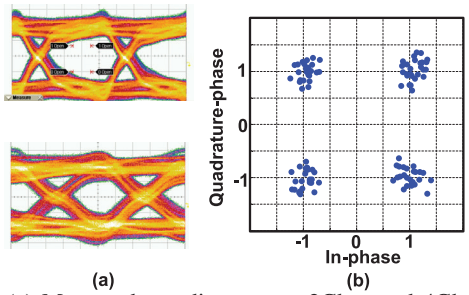

Fig. 7. (a) Measured eye-diagrams at 2Gbps and 4Gbps BPSK and (b) Recovered constellation for QPSK at 4Gbps.

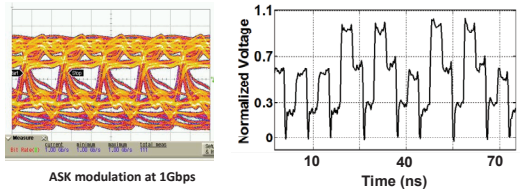

Fig. 8. (a) Eye diagram for ASK at 1Gbps (b) Demodulated symbols for duo-binary coding.

Direct digital control of the segmentation bits leads to ASK modulations as shown in Figure 8(a) at 1Gbps (limited by test setup) and 3-ASK at 500Mbps (Fig. 8(b)). For non-constant envelope modulation schemes, phase modulated LO signal at 50GHz is fed to the transmitter and power control is achieved through base-band segmentation bits. An example generation of a 16-QAM signal is shown in Figure 9(a) where the three amplitude levels are selected directly by the segmentation settings and twelve phases are generated at the LO frequency. Fig. 9(b) shows generated constellation for 16-QAM modulation with a raw EVM of -18.45dB.

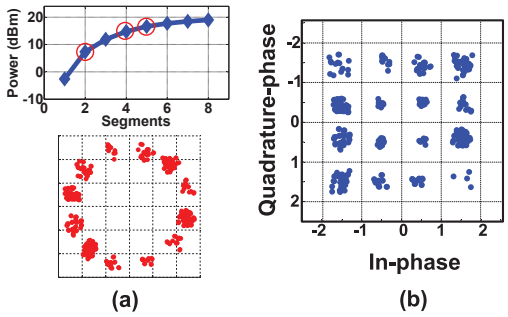

Fig. 9. (a) Amplitude and phase generation for 16-QAM signal (b) Generated 16-QAM constellation.

C. Reliability measurements

A typical problem in polar PA's or in a segmentation based architecture arises when the amplifier is operating at close to its maximum power, where one or two segments are off. While the output signal swing is still reasonably high, the off segments experience a large voltage swing across them, leading to long term reliability or breakdown issues. The reliability of the amplifier in the present design is verified by exposing it to full stress operational condition for extended time periods with the worst case segmentation, as shown in Figure 10. One of the 8 segments was kept off for progressively longer time periods while occasionally turning that segment on and verifying its reliability. No degradation of output power was observed at an increased supply voltage of 2.2-V over a 12-hour measurement window. Figure 11 shows the pad-limited die-photo of the implemented chip.

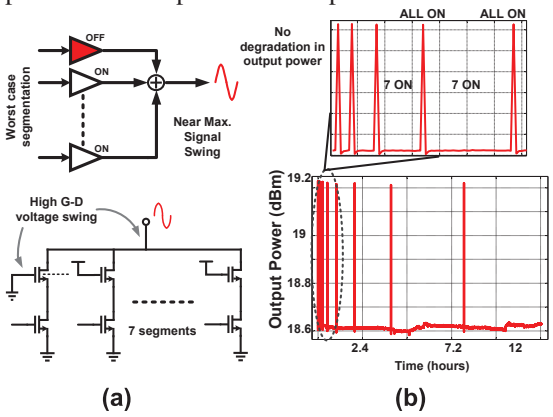

Fig. 10. (a) Worst case segmentation and (b) power measurements over time for the same.

IV. Conclusion

This paper presents a high-power, fully integrated mm-wave transmitter implemented in 32nm SOI CMOS capable of generating high-speed, non-constant envelope modulations with high-efficiency. The segmented power generation approach leads to significant DC power savings as well as efficiency improvement during non-constant envelope modulation. BPSK and QPSK modulations have been demonstrated at 4Gbps on a 50GHz carrier. High-speed ASK, m-ary ASK as well as 16-QAM measurements show the flexibility of the transmitter for a variety of modulation schemes.

TABLE I
Comparison with recently published work

Metric	This Work	[1]	[2]	[3]
Freq. (GHz)	50	60	60	45
Process	32nm SOI CMOS	65nm CMOS	65nm CMOS	45nm SOI CMOS
Power (dBm)	19.1	17.9	9.6[1]	24
V_{DD} (V)	1.7	1.0	1.0	5.1
PAE (%)	10.2	11.7	17.4[2]	14.6
Area (mm^2)	0.51	0.83	N/A	0.77
Modulations	ASK m-ASK, BPSK, QPSK 16-QAM	N/A	QPSK, 16-QAM	ASK, BPSK, QPSK

[1]One transmitter unit, no power combining, [2]Transmitter efficiency

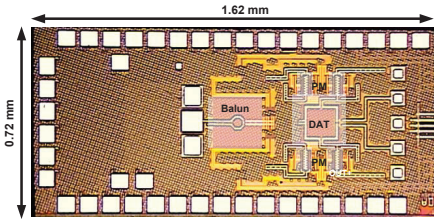

Fig. 11. Die-photo of the implemented transmitter.

Acknowledgment

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