15.3 A 0.28THz 4×4 Power-Generation and Beam-Steering Array

Kaushik Sengupta, Ali Hajimiri

California Institute of Technology, Pasadena, CA

Up until recently, the terahertz frequency range (0.3 to 3THz) has been mostly addressed by high-mobility custom III-V processes, bulky and expensive nonlinear optics, or cryogenically cooled quantum cascade lasers. A low-cost room temperature alternative will enable a wide range of applications in security, defense, ultra-high-speed wireless communication, sensors, and biomedical imaging not currently accessible due to cost and size limitations. CMOS can potentially provide such a low-cost platform, but it requires novel techniques and architectures to generate, manipulate, radiate, and detect signals above transistor f_{max}, which are in the sub-THz frequency region in most of today's nodes.

An efficient power generation and radiation approach for THz applications was presented in [1], where the distributed active radiator (DAR) was shown to radiate directly out of a silicon chip with high conversion efficiency from DC to THz EIRP (effective isotropic radiated power). Up to 4 DAR's were mutually injection locked to beam-form [1] and beam-steer [2] using two different coupling mechanisms. While it is possible to achieve coherent array operation on a small scale using injection locking, this approach is not scalable to larger arrays due to the complexity of the necessary coupling networks. Furthermore, in a mutual injection-locking setting, the center frequency of the radiated signal is determined by the consensus locking frequency of the elements, and is thus still collectively free running in nature.

In this work, we present a scalable array architecture for power-generation and beam-steering at THz frequencies with a centralized frequency generation scheme, compatible with phase and frequency locking to a low frequency external reference. As an example, a 4x4 element array is implemented in a 45nm SOI CMOS process (typical f_{max} ~190GHz and substrate resistivity of 13.5Ω-cm [6]) that achieves +9dBm EIRP between 0.27 and 0.28THz with 80° digitally controlled electronic beam-scanning in each of the orthogonal axes in 2D space (azimuth and elevation).

The proposed architecture is shown in Fig. 15.3.1, where the signals are generated and distributed at subharmonic frequencies to minimize the loss in signal distribution at high frequencies. An on-chip VCO with cross-coupled transistors serves as the central time-base that can be phase and frequency locked to an external low-frequency reference. It generates a tunable differential signal centered at 94GHz, which is one third of the radiation frequency. Two buffers distribute the generated signal to four symmetric midpoint junctions on the chip where single-ended divide-by-two blocks generate differential quadrature (I and Q) signals centered at 47GHz. These signals are then fed to individual phase rotators that are routed to each array element. The phase rotation is achieved by a digitally controlled weighted summation of the I and Q signals at 47GHz. The output of the each of the phase shifters with individual phase control drives injection-locked frequency triplers [3], whose oscillation frequencies are designed to be around 140GHz. The traveling wave oscillatory signal of each distributed active radiating element is injection locked to its corresponding tripler output, thus controlling the second harmonic of the DAR, which is the radiation frequency at around 280GHz as shown in Fig. 15.3.1. In this scheme, the phase rotation induced by each phase rotator, θ, at 47GHz directly translates to a phase shift of 6θ at the radiated frequency of 282GHz.

The schematics of the central time-base VCO and the buffers are shown in Fig. 15.3.2. The oscillator output is distributed to four symmetrical midpoint junctions with equal delays using carefully modeled symmetric transmission lines with equal path lengths. The oscillator core with buffers drive on-chip substrate-shielded differential coplanar striplines with grounded tub with an odd-mode characteristic impedance of Z_{00}=25Ω. The t-lines branch out into two matched differential t-lines with Z_{00}=50Ω and distribute the differential signals to drive eight single-ended injection-locked divide-by-2's, as shown in Fig. 15.3.1 and Fig. 15.3.2. The inputs of the divide-by-2's are matched to 50Ω for maximum power transfer to ensure wide locking range over process variations and frequency tuning range. The phase rotator performs a weighted sum of the quadrature signals by current addition via two current-commuting (Gilbert) cells, as shown in Fig. 15.3.2. The phase-control voltages are generated through a digital serial interface and a 6b on-chip DAC. The output of each of the phase rotators with individual phase control drives injection-locked frequency triplers [3] through a t-line matching network, as illustrated in Fig. 15.3.2. Each of the 16 distributed active radiator elements, which are self-sustaining traveling-wave oscillators [1] are locked to their associated tripler outputs. The active radiators have the same fundamental oscillation frequency as the tripler output but radiate power efficiently only at the second harmonic, i.e., 280GHz, as shown in Fig. 15.3.3 [1]. In a DAR, signal generation, frequency doubling, quasi-optical filtering of the undesired fundamental and radiation of the desired signal at the doubled frequency all happen simultaneously and locally [1]. This allows it to achieve much higher DC-to-THz EIRP conversion efficiency than a conventional frequency-generation and multiplication chain connected to a tuned antenna. The DAR is particularly suitable for high-efficiency radiation through the substrate, even un-thinned [1]. Due to thermal considerations in such a large-scaled integrated system, the substrate is back-lapped to 70μm and then mounted on brass to radiate from the top side, as shown in Fig. 15.3.3.

The chip is implemented in a 45nm digital SOI CMOS process with 2.1μm thick top aluminum layer, with typical f_{max}~190GHz [6], and substrate resistivity of 13.5Ω-cm. The chip measures 2.7×2.7mm^2 and the radiating elements are separated by 500μm which corresponds to approximately $\lambda/2$ placement in air and $3\lambda/2$ of the dominant substrate mode in silicon leading to partial substrate mode cancellation and increased radiation efficiency.

The measurement setup is shown in Fig. 15.3.4. The chip is mounted on brass and the PCB supports the low-frequency digital signals and the power supplies. The traveling-wave radiators on-chip radiate circularly polarized modes from the top-side of the chip which is captured by a 25dB gain linearly polarized diagonal WR-3 antenna (220 to 325 GHz) and then downconverted by a harmonic mixer and analyzed using a spectrum analyzer [1]. Due to polarization mismatch, only half of the available free-space power is captured by the receiver. The setup is calibrated by using an Erickson power meter. The calibrated sub-THz spectrum at 280.7GHz, detected at far-field distance of 50mm, is also shown in Fig. 15.3.4. The 8μW power captured translates to a broadside EIRP of +9.4dBm. The chip was rotated through a 90° span during which the power captured did not vary significantly, verifying the circular polarization of the radiated beam.

The frequency of the radiated signal, limited by the locking range of the tripler, is tunable between 276 and 285 GHz by controlling the tuning voltage of the central VCO (92 to 95GHz). The architecture is compatible with phase and frequency locking to a low-frequency external reference. Phase noise of the free-running central VCO at 94GHz is measured to be at -112dBc/Hz at a 10MHz offset. The measured broadside EIRP over the frequency range is greater than 9dBm for the entire tuning range, as shown in Fig. 15.3.4. The measured radiation patterns at 0.28THz are shown in Fig. 15.3.5. The broadside directivity is measured to be 16.6dBi and electronic beam-steering range is shown to be approximately 80° in each of the two orthogonal directions in space. The performance of the sub-THz transmitter is summarized in Fig. 15.3.6. The die micrograph is shown in Fig. 15.3.7. While previous works [4,5] have demonstrated feasibility of smaller components for THz power generation on-chip, this work introduces a scalable array architecture for radiating and beam-steering efficiently from silicon chips, with 200x higher EIRP compared to previous results [7].

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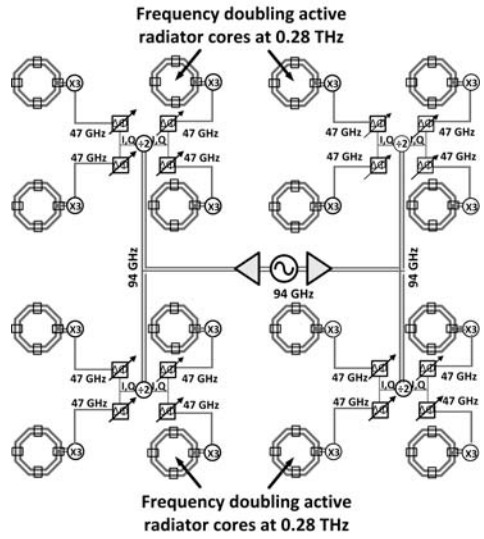

Figure 15.3.1: Proposed scalable architecture of the integrated THz power generator and beam-steering array.

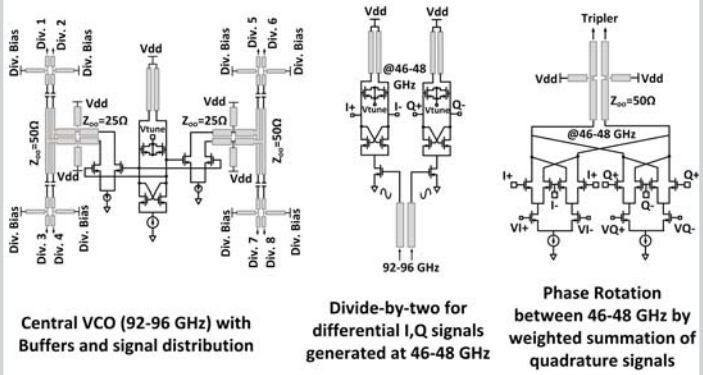

Figure 15.3.2: Circuit schematics showing central VCO, buffers and signal distribution, frequency divider for I,Q generation for phase shifting and phase rotation by weighted summation of quadrature signals.

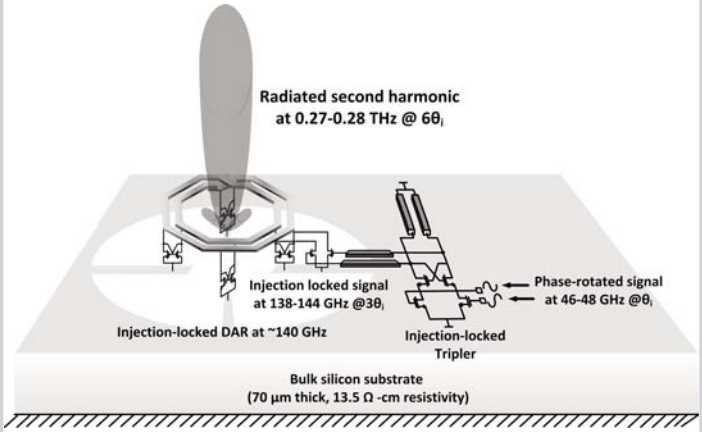

Figure 15.3.3: Injection-locked tripler with the coupled distributed active radiator for each element of the array. The figure shows frequency and phase multiplication and radiation at 0.28THz from a grounded substrate of 70μm thickness.

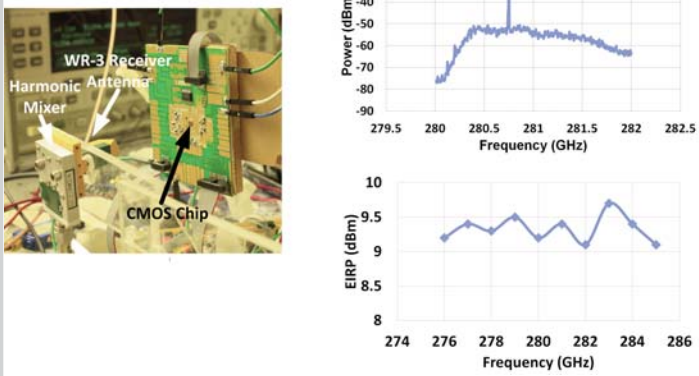

Figure 15.3.4: Measurement setup showing chip radiating from the top-side which is captured by the calibrated receiver. The figure shows the calibrated received signal at 280.7GHz. The figure also shows that broadside EIRP remains above 9dBm over the entire frequency tuning range.

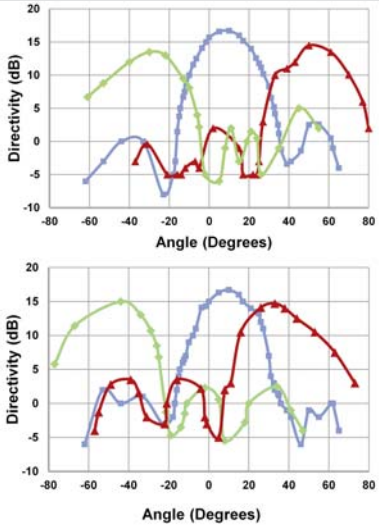

Figure 15.3.5: Measured radiation patterns at 0.28THz showing broadside radiation and beam-steering of around 80° in 2D space.

Chip performance summary

Transmitter Performance

Frequency of operation	276-285 GHz
Maximum broadside EIRP	+9.4dBm
Total radiated power (broadside)	190μW
EIRP flatness	less than 1dB between 275-285 GHz
Beam-steering	80° in each of the orthogonal axes in 2D space
Beam-steering resolution	continuous (limited by DAC resolution in practice)
Side lobes ratio	>10dB
Central time-base VCO tuning range	90.2-98.5 GHz

Power consumption

Central VCO and Buffers @1.1V	30mA
Divide-by-two elements (total of 8) @1.1V	8mA per element
Phase-rotators (total of 16)@1.1V	22mA per element
Triplers (total of 16) @1.1V	4mA per element
Distributed active radiators (total of 16) @0.8V	20mA per element

Figure 15.3.6: Chip performance summary.

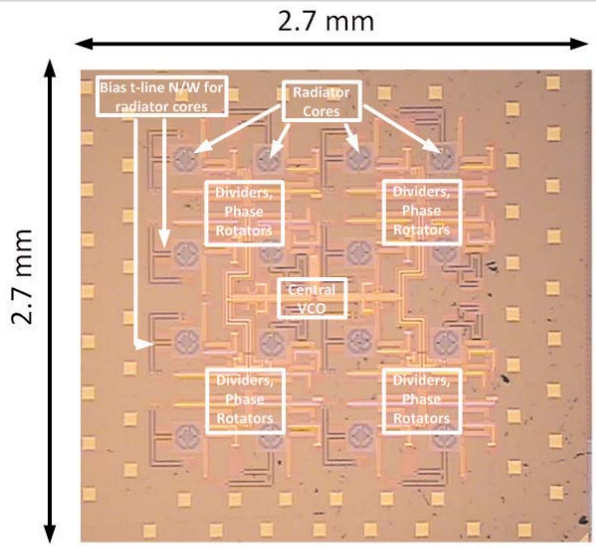

Figure 15.3.7: Die micrograph showing component placements.

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