23.1 A Millimeter-Wave Intra-Connect Solution

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The number and bandwidth of the internal I/O's in today's highly sophisticated electronic systems have grown faster than the external ones [1]. This demand for multiple, high-speed short-range internal I/O's results in several product design issues. In many cases, the number of I/O's, instead of actual circuits, determines the SoC chip size. The wires and connectors limit mechanical design flexibilities and the physical and topological challenges of such wired interconnects can affect the system performance and reliability. Furthermore, wired connections are never free as they require additional on-chip drivers to maintain signal integrity. This results in additional dynamic power dissipation and adds to the component and implementation costs of the system.

It is paramount to find a solution for these issues. Any such solution must also satisfy small area, cost, and power consumption requirements while providing enough transmission range between the chips and the boards. Capacitive and inductive coupling type inter-chip communication systems were reported in [2,3]. They satisfy the data rate, size, and power consumption requirements but need almost immediate proximity with precise alignment of the couplers. Millimeter-Wave wireless interconnect systems, an example of which is reported in [4], have a longer transmission range but the systems reported so far are power hungry and occupy too much area to be useful as an Intra-Connect solution (connections within a system box between boards, modules, etc.). This paper presents an 11Gb/s mm-Wave system suitable for wireless Intra-Connect solutions (Fig. 23.1.1).

The system utilizes a free-running TX LO and injection-lock carrier synchronization. This combination reduces the size and power consumption of TX and RX circuits. The transmitter consists of a TX LO, a Gilbert-Cell mixer, and a TX amplifier, as shown in Fig. 23.1.2. The TX LO, a free-running cross-coupled oscillator, generates differential LO signals, which are applied to the mixer at the gates of transistors M_3 and M_4. This direct connection reduces the area and power consumption of the circuit. The differential input data is supplied to the gates of transistors M_5, M_6, M_7, and M_8 to modulate the LO signal. The carrier level of the modulated signal is controlled by adjusting the DC voltages superimposed on the input data signals. The modulated signal is delivered to the 3-stage TX amplifier that has a peak gain of 14dB, a P_{1dB} of -2dBm, and a saturated output power (P_{sat}) of +4dBm. The amplified signal is transmitted by the antenna subsequently. The TX chip has an output power of 0dBm at 58GHz, a 3dB bandwidth of 10GHz, and a power consumption of 29mW at a supply voltage of 1.1V. The active footprint is 0.06mm^2.

The RX is a direct conversion receiver and consists of an LNA, an injection path circuit, an RX LO, a mixer, a DC offset cancellation circuit, and a wideband baseband amplifier, as illustrated in Fig. 23.1.3. The LNA amplifies the signal received from the RX antenna. It achieves a peak gain of 18dB, 3dB bandwidth of 11GHz from 52 to 63GHz, and an NF of 7dB. The LNA output is delivered to the mixer and to the RX LO via the injection path circuit. The injection path circuit controls the injection level by adjusting the bias voltage, V_{IL}. The DC offset due to the carrier component of the received signal is compensated at the output of the direct conversion mixer. The baseband amplifier is designed to have a gain of 10dB, a bandwidth of 8GHz and consumes 11mW. The RX chip has a conversion gain of 20dB at 58GHz, a 3dB bandwidth of 8GHz, an OIP3 of -3.9dBm, and dissipates a total power of 41mW. The active footprint is 0.07mm^2.

Figure 23.1.4 shows the measured injection locking range. For an RF input power of -30dBm, the locking ranges are 60MHz, 110MHz, and 160MHz at V_{IL} of 0.6V, 0.8V, and 1.0V, respectively. A 2GHz carrier was transmitted through TX and RX, and the input and output phase noises were compared. The measured input and output carrier phase noises at 1MHz offset were -141dBc/Hz and -123dBc/Hz, respectively.

The fabricated Intra-Connect demonstrator achieves 11Gb/s at 56GHz over a transmission distance of 14mm. Figure 23.1.5 shows the demonstrator setup. It utilizes ASK with a modulation depth of 150%. Bonding wire antennas with a measured gain of 0dBi are used for both TX and RX. The observed BER is less than 10^{-11} for 2^7-1 PRBS as the input data stream.

This Intra-Connect solution can be scaled to multiplexed channels using directional antennas to create separation among various channels and minimize the crosstalk. Moreover, as long as these low-power Intra-Connects are confined within the box with low leakage, several different frequencies can be used for frequency multiplexing in addition to the spatial multiplexing obtained through a directional antenna. In the long run, electronically steerable phased arrays can be used to provide dynamic and flexible signal routing [5].

The demonstrated 11Gb/s mm-Wave Intra-Connect chips were fabricated on 40nm Low-Power Logic CMOS and occupy an active footprint of 0.13mm^2 per channel. The energy efficiency of the system is 6.4pJ/bit. The results are summarized in Fig. 23.1.6, and the die micrographs of TX and RX chips are shown in Fig. 23.1.7.

References:
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[2] Q. Gu, et al., "Two 10Gb/s/pin Low-Power Interconnect Methods for 3D ICs," *ISSCC Dig. Tech. Papers*, pp. 448-614, Feb. 2007.
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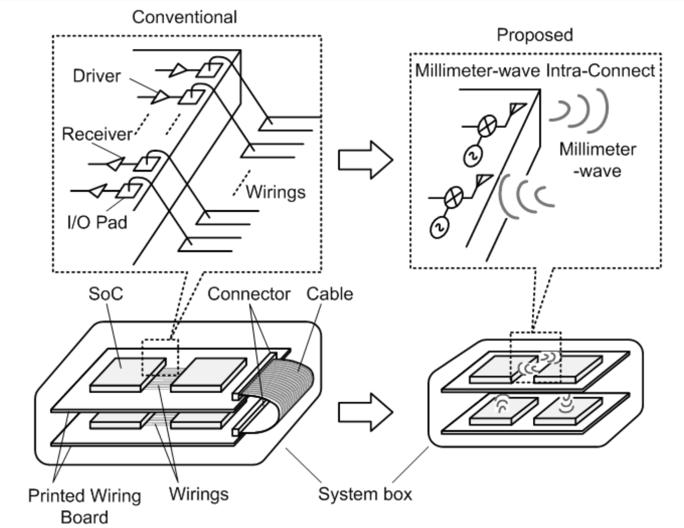

Figure 23.1.1: Concept of "millimeter-wave Intra-Connect" system (left: conventional approach, right: proposal).

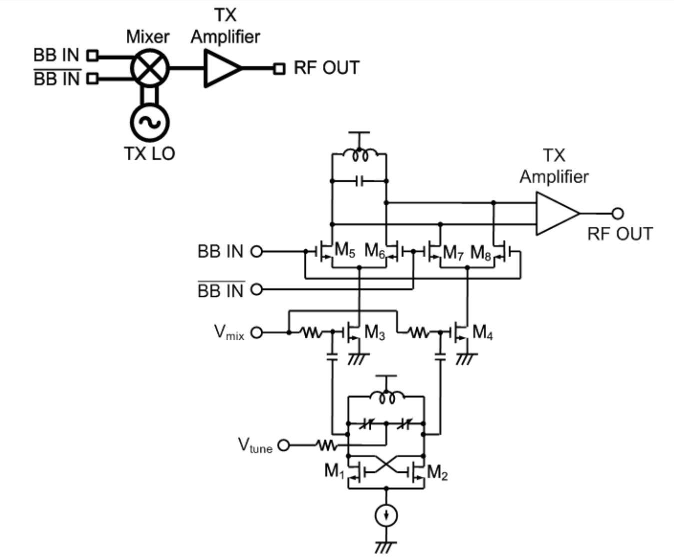

Figure 23.1.2: Circuit diagram of TX.

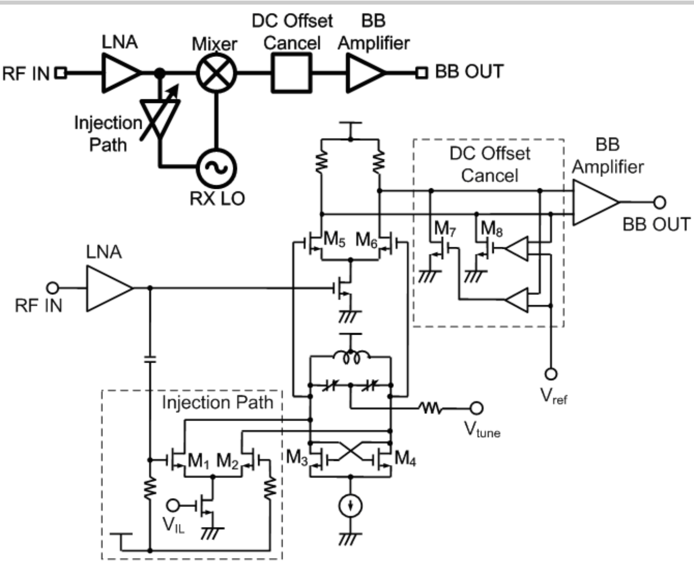

Figure 23.1.3: Circuit diagram of RX.

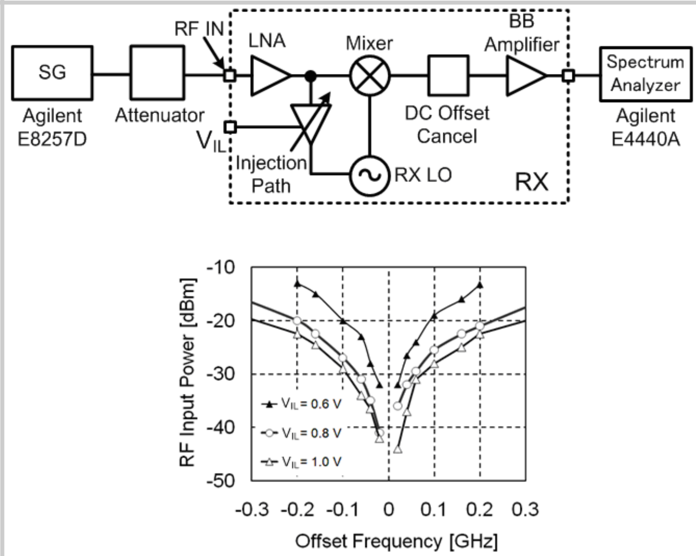

Figure 23.1.4: Measured injection locking ranges.

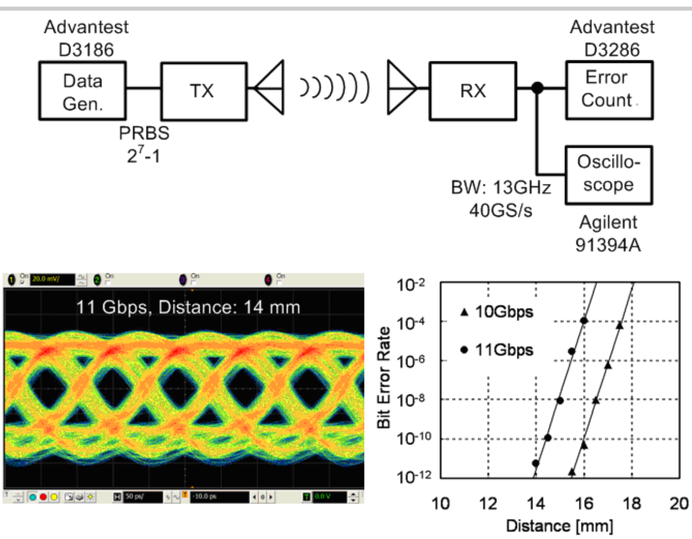

Figure 23.1.5: Millimeter-wave Intra-Connect demonstrator setup, 11Gbps eye diagram at RX output, and BER performance.

	This work	[4]	[2]	[3]
Frequency	**56 GHz**	60 GHz	25 GHz	Baseband
Coupling	**Antenna**	Antenna	Capacitive	Inductive
Modulation	**ASK**	OOK	ASK	Pulse
Data rate	**11Gbps**	2.5Gbps	11Gbps	11Gbps
Transmission distance	**14mm**	40mm	0.003mm	0.015mm
Power dissipation	**Tx: 29mW** **Rx: 41mW**	Tx: 183mW Rx: 103mW	4.3mW	15mW
Enery efficiency	**6.4pJ/bit**	114pJ/bit	0.39pJ/bit	1.4pJ/bit
Active footprint	**Tx: 0.06mm^2** **Rx: 0.07mm^2**	Tx: 0.43mm^2 Rx: 0.68mm^2	0.0021mm^2	0.015mm^2 (channel area)
Process	**40nm CMOS**	90nm CMOS	180nm CMOS	180nm CMOS

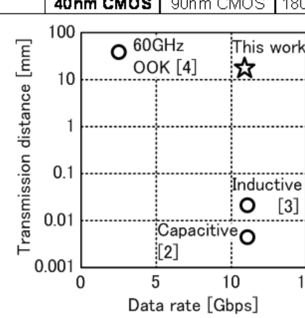

Figure 23.1.6: Comparison with other works.

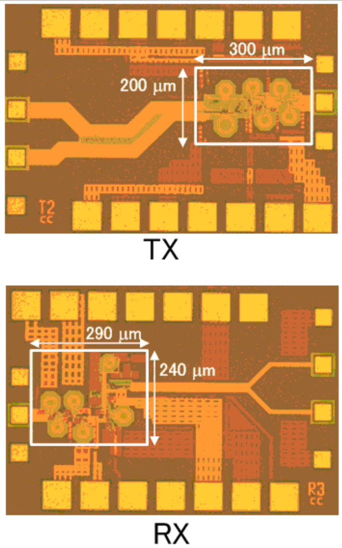

Figure 23.1.7: Die micrograph.