A 2x2 Dynamic Polarization-Controlling Integrated Phased Array

Amirreza Safaripour[1], Steven M. Bowers[1,2], Kaushik Dasgupta[1,3], and Ali Hajimiri[1]
[1] California Institute of Technology, Pasadena, CA 91125, USA
[2] University of Virginia, Charlottesville, VA 22904, USA
[3] Intel Corporation, Hillsboro, OR 97124, USA

***Abstract*— Radiator arrays with Dynamic Polarization Control (DPC) and 2D beam steering enable polarization matching to the receiver antenna regardless of its polarization, orientation, and location. A fully integrated 122.9 GHz 2x2 DPC multi-port driven phased array radiates all linear polarizations (0°-180° polarization angles) with axial ratios above 14 dB, and controls the axial ratio from 1.2 dB (circular) to 17.8 dB (linear) with a maximum EIRP of +12.3 dBm and 2D beam steering of up to 15°.**

***Index Terms*— Antenna arrays, CMOS integrated circuits, Electromagnetic radiation, Phased arrays, Millimeter wave integrated circuits, Beam steering.**

I. Introduction

Polarization matching between transmitter and receiver antennas in wireless communication links is a significant factor that directly affects the efficiency of the link, since any polarization mismatch between the two antennas introduces additional coupling loss on top of the free-space propagation loss. This phenomenon is even more important in mobile wireless applications where the orientation and location of the receiver antenna is continuously changing with respect to the transmitter. In such cases, transmitters that utilize a fixed linear polarization would not be able to communicate efficiently since accurate alignment is required for linearly polarized links. Alternatively, if a circularly polarized transmitter is used, the orientation dependence will only reduce for a receiver antenna with circular polarization of the same handedness (at the cost of narrower polarization bandwidths and beamwidths), while for a linearly polarized receiver only half of the energy would be coupled.

Dynamic Polarization Control (DPC) is introduced in [1] as a solution to overcome polarization mismatch. A unit element DPC antenna is capable of transmitting all polarizations (linear, circular, and elliptical) based on the receiver's need. Furthermore, DPC antennas can be phased properly in an array to form a more directive beam with higher power and to steer it towards a target while maintaining polarization matching (Fig. 1). Thus, a two-dimensional (2D) phased array of DPC antennas ensures polarization matching to the receiver within the 2D steering range of the DPC phased array regardless of the polarization of the receiver, its orientation in space, or its location. In this work, an integrated 2x2 array of DPC antennas is implemented to demonstrate these features.

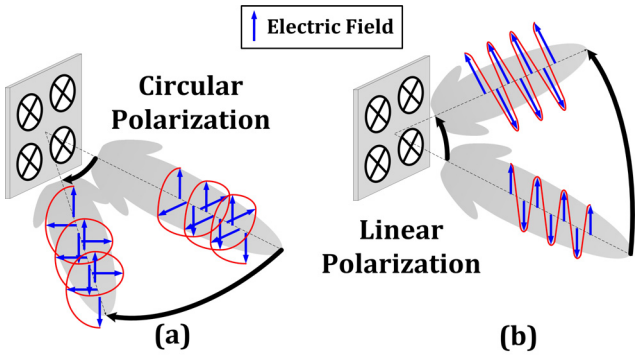

Fig. 1. Two-dimensional phased arrays of DPC antennas are capable of transmitting any desired polarization—for example circular (a) or linear (b)—at any direction within the 2D steering range to ensure polarization matching.

II. Design

A 122.9 GHz 2x2 DPC radiator array is designed in a 32nm CMOS SOI process. The simplified block diagram of the system is shown in Figure 2. It consists of four antenna elements, each with independent DPC capability [1]. Power is generated locally within each element's core through two differential oscillators whose outputs are then amplified to drive the antenna ports. Each of the two oscillators is independently phase-controlled with respect to the phase of a central quadrature oscillator (QVCO). The quadrature outputs of this QVCO are routed to all four cores through a central locking network to both synchronize the frequencies and allow full 360° phase control within each radiator by providing in-phase (I) and quadrature (Q) components of the fundamental frequency.

A. Antennas

Each of the four antennas in the array is a multi-port driven antenna [2]. They operate by driving a ring at four ports against a set of ground spokes. Each pair of opposite ports is driven differentially with the same amplitude as a subpart, but independently in phase and amplitude from the other subpart pair of ports on the orthogonal spoke. The drives of each antenna subpart generate far-field linearly polarized radiation aligned with the subpart's spoke [1]. These independent drives allow the antenna to transmit various polarizations by adjusting the relative phases and amplitudes of the two antenna subparts.

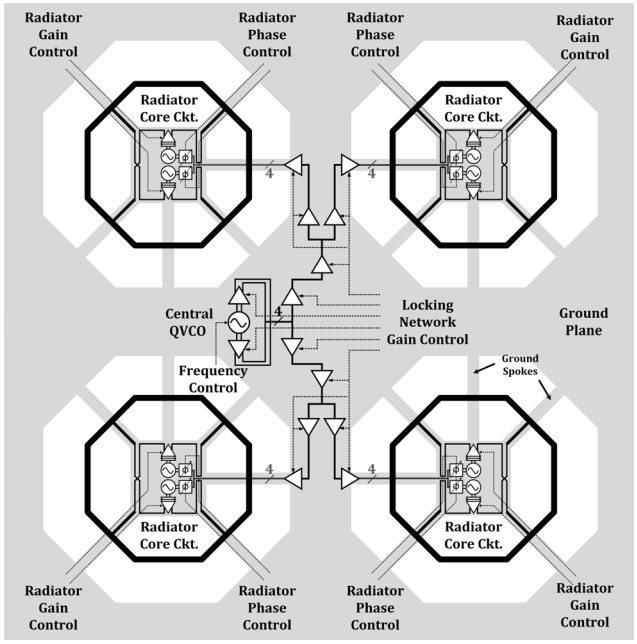

Fig. 2. Simplified block diagram of the 2x2 DPC radiator array with independent phase and gain control of each antenna element and frequency control of the entire array through QVCO tuning.

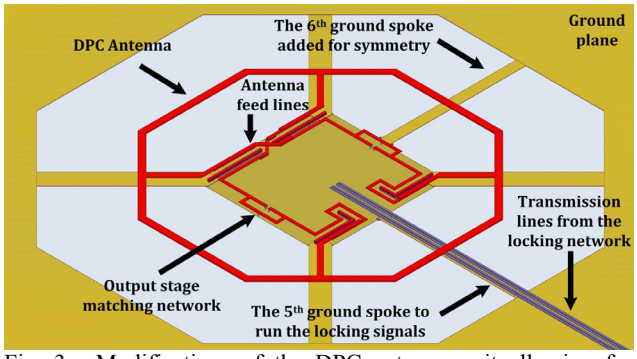

Fig. 3. Modifications of the DPC antenna unit allowing for transmission lines to run above the ground plane while preserving polarization symmetry.

One challenge in making arrays of these antennas is distributing a locking signal to the core circuitry at the center of each antenna. The distribution transmission lines must be run along one of the ground spokes to maintain a consistent voltage reference. In [1] the locking signals were run underneath one of the four spokes used to drive the antenna, requiring low metal layer transmission lines that introduced significant loss in the distribution network. To alleviate this issue, a 5th ground spoke was added for the locking signal distribution, allowing transmission lines to run above the ground spoke with less loss. This spoke is still run orthogonal to the antenna ring, minimizing mirror currents and having as small an effect on the radiation pattern as possible, but it does not drive the ring directly. The 5th spoke does add some undesired asymmetry to the design, and thus a 6th ground spoke was also added to help preserve that symmetry (Fig. 3) so that one polarization would not be favored over another. The array of four antennas is designed to be fabricated onto a substrate about one quarter wavelength in thickness that is then mounted onto a ground plane to enable top-side radiation. The full chip was simulated with Ansys HFSS FEM 3D electromagnetic solver and yields a radiation efficiency of 7% (from the drains of the output transistors to far-field radiation, including all antenna feed lines and the output stage matching network), a maximum gain in the broadside direction of 0.3 dBi, and an antenna pattern shown in Figure 4.

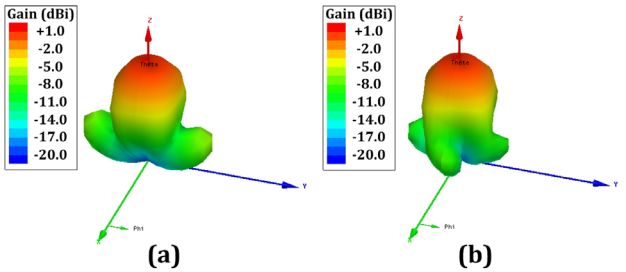

Fig. 4. Simulated patterns of antenna gain for the array with maximum gain of 0.3 dBi for linear (a) and 0.2 dBi for circular (b) polarization modes in the broadside direction.

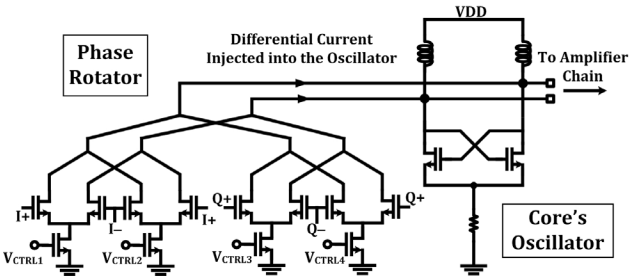

Fig. 5. Schematics of each phase rotator and its corresponding oscillator. The output current of the phase rotator is directly injected into the oscillator output nodes.

B. Antenna Drive Circuitry

Two independent differential cross-coupled oscillators inside each element's core generate the required power to drive its antenna. Each oscillator is injection locked to the phase of the output current of a phase rotator consisting of two Gilbert cells which are fed by I and Q lines of the locking network, and, through proper weighted summation, produce a differential current with the desired phase. The differential output current of each phase rotator is directly injected into the output nodes of the corresponding oscillator to both synchronize its frequency with the central QVCO and set its phase to the desired value. Figure 5 shows the schematics of each phase rotator and its corresponding oscillator. The outputs of each oscillator are then amplified through three stages of differential cascode amplifiers whose gain can be controlled through

bias adjustment. An integrated digital interface and on-chip DACs are implemented to enable digital control of the phase and gain settings.

C. Locking Network

The central QVCO is formed by two mutually coupled differential cross-coupled VCOs that generate quadrature signals at 122.9 GHz. They are coupled to each other through two mechanisms: parallel transistor coupling and resistive coupling (Fig. 6**).** The quadrature outputs of the QVCO feed a buffer network, which distributes them to the four radiator cores. The amplification, distribution, and splitting of the signals are done in a distributed fashion through six stages of amplification. All buffers are differential cascode amplifiers and are sized properly for impedance matching and maintaining the signals' power at the required level for the phase rotators' inputs.

III. Measurements

The chip is fabricated in a 32nm CMOS SOI process. It is mounted onto a PCB and attached to a 2D stepper motor for antenna pattern measurements. A 22.7 dBi gain horn antenna placed 10.5 cm away from the chip receives the radiated signal, as shown in Figure 7. The horn antenna feeds a 10th harmonic mixer – IF amplifier – spectrum analyzer/IF power meter chain to allow spectrum and IF power measurements. The entire setup is calibrated with a PM4 Erickson power meter. The radiator analog circuitry consumes a total of 1.726 W from 1.25 V and 1.4 V supplies while the digital interface and the DACs consume 159 mW. The total area of the chip is 2.85 x 2.85 mm^2.

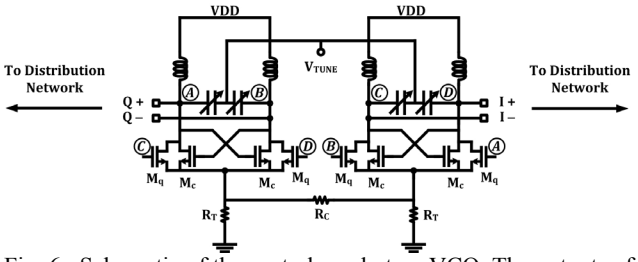

Fig. 6. Schematic of the central quadrature VCO. The outputs of this QVCO are routed to the four cores to enable both phase control and frequency synchronization.

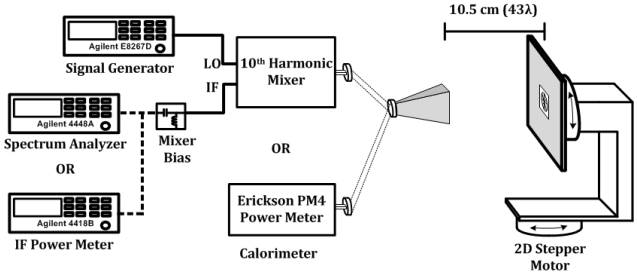

Fig. 7. Measurement setup for the 2x2 DPC radiator array with a 10th harmonic mixer to a calibrated spectrum analyzer and IF power meter.

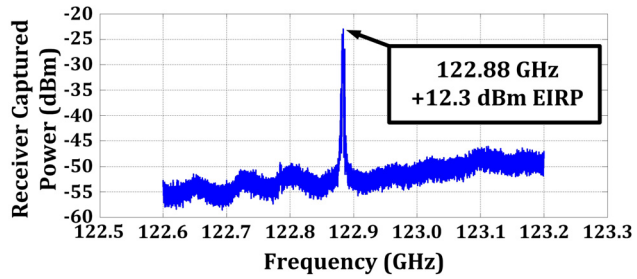

Fig. 8. Measured calibrated spectrum in linear polarization mode shows a 122.88 GHz tone with a maximum EIRP of +12.3 dBm.

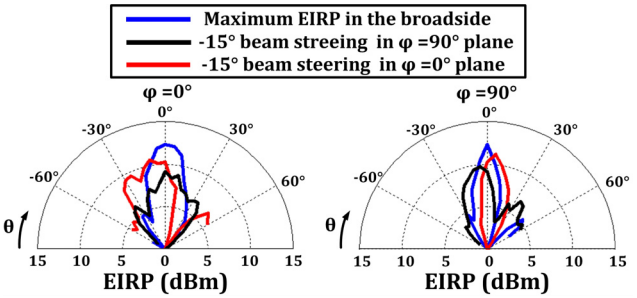

Fig. 9. Measured antenna pattern for beams in three directions in orthogonal planes show 2D beam steering of up to 15°.

The spectrum of broadside radiation is measured with the calibrated spectrum analyzer showing a maximum EIRP of +12.3 dBm at 122.9 GHz (Fig. 8). The measured antenna pattern shows 2D beam steering along the two orthogonal planes of $\varphi = 0°$ and $\varphi = 90°$ up to 15° for linear polarization at a 180° polarization angle (Fig. 9).

To demonstrate reliable polarization control of the radiated signal, a gradient descent based optimization algorithm is used to calculate the settings for any defined polarization goal (linear, circular, or elliptical with a certain axial ratio). With such an algorithm, possible deviations due to process variations and delay mismatch between transmission lines can be compensated for. Figure 10 shows the results of the optimization process where linear polarizations at broadside ($\theta = 0°$) for the full range of polarization angles (0° to 180°) are achieved. For each polarization angle the axial ratio is maximized to meet a pre-defined threshold of 14 dB and the goal is met in all measured polarization angles. The same algorithm is used to demonstrate the tuning ability of the axial ratio for elliptical polarization. To exhibit this, the optimization goal is set to arbitrary axial ratios (10 dB, 7 dB, and 4 dB) at arbitrary polarization angles (30° and 90°), and it results in elliptical polarizations with the desired axial ratios at the target polarization angles (Fig. 11). The radiator can also transmit circular polarization with an axial ratio of 1.2 dB, as shown in Figure 11, which was the minimum axial ratio achieved, measured at broadside. A comparison against other integrated silicon-based radiating sources above 100 GHz without external dielectrics is presented in Table I, and the die photo is shown in Figure 12.

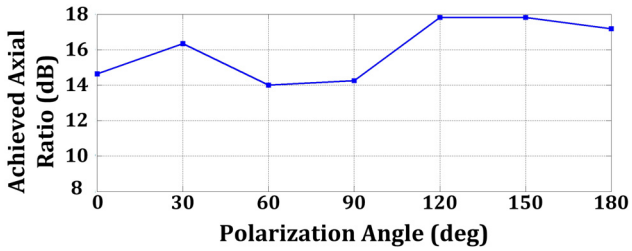

Fig. 10. Polarization angle tuning across the full 0°-180° range while maintaining linear polarization with axial ratios above 14 dB for broadside radiation.

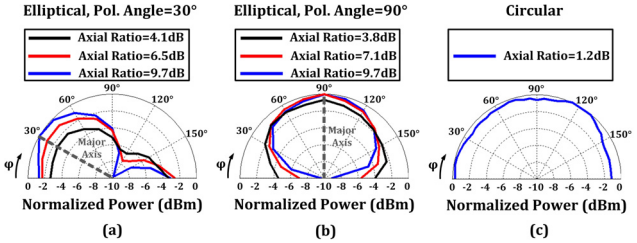

Fig. 11. Axial ratio tuning. Normalized plots of projected polarization at different angles in broadside show the ability to tune the axial ratio of elliptical polarization to the desired values at polarization angles of $\varphi = 30°$ (a) and $\varphi = 90°$ (b) as two examples, as well as generating circular polarization (c).

IV. Conclusions

Dynamic Polarization Control (DPC) of 2D phased arrays is a means to ensure polarization matching between transmitter and receiver antennas regardless of the polarization of the receiver antenna, its orientation in space, and its location, within the 2D steering range of the array. DPC was demonstrated on a 122.9 GHz 2x2 integrated phased array with full 0° to 180° tuning range of polarization angle, and a measured axial ratio tuning range of 1.2 dB to 17.8 dB, with a maximum EIRP of +12.3 dBm and 2D beam steering of up to 15°.

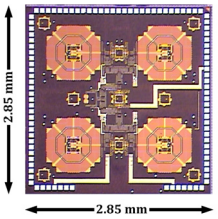

Fig. 12. Die photo of the 2x2 DPC radiator array.

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TABLE I
COMPARISON OF INTEGRATED RADIATING SOURCES IN SILICON WITHOUT EXTERNAL DIELECTRICS.

Metric	**This Work**	[1]	[2]	[3]	[4]	[5]	[6]
Polarization Control	Dynamic	Dynamic	N/A	N/A	N/A	N/A	N/A
Polarization	Linear, Circular, Elliptical	Linear, Circular, Elliptical	Circular	Linear	Linear	Circular	Circular
Maximum EIRP (dBm)	12.3	7.8	4.6	17.1	5.1	-1.9	6
Number of Elements	4	2	1	16	4	4	1
EIRP per Element* (dBm)	0.3	1.8	4.6	-6.9	-6.9	-13.9	6
Beam Steering	2D	1D	No	2D	No	2D	No
Frequency (GHz)	122.9	105.5	161	338	210	191	134.5
Process	32 nm CMOS SOI	32nm CMOS SOI	130 nm SiGe	65 nm CMOS	32nm CMOS SOI	65 nm CMOS	32 nm CMOS SOI
DC Power (mW)	1885	476	388	1540	240	77	168
Area (mm^2)	8.12	2.64	1	3.9	3.5	1.1	1.2

*EIRP per element is estimated as EIRP/(Number of Elements)^2 to account for array gain.