A 180-GHz CMOS Down-converter MMIC for Atmospheric Remote Sensing Applications

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***Abstract* — In this paper, we study the feasibility of using CMOS circuit blocks for designing future light weight, small in size atmospheric remote sensing receivers. A compact CMOS down-converter is designed which operates from 160 to 188 GHz and includes a sub-harmonically pumped I/Q resistive mixer, two IF amplifiers and a voltage controlled oscillator (VCO) with LO buffer. A measured down-conversion gain of +2.6 dB is achieved with a total dc power consumption of 152 mW using the nominal supply of +1.2 V. The measurement results show a 3 dB IF bandwidth from 1 to 5 GHz and the VCO tuning range is from 85 to 89 GHz. The designed CMOS MMIC down-converter including the probing pads occupies a silicon area of 0.575 mm^2.**

***Index Terms* — Amplifier; CMOS integrated circuit; I/Q; image-rejection; mixers; MMIC; millimeter-wave integrated circuit; remote sensing; sub-harmonic; VCO**

I. Introduction

The monolithic microwave integrated circuits (MMICs) facilitate the fabrication of low noise (temperature), miniature size, low power consumption, and light weight radiometers, such as the geostationary synthetic thinned aperture radiometer (GeoSTAR) [1], the high-altitude MMIC sounding radiometer (HAMSR) [2], and small satellites (CubeSats) [3]. Traditionally, the MMICs for these applications have been implemented by using the technologies based on compound semiconductors, such as InP and GaAs. However, latest advancement of CMOS technology has shown its potential of designing RF front-end circuits at millimeter-wave frequencies [4]-[8]. Furthermore, the recent development has made CMOS technology attractive also for non-commercial low volume applications such as the atmospheric remote sensing [9], [10]. Integrating more functions in a single CMOS chip would reduce the mass and size of the atmospheric remote sensing radiometers and small satellites. Although the gain and noise performance of CMOS technology is not competitive to its III-V counterparts, CMOS circuitry can be utilized such that the required receiver noise figure will be determined by utilizing preceding III-V low noise amplifier. Fig. 1 shows simplified block diagram of the intended low-noise, light-weight, and low-power receiver architecture suitable for atmospheric remote sensing application. Considering this receiver configuration, in this paper, we have designed a compact CMOS MMIC operating at an atmospheric channel of 183 GHz which includes a sub-harmonic I/Q mixer, a VCO with LO buffer and two IF amplifiers at the mixer's I- and Q-channels.

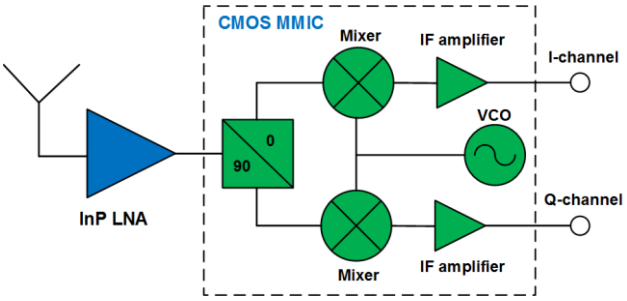

Fig. 1. Simplified block diagram of a hybrid multichip receiver architecture for future atmospheric remote sensing receivers.

II. Down-converter Design and Realization

A simplified schematic of the designed down-converter is shown in Fig. 2. Brief descriptions of each blocks of the designed down-converter are discussed in the following sub sections.

A. Mixer Design

Sub-harmonically pumped I/Q balanced resistive mixer topology is adopted for the mixer design [10]. The balanced I/Q resistive mixer consists of two singly balanced resistive mixers. The RF signal is delivered through an on-chip Lange coupler. The Lange coupler provides the essential wideband 90º phase shift with good amplitude balance [11] between the two singly balanced mixers, which is very important for the proper I/Q

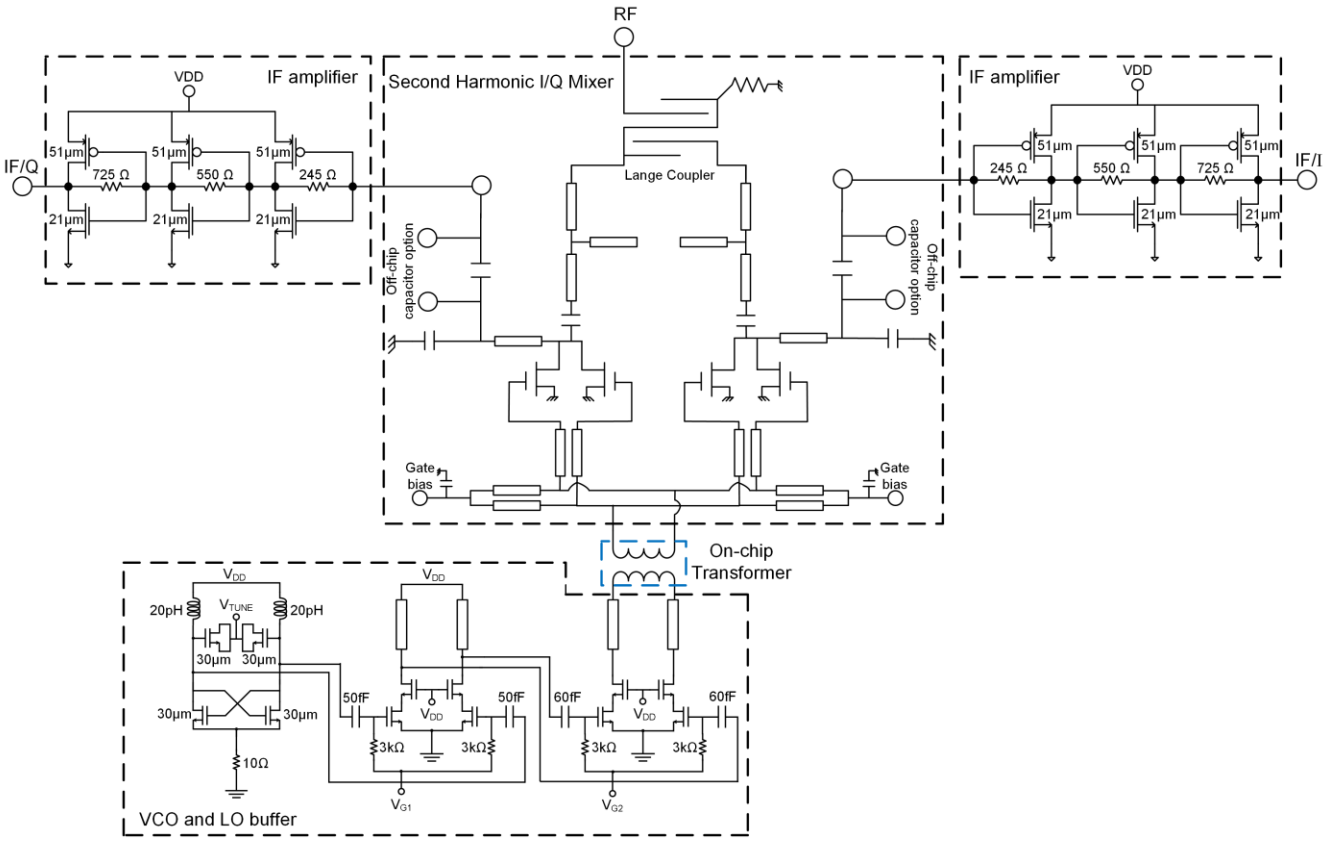

Fig. 2. Simplified schematic of the designed CMOS MMIC down-converter includes sub-harmonic I/Q mixer, VCO with LO buffer and two IF amplifiers at mixer's I- and Q-channels.

operation. The required LO signal for the mixer is provided from an on-chip VCO through a 1:1 on-chip transformer. The LO and RF matching is realized with microstrip transmission lines. Finally, the generated IF signals are extracted from the transistor drains of each unit mixers and amplified by the on-chip IF amplifiers.

B. VCO and LO Buffer Design

A differential cross-coupled LC oscillator with varactor tuning is used as the VCO to generate the required differential LO signals for the mixer's operation. The oscillator's differential tank inductor is realized with microstrip transmission lines and is implemented and modeled by the method introduced in [12] for less sensitivity to process variations and the possible errors in metal layers fabrication. The VCO is followed by two ac-coupled cascode buffer stages with 20-µm and 40-µm wide transistors, respectively, before feeding the transformer. The ac-coupling capacitors allow independent control over the gate biasing voltage of the buffer stages which allows gain control of the LO buffer chain. They also contribute to impedance matching between the stages together with the shorted transmission line stubs. The drains of the second buffer's cascode transistors are connected to VDD through the transformer.

C. IF Amplifier Design

Two identical IF amplifiers are connected at the mixer's I and Q channel through on-chip dc de-coupling capacitors. A three-stage cascade resistive feedback CMOS common-source topology is used for IF amplification. The size of the NMOS and PMOS transistors and the resistors are chosen to fulfill the gain and bandwidth requirement of the receiver.

D. Circuit Realization

A 32-nm SOI CMOS technology was used to design the CMOS down-converter MMIC. Modeling of the transistors, resistors, and capacitors are relied on *RC* parasitic extractions and electromagnetic simulations for the required accesses. The RF pad, Lange coupler and RF matching network were realized in microstrip environment. The transformer was realized by using the two top copper layers from the technology. The chip area

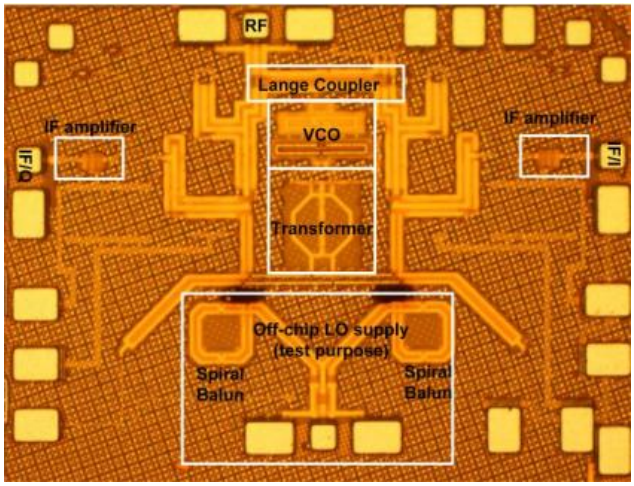

Fig. 3. Micrograph of the realized CMOS down-converter. The chip area including the probing pads is 0.575 mm^2.

including the probing pads is 0.575 mm^2. The micrograph of the designed MMIC is shown in Fig. 3.

III. Measurement Results

On-wafer large-signal measurements were carried out to characterize the designed down-converter performance. A PCB was designed to facilitate the dc connections. The RF signal was provided using a 12x multiplier chain fed from a synthesizer. The down converted IF signals were measured with a spectrum analyzer. Losses from the RF and IF probes, and the associated cables were calibrated from the measurement results. The VCO draws 65 mA current and two IF amplifiers draw 62 mA current using a 1.2 V supply. The total dc power consumption of the down-converter MMIC is 154 mW.

The designed I/Q down-converter shows a peak conversion gain of +2.6 dB with an image rejection (IR) ratio of 15 dB. The down-converted measured and simulated conversion gain of the I- and Q-channels as a function of IF frequency are shown in Fig. 4 where the LO frequency was tuned at 86 GHz. The 3 dB IF bandwidth is achieved from 1 to 5 GHz. The conversion gain is limited at lower frequencies due to the on-chip ac coupling capacitors used in between the amplifiers and IF channels (see Fig. 2) to simplify the mixer design. Even though the down-converter is not characterized in this work, the off-chip capacitors shown in Fig. 2 can be used to extend the lower frequency bandwidth.

The receiver tuning range is measured by tuning the control voltage while adjusting the IF frequency fixed at 2 GHz. The RF frequency tuning range is obtained from 172 to 180 GHz as shown in Fig. 5.

A noise simulation was also carried out and the designed CMOS MMIC shows a 30-dB noise figure. Considering preceding InP LNAs as in [1] with a combined noise figure of 3.7 dB and gain of 35 to 40 dB, the resulting receiver noise figure would be 3.9 to 4.25 dB with a gain of around 40 dB, which is better or comparable to the InP receiver demonstrated for atmospheric remote sensing application in [1].

The performance of the first cycle developed CMOS MMIC down-converter is comparable to the InP HEMT mixer [1] developed for GeoSTAR radiometer as shown in Table I. Furthermore, this developed CMOS MMIC includes integrated VCO and IF amplifiers which could significantly simplify the LO distribution system and IF amplification system of the radiometers like GeoSTAR.

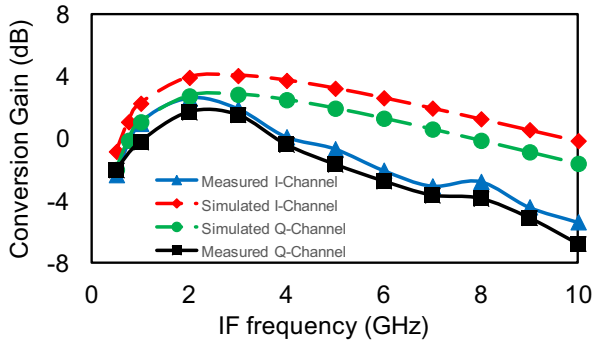

Fig. 4. Measured and simulated conversion gain of I- and Q-channels as a function of the IF frequency. The LO frequency was tuned to 86 GHz and RF frequency was swept from 172.5 to 182 GHz.

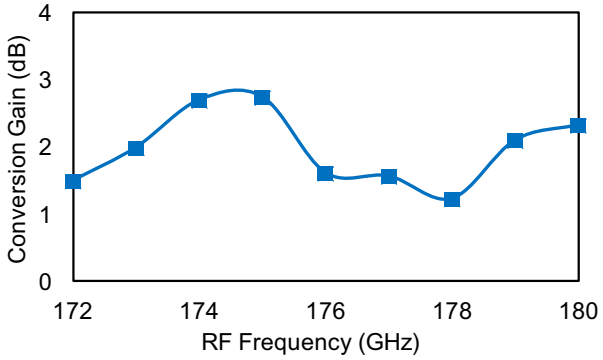

Fig. 5. Measured conversion gain at a fixed IF frequency of 2 GHz while the LO frequency was swept from 85 to 89 GHz by tuning the control voltage of the oscillator.

VII. Conclusion

In this paper, we have presented a 180-GHz CMOS down-converter MMIC which integrates an I/Q mixer, a VCO with LO buffer and two IF amplifiers. Assuming preceding

TABLE I
PERFORMANCE COMPARISON AMONG I/Q DOWN-CONVERTER MMICS FOR EARTH REMOTE SENSING

Ref.	Tech.	Integration level	RF freq. (GHz)	IF bandwidth (GHz)	CG (dB)	IR ratio (dB)
This work	32-nm SOI CMOS	Mixer + VCO + IF amps	160-188	1-5	2.6	>15
[1]	35-nm InP	Mixer	165-183	0.01-0.5	-21*	>20
[10]	32-nm SOI CMOS	Mixer + IF amps	158-182	1-10	8	>20

*Estimated

high gain, low noise InP HEMT amplifiers, the performance of the designed CMOS down-converter MMIC demonstrates the potential of the CMOS technology for achieving high level of integration for future small sized atmospheric remote sensing receivers and small satellites. Our future work includes the phase-locking of the VCO and packaging of the InP and CMOS chips into a hybrid multichip waveguide module.

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