26.3 A 69-to-79GHz CMOS Multiport PA/Radiator with +35.7dBm CW EIRP and Integrated PLL

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Low-cost mm-wave silicon integrated signal generation and processing enable many applications, such as silicon-based automotive radars for self-driving cars and wireless communications. Some challenges encountered in commercialization of such systems are the high packaging and testing costs and high sensitivity to antenna parameters, which can diminish the advantage of integrated silicon solutions. On-chip antennas have been proposed as a solution to reduce the packaging costs [1,2]. Link budget analysis of systems (e.g., radar) necessitates high-power (high EIRP) transmitters while system resolution analysis suggests higher frequency of operation for better spatial resolution. The scaling of CMOS transistors facilitates the latter requirement, but, unfortunately, the lower breakdown voltage of the transistors reduces their maximum power handling capabilities at a given radiator impedance. Several approaches have already been implemented to address this issue, each with its own shortcoming. Power-combining multiple PA outputs with passive on-chip power combiners [3] adds extra loss and reduces the overall efficiency, spatial power combining using phased arrays [4] consumes a large die area. Power combining at the antenna [5,6] has been proposed as an approach to address these challenges. In this paper, we propose a spatial PA/radiator power combining approach with optimal PA-load design using strongly coupled antennas in close proximity. This approach utilizes techniques of power combining in free space resulting in favorable drive-point impedance design and using on-chip PAs and radiators to achieve high radiated output power.

Figure 26.3.1 shows the concept of the proposed strongly coupled radiator and its associate impedance scaling. A single slot antenna has a radiation impedance of around 520Ω and thus only radiates around 1mW if driven with a 1V swing. If a second strongly coupled slot in close proximity to the first one is driven in phase, the total radiated power increases fourfold; similarly, three slots radiate 9mW, and the quadratic trend holds up for slots placed in such fashion so long as the overall dimension is smaller than roughly one wavelength. The quadratic increase in radiated power is due to the simultaneous reduction of the drive-point impedance and the increased number of the power sources. The addition of a strongly coupled slot radiator increases the total radiated power not only by increasing the number of power sources but also by increasing the radiated power of each slot through lowering the drive-point impedance. Unlike previous spatial power-combining methods, the proposed array of slots does not significantly change the radiation pattern compared to a single-element antenna.

We implemented a 16-element slot array of the proposed radiator in the top aluminum layer of a 65nm bulk CMOS process. Figure 26.3.2 shows the dimensions of the implemented radiator as well as the topology of 8 PAs and their transistor sizing. Each PA is a pseudo-differential cascode stage with a 24pH shunt inductor to resonate the parasitic capacitance of the cascode node and drives two slots by utilizing a virtual ground between them, as shown Fig. 26.3.2. By properly designing the slot length, we are able to completely absorb the parasitic capacitance of the PA output node into the antenna structure. The antenna also provides the DC power to the PA, eliminating the need for RF chokes and improving the PA efficiency. All the PAs are driven in-phase through a differential 77GHz binary-tree clock-distribution network.

To allow for FMCW operation, a PLL with a multiplication ratio of 32 was implemented to generate a 10GHz BW chirp using a synthesized 2.156-to-2.469GHz reference signal. The block diagram of the PLL is shown in Fig. 26.3.3. The closed loop BW of the PLL is higher than 20MHz, allowing fast chirp rates. The VCO has a tuning range of 67.9 to 80.6GHz, while the PLL locking range was 69 to 79GHz. The measured phase noise of the PLL is -96.4dBc/Hz at 1MHz offset. This is obtained by downconverting the radiated power using the 5th harmonic of PMP MOD-WM harmonic mixer.

Electromagnetic simulations indicate that the radiation efficiency of the radiator can be improved from 46% to 52% by using a low-cost 6.35mm diameter alumina hemispherical lens, which increases the directivity of the antenna from 5 to 10dBi and also improves heat dissipation. Full 3D pattern measurements of the radiator with the lens were performed over the full frequency span from which the directivity of the radiator was obtained. Figure 26.3.4 shows the highlights of these measurements.

The EIRP of the radiator at broad side was measured using Agilent V8486A and W8486A power sensors with 15dBi WR-15 and 25dBi WR-12 standard horns, respectively. The calculated gain of the horn antennas vs. frequency [7] matches the datasheet at provided frequency points. Total radiated power (TRP) was calculated from the measured EIRP and measured radiator directivity. The PA efficiency and total output power can be calculated from TRP and the simulated antenna efficiency. Figure 26.3.5 shows these measurement results. The radiator achieves a peak EIRP of +35.7dBm at 71.25GHz when running continuously from a V_{DD}=1.8V supply and consumes 1006mA of current. The measurements correspond to a maximum TRP of +24.4dBm with a peak directivity of 12.2dBi. The combined PA peak output power is +27.4dBm with a drain efficiency of 30.8%. Simulations indicate that the output power varies by less than 20% across the PAs due to presence of edge effects in the structure.

A comparison table provided in Fig. 26.3.6 summarizes the results of this work and compares them against other works.

Acknowledgment:
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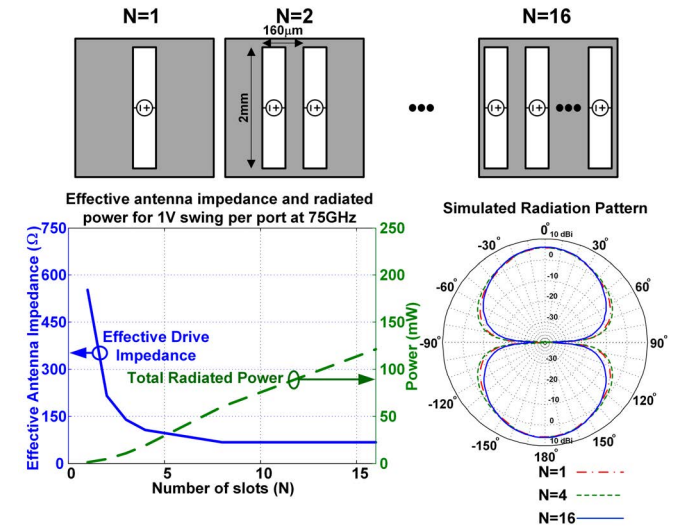

Figure 26.3.1: Impedance- and radiated-power scaling of tightly coupled slot array antennas.

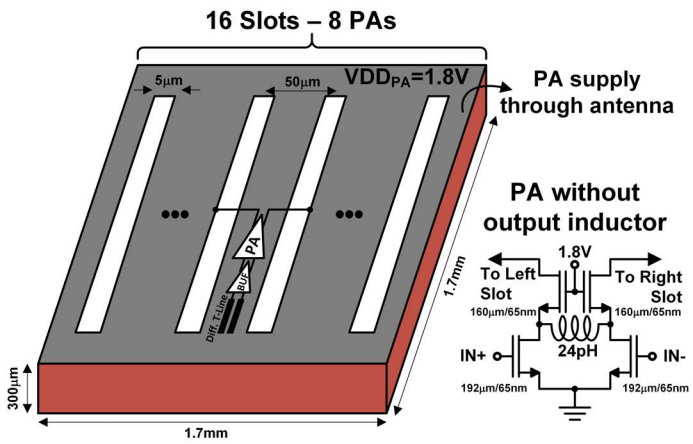

Figure 26.3.2: Eight differential cascode PAs drive 16 slots. The radiator is designed to absorb the parasitic capacitance of PA output.

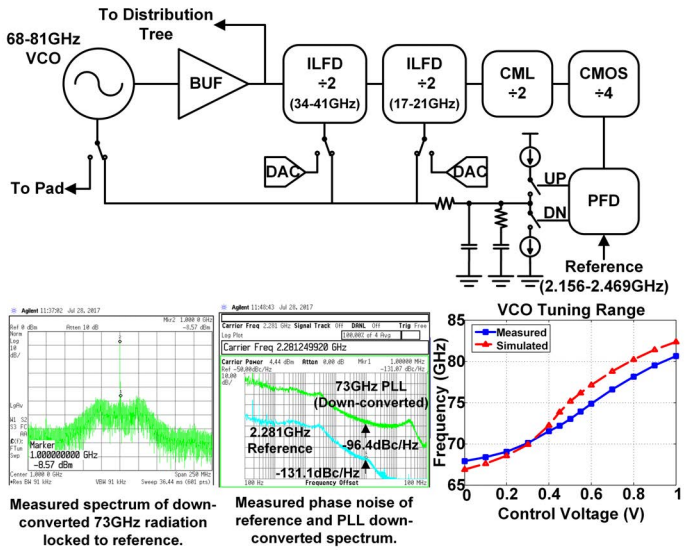

Figure 26.3.3: PLL block diagram and measurement results.

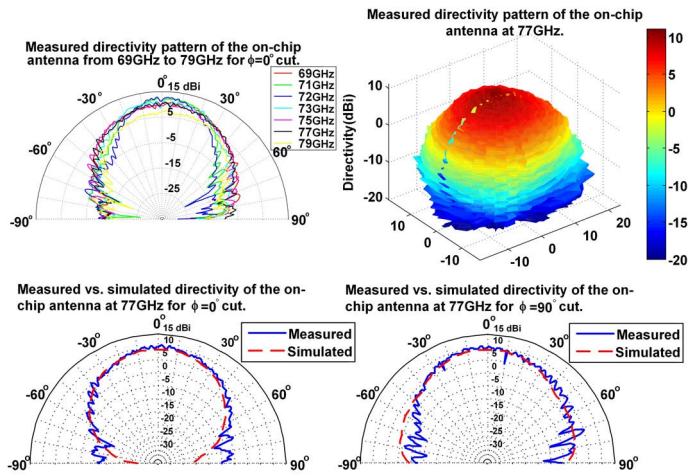

Figure 26.3.4: Measured and simulated radiation pattern of the radiator.

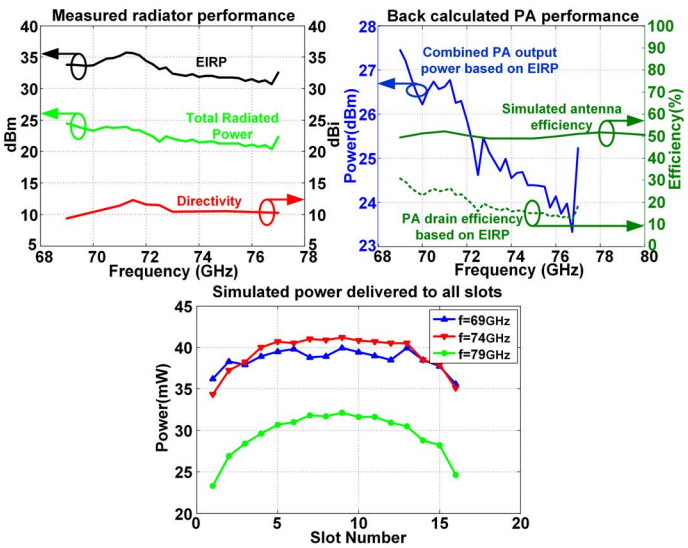

Figure 26.3.5: Radiator and PA performance.

	This Work	[1]	[4]	[6]	[8]	[9]
Process	**65nm CMOS**	32nm SOI	180nm SiGe	45nm SOI	32nm SOI	65nm CMOS
Frequency(GHz)	**69-79**	134.5	108-114	53-63	58.3-60.5	88-99
EIRP(dBm)	**35.7**	6.0	24.5	33.1	17.1	35
On Chip Antenna	**YES**	YES	NO	YES	NO	NO
Radiator Directivity (dB)	**12.2**	7.1	17	6.9	32.5	36 (Dish Ant.)
Tot. Rad. Power (dBm)	**24.4**	-1.3	7.5	26.2	N/A	0
Antenna Efficiency	**52%**	39%	45%	74.5% (Uses High Res. Sub.)	N/A	N/A
PA P_{sat}(dBm)	**27.4**	N/A	11	27.9	N/A	N/A
PA Efficiency	**30.8% (Drain Eff.)**	N/A	N/A	23.4% (PAE)	N/A	N/A
Phase Noise (dBc/Hz)	**-96.4@1MHz**	N/A	N/A	N/A	-113 @10MHz	-85.6 @1MHz
Total DC Power(W)	**PA+PLL/Distrib 1.81+0.55=2.36**	0.17	3.4	N/A	0.23	0.6
Chip Area(mm^2)	**2.9**	1.2	39	10.5	9 (RX+TX)	4.32 (RX+TX)

Figure 26.3.6: Comparison with other works.

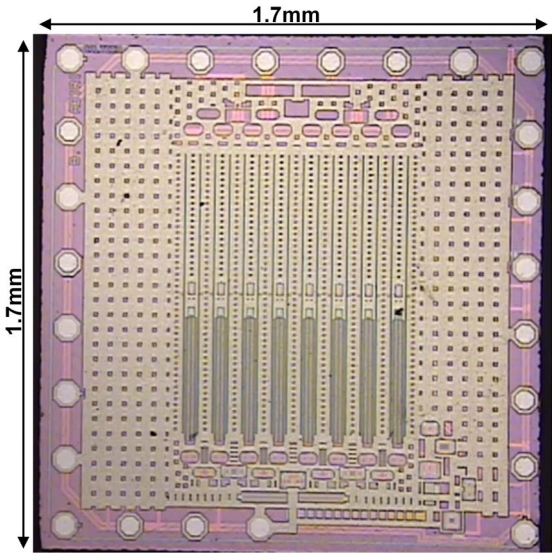

Figure 26.3.7: Die micrograph.

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