

# An Adjustable Self-Equalizing Photo Detector

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**Abstract:** An optically-wideband adjustable self-equalizing photo-detector (ASEPD), capable of reviving eye closure due to limited bandwidth of electro-optical components in an optical link, is presented. The ASEPD enables use of various slower electro-optical components in faster data links.

**OCIS codes:** (130.0130) Integrated optics; (250.5300) Photonic integrated circuits (040.5160) Photodetectors; (130.3120) Integrated optics devices; (250.3140) Integrated optoelectronic circuits; (250.4745) Optical processing devices;

## 1. Introduction

The proliferation of high bandwidth applications such as instant video has resulted in high demand for faster data communication. Copper based communication channels are being replaced with superior optical fiber channels that provide more available bandwidth. As a result, the communication speed bottleneck is moving from communication channel to the electro-optical interfaces. Equalization, a widely used technique to compensate copper channel bandwidth limitation, is also used to mitigate the limited bandwidth of electro-optical components [1]. While integrated electronic circuits have become orders of magnitude faster since their invention, they are facing difficulties keeping up with the necessary bandwidth for equalization, as electro-optical components improve. In this paper, we demonstrate an adjustable self-equalizing photo-diode that substantially improves the incoming optical signal directly before entering the electronic IC that recovers the data through a hybrid electro-optical solution. The presented ASEPD is optically wideband, hence it does not need to be retuned for different optical channels in a WDM system. Unlike the previously reported self-equalizing PD [2], this design provides the ability to adjust the equalization profile and level, thereby making it a versatile PD that can be used in different optical communication channels with different optical modulators, data rates, and TIA bandwidths.

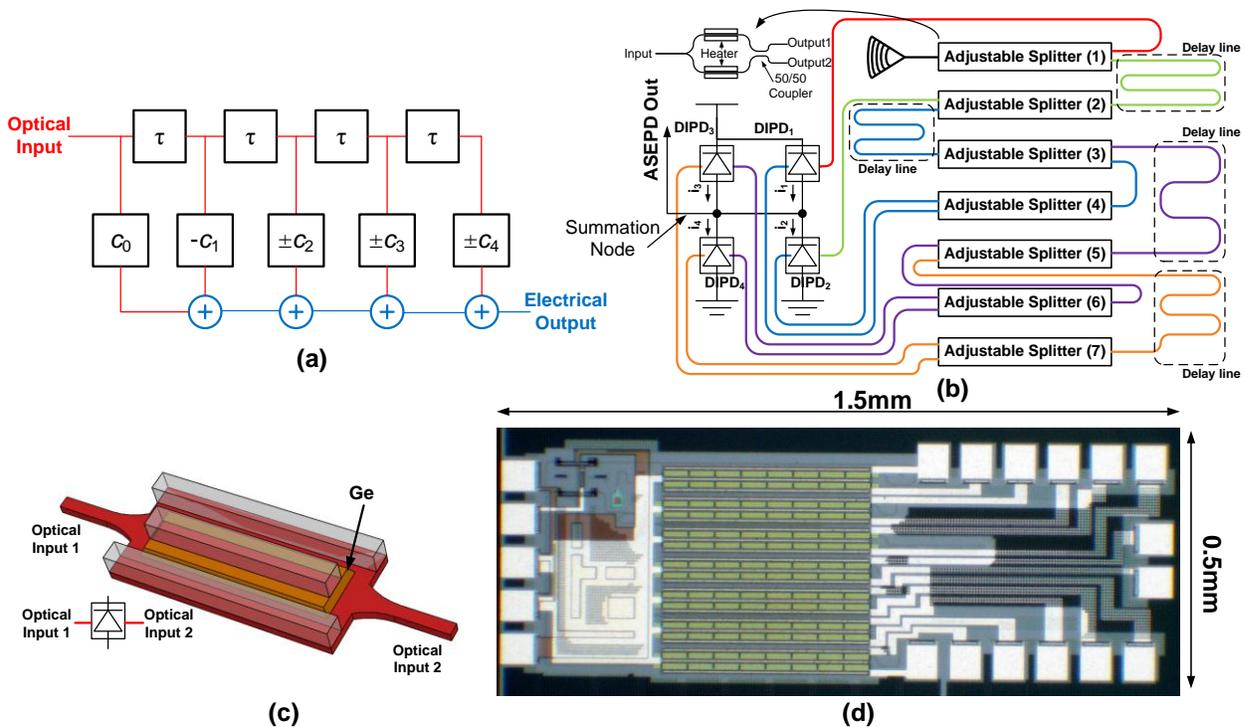


Figure 1. (a) Block diagram of the adjustable self-equalizing PD (ASEPD) and (b) its layout floor-plan. (c) Dual-input SiGe PD. (d) Photo of the fabricated chip

## 2. Design and Fabrication

In order to create a versatile ASEPD, a general 4-tap feed-forward equalizer (FFE) with 30ps tap delays was chosen to provide equalization in the PD. In order to provide more flexibility to the equalization of the optical signal, the second, third, and fourth tap of the FFE were designed with selectable signs [3]. This improves versatility of the equalizer, allowing more complex frequency responses.

Figure 1(a) shows the conceptual block diagram of the equalization that is performed in the ASEPD. Part of the light coupled to the chip is allocated for the main tap,  $c_0$ , and the rest of the light power is passed through a  $\tau=30$ ps delay line, after which a portion of light is allocated for the second tap,  $c_1$ . The second tap is subtracted from the main tap, hence providing a peaking in the frequency response at around 16GHz. The remaining portion of the light goes through additional delays where, after each delay, part of the light is set aside and is added to or subtracted from the output. In our design, the addition and subtraction of signals are done in current mode in the electrical domain; hence these operations are not dependent on the phase of the optical signal and are thus optically wideband. The subtraction or addition of the current allows either having peaking or notches at lower frequencies; as a result, it is possible to adjust the response of the ASEPD based on the channel.

Figure 1(b) shows the implementation of the ASEPD. It includes a grating coupler for coupling light from optical fiber into the silicon photonics chip and a chain of adjustable splitters and delay lines that couple light into dual-input photo-detectors (DIPD), where the summation is done in electrical domain. The adjustable splitters in this design utilize thermally tuned MZIs with a 50/50 coupler at the output [4]. By tuning the phase of the arms of the MZI, it is possible to vary the intensity of light that comes out of each of the output ports. In our design, the adjustable splitters are used to adjust the value and sign of tap weights, whereas the DIPDs perform addition/subtraction in current domain as well as opto-electric conversion in a compact form. The DIPD, as shown in Fig 1(c) is a vertical SiGe PD with two optical inputs. Connecting two inputs to a single photo diode results in fewer number of photo-diodes and hence the total capacitance on the output node is reduced. In order to reduce the output junction node capacitance further, the sizes of DIPDs connected to higher order taps are reduced. Although smaller DIPDs have smaller responsivity, the higher order tap coefficients are generally smaller and less effective in opening the eye than reducing the output node capacitance of the ASEPD.

Fig 1(d) shows a photograph of the chip designed in IME SOI process with 220nm silicon layer and a Ge epitaxial layer for photo-detectors [5]. The chip occupies an area of  $1.5 \times 0.5 \text{mm}^2$  including all pads and electrical connections.

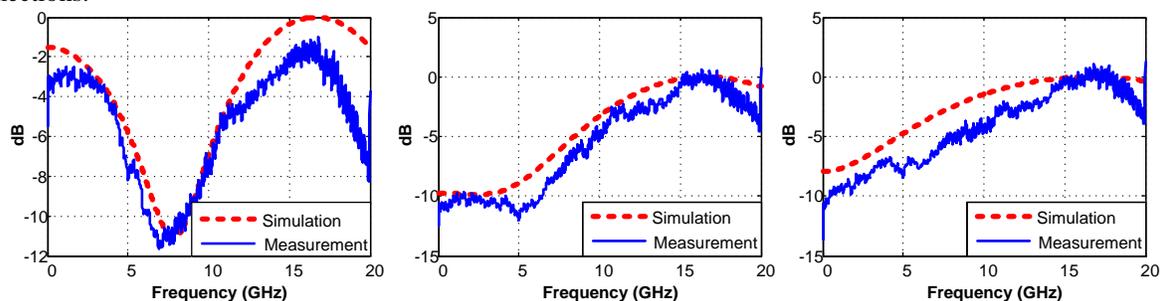


Figure 2. Examples of filter responses that can be generated with ASEPD

## 3. Measurement Results

We measured the frequency response of the ASEPD for different tap settings. Figure 2 shows examples of different frequency responses that can be achieved with different tap coefficient adjustments. The ideal FIR filter response is shown on each graph for comparison. The faster roll off of ASEPD at around 18GHz is due to the limited bandwidth of the DIPDs used in this design. The frequency response of the ASEPD is characterized by de-embedding the frequency response of the modulator and cables used in our test setup.

Figure 3 shows the ability of the ASEPD to open an otherwise closed eye at 25Gbps. A 12.5Gbps optical modulator was used to modulate the optical signal from a DFB laser at 25Gbps. When a 35GHz bandwidth PD is used in the receiver, the eye will be closed as shown in Figure 3(a). By using ASEPD and turning on the equalization the eye diagram opens (Figure 3(b)) making it possible to use a lower speed modulator at higher data rate. The ASEPD was also tested with a different channel at a different bit rate. Fig. 4 shows the un-equalized eye diagram at 12.5Gbps. A 4-inch FR4 trace was used prior to the 12.5Gbps modulator in order to emulate a different channel and provide attenuation. After adjusting the tap coefficients, the eye becomes open again. Figure 5 shows the test setup and BER versus input optical power for 12Gbps for both cases when the equalizer is on and off. The ASEPD with adjusted tap coefficients achieves BER better than  $10^{-13}$ .

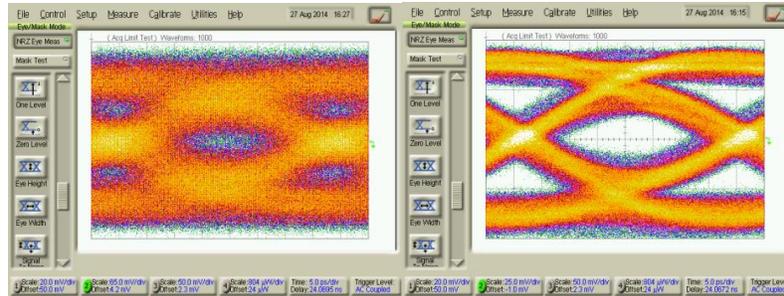


Figure 3. Operation of EQ at 25Gbps. (a) With a discrete 35GHz PD (b) with ASEPD (equalizer on)

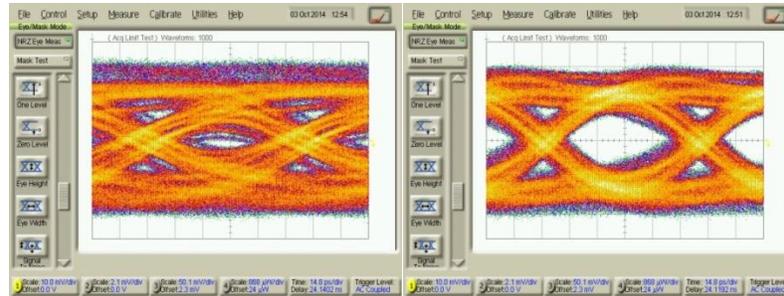


Figure 4. Operation at 12.5Gbps with 4" FR4 trace with (a) Equalization off and (b) Equalization on

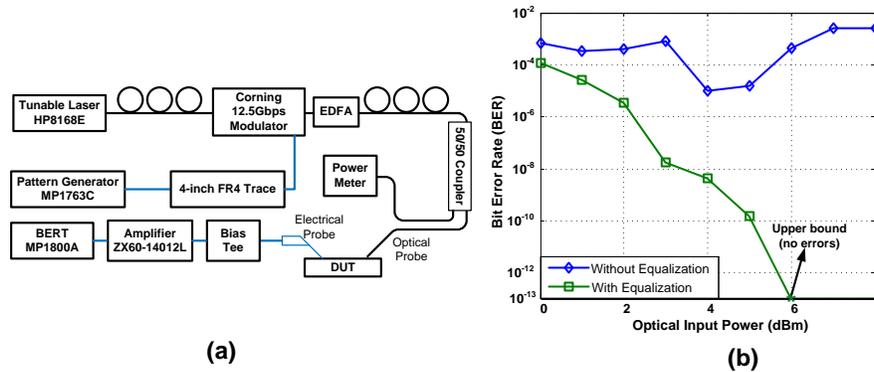


Figure 5. (a) Test Setup and (b) measured BER vs. input power with and without the equalization for 12Gbps PRBS7

**4. Conclusion**

An adjustable self-equalizing photo detector capable of equalizing 25Gbps signals was demonstrated. The proposed ASEPD utilizes on-chip silicon waveguides for delays and MZI-based thermally tunable splitters to adjust the tap coefficients. To achieve wide optical bandwidth, the summation is done in current mode in electrical domain through use of four dual-input photo-detectors.

**5. Acknowledgement**

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