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Binary particle swarm optimized 2 × 2 power splitters in a standard foundry silicon photonic platform

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Compact power splitters designed *ab initio* using binary particle swarm optimization in a 2D mesh for a standard foundry silicon photonic platform are studied. Designs with a 4.8 μm × 4.8 μm footprint composed of 200 nm × 200 nm and 100 nm × 100 nm cells are demonstrated. Despite not respecting design rules, the design with the smaller cells had lower insertion losses and broader bandwidth and showed consistent behavior across the wafer. Deviations between design and experiments point to the need for further investigations of the minimum feature dimensions. © 2016 Optical Society of America

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Foundry fabricated silicon (Si) photonics seek to implement highly sophisticated photonic integrated circuits (PICs) at low cost by using the mature manufacturing process of microelectronics [1–3]. The high refractive index contrast in Si photonic platforms not only allows for compact device footprints but also makes possible device concepts that can take advantage of the strong optical confinement and scattering (e.g., grating couplers, micro-resonators, photonic crystals) [4–6]. The growing availability of foundry Si photonics, in combination with expanded computation capabilities for detailed electromagnetic simulations, open the opportunity to explore device designs that cannot be implemented in traditional, lower index contrast PIC platforms such as silica and compound semiconductors and are yet volume manufacturable.

Device design performed by topology optimization without any *a priori* assumptions on the geometry has recently generated much interest [7–10]. As opposed to conventional design methodologies in which a few critical geometric parameters are tuned on a fixed geometry, topology optimization can find unexpected solutions with good performance within demanding constraints by exploring much larger parameter spaces. An example is the polarization beam splitter of [9], which had a design footprint constraint of 2.4 μm × 2.4 μm. However, usual optimization approaches (e.g., in [8–10]) rely on high-resolution rendering of intricate geometric features, such as through electron-beam lithography, which can result in designs that are incompatible with the design rules and minimum feature sizes in foundry processes, which use deep ultraviolet (DUV) photolithography.

In this Letter, we investigate foundry fabrication of an optimization designed 2 × 2 3 dB power splitter. Power splitters are a common building block in PICs and, in Si photonic platforms, are typically implemented as multimode interference (MMI) couplers, directional couplers, and adiabatic couplers. Typical footprints in a standard Si photonic platform have footprints around 39 μm × 5.2 μm for a 3 dB directional coupler and 158 μm × 4.1 μm for an MMI coupler [11]. Because power splitters may be instantiated many times in a PIC, a size reduction of the 2 × 2 splitter can save substantial circuit area. Here, we explore the design and implementation of 2 × 2 power splitters with a footprint constraint of 4.8 μm × 4.8 μm designed through optimization that accounted for the minimum feature size of the foundry process. We will first briefly describe the Si photonic platform and the optimization problem setup. Two device variants and their measurements are presented, followed by discussions on directions for improvement.

The designs to be described were implemented in the A*STAR IME Baseline Silicon photonics platform [12,13], which provides a 220 nm thick silicon layer with a 2.1 μm top oxide cladding and a 2 μm buried oxide, and partial etches for rib waveguides and grating couplers. The process uses 248 nm DUV photolithography on 8 in. (20.32 cm) silicon-on-insulator (SOI) wafers. The 2 × 2 power splitter is designed for the fully etched 220 nm thick Si layer. To impose the symmetry expected of a 2 × 2 3 dB power splitter, the design region is a quadrant of the device with a feed waveguide, which is reflected horizontally and vertically to constitute the complete device with four ports, as illustrated in Fig. 1(a). A square mesh is applied on the design region, and a binary variable is assigned to each square mesh cell to indicate the presence of Si or SiO_2 in the cell. This parameterization of the design region is commonly used in structural optimization [14,15] and also has been applied

to electromagnetic design problems [7,9,16]. Because the smallest feature in such a design will be a single cell, we use the heuristic of taking the cell side length to be the minimum manufacturable feature/spacing size. The platform had design rules similar to [4], which had a nominal minimum feature size of 180 nm. Therefore, we first chose to optimize based on using a mesh composed of cells with a size of 200 nm × 200 nm to satisfy design rules.

We used the binary particle-swarm optimization (BPSO) algorithm [17] to optimize the binary-valued configurations of the cells. The particle swarm is transformed from a continuous configuration space to a discrete configuration space through treating each binary variable as a dimension and applying thresholding. BPSO was chosen for its ease of implementation and for its reported applicability to similar problems [18–20]. To design the device, we used BPSO to optimize the figure of merit:

$$f(x) = \min\{P_1(x, 1550\ \text{nm}), P_2(x, 1550\ \text{nm})\}, \quad \textbf{(1)}$$

where x is the configuration of cells of the design and $P_1(x, \lambda)$ and $P_2(x, \lambda)$ are the transmitted power in the fundamental mode of the transverse electric polarization (TE0) at the output ports, OUT1 and OUT2, for a TE0 input at IN2 for a given configuration and wavelength, λ. This is shown in Fig. 1(a). Equation (1) heuristically encourages 3 dB power splitting and minimization of the insertion loss by improving the worse performing output. Each evaluation of the objective function entailed a 3D finite-difference time-domain (FDTD) simulation of the design. An FDTD simulation mesh size of 50 nm × 50 nm × 40 nm with a power cutoff condition of 0.001% of initial power was used. As a compromise between the size of the configuration space and tractability of the simulations, we constrained the optimization to a 4.8 μm × 4.8 μm area, using 12 × 12 cells. Each iteration required approximately 10 s on an Intel i7-3770 CPU computer with 16 GB of RAM.

The design for 200 nm cells was optimized based on an initial population of 21 using three repetitions of the heuristic configurations in Fig. 1(b) with randomized velocities and run over 500 iterations. Figure 2(a) shows the convergence to a figure of merit value of 0.174, and the resulting design is shown in Fig. 2(b). The transmission spectrum of the simulated device in Fig. 2(c) shows a wavelength-dependent splitting ratio, crossing over at 1531 nm with insertion loss

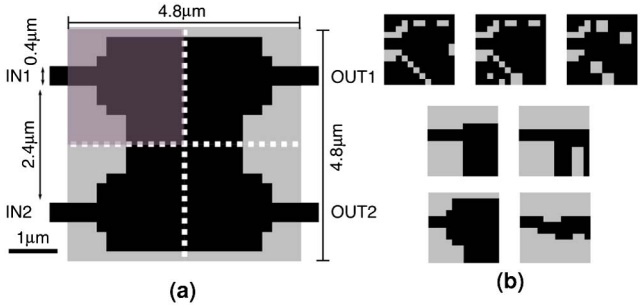

Fig. 1. (a) Schematic of the design problem. The design area (highlighted, top left) is reflected vertically and horizontally along the dotted white lines along with an input port. Black and gray cells represent the presence and absence of material, respectively. In FDTD simulations, a TE0 mode is launched into IN2, and the TE0 mode power is monitored at OUT1 and OUT2. (b) Initial configurations for the optimization of the 200 nm cell design. The initial population is based on these shapes with randomly initialized particle swarm velocity.

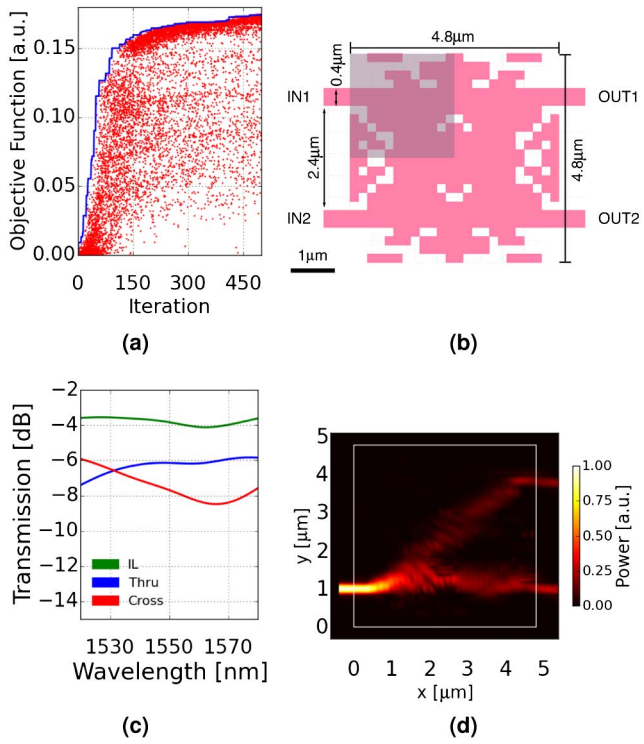

Fig. 2. (a) Figure of merit at each iteration for the device with the 200 nm cells. Red dots are the individual values, and the blue line is the best value obtained by that iteration. (b) The device design with the highest figure of merit value of 0.174. (c) Simulated transmission and loss spectra of (b). (d) Normalized intensity profile of the device.

of 3.56 dB and worst insertion loss of 4.11 dB. The optimization resulted in a design with an unconventional geometry, confined within the 4.8 μm × 4.8 μm design region. The normalized power profile in Fig. 2(d) shows that the device did not operate as purely as an MMI or a directional coupler. This design is highly compact because extra bend-in waveguides are not needed due to the large spacing between the input ports.

This design was implemented in the A*STAR IME Baseline Si photonics process, with the input/output ports connected to a row of TE grating couplers for coupling out of chip with a fiber array with an 8° angle polish. An additional pair of grating couplers connected with a waveguide was included in the row to optimize the fiber-to-chip alignment. A swept tunable laser and optical power monitor were used for spectral measurements. The measured spectra [Fig. 3(a)] show a symmetric response as expected from the symmetry of the device. Figure 3(b) shows the spectra of a few devices from across the wafer were similar, confirming inter-die fabrication reproducibility.

However, these measurements greatly differed from the simulation, with insertion loss now at best around 6 dB and less balanced power splitting. To determine the cause of the discrepancy, we obtained the scanning electron micrographs (SEMs) of the fabricated devices, as shown in Fig. 3(c), by partially etching away the SiO_2 cladding layer in a hydrofluoric acid solution. We imaged with backscattered electrons to view the features under the residual SiO_2. The SEMs revealed that many of the smaller isolated features in the nominal design were absent and the features were rounded. Although the rounding was expected [21], it was unanticipated that the

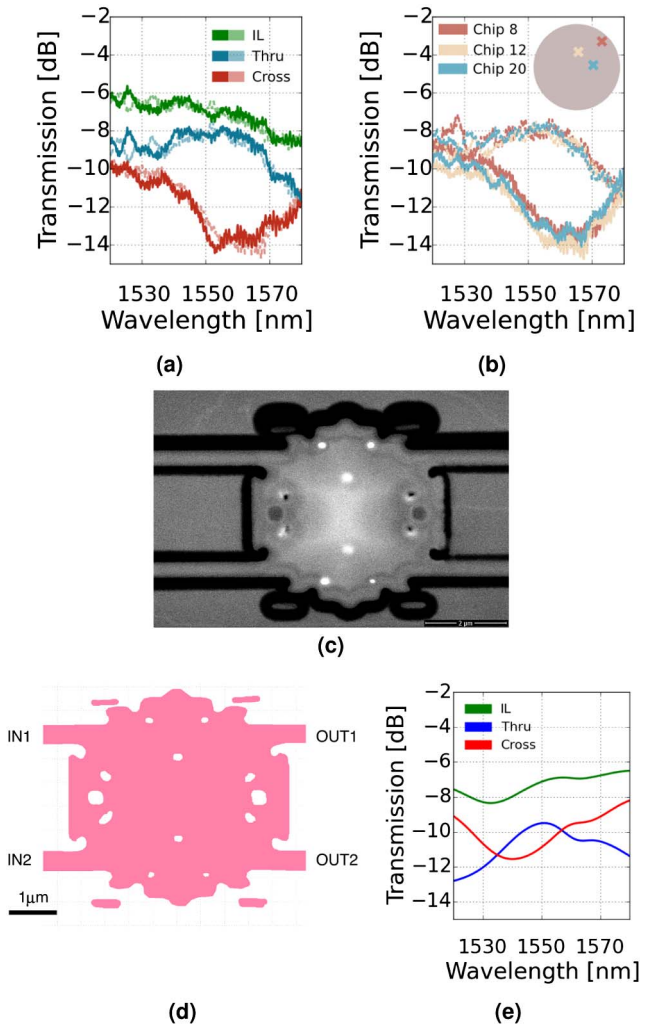

Fig. 3. (a) Measured through (blue) and cross (red) port transmission spectra and the insertion loss of the 200 nm cell device for input from IN1 (solid) and IN2 (faded, dashed). (b) Measured spectra from several devices from across the wafer. The die locations are shown in the inset wafer map. (c) Backscattered electron SEM of the device with most of the cladding removed. (d) Trace of (c) used for FDTD simulations. (e) Simulated transmission spectrum based on (d).

smaller features would be absent because the minimum feature size design rule was nominally satisfied.

To simulate the expected transmission of the fabricated device, we traced the SEM as in Fig. 3(d) and imported a 220 nm thick Si with the corresponding planar geometry into a 3D FDTD simulation. The computed transmission is plotted in Fig. 3(e). Insertion losses were closer to that of measurements, but the disparity between simulated and measured transmission persisted, suggesting that other manufacturing nonidealities, such as sloped side walls or partial etching, were present. In our measurements, light, which is converted into the transverse magnetic (TM) polarization (due to sloped side walls), would have been filtered out by the TE grating couplers.

We also implemented a second design using 100 nm × 100 nm cells, which are smaller than the allowed minimum feature size of the foundry process. The design was a variant of the 200 nm cell design and used 24 × 24 cells. The design was developed through BPSO with an initial population size of 10 initialized to the nominal 200 nm cell design with random velocities and run over 478 iterations. Convergence is shown in Fig. 4(a), with improvement of the figure of merit from 0.174 to 0.223. The design is shown in Fig. 4(b). The simulated transmission spectrum [Fig. 4(c)] shows a more constant power splitting ratio without a crossover point with a lower worst case insertion loss of 2.9 dB than the 200 nm cell design.

Measurements in Fig. 5(a) show that the splitter had improved insertion loss and power splitting behavior compared with the measurement results of the 200 nm design. Although the spectra did not match the simulation, the cross port received power comparable with the through port, and an equal power splitting ratio was obtained at wavelengths of 1535 and 1560 nm. Worst insertion loss was around 3.5 dB.

The SEM of the fabricated device [Fig. 5(c)] is similar to the 200 nm cell device but has larger openings in the holes, which were enlarged during the optimization. This suggests that having a refinement in the mesh is useful for improving performance by allowing the boundaries of larger features to be re-positioned and not be constrained by the original mesh grid, even if the smaller features are not fabricated. Thus, in future designs, if small features could be filtered out of the design during the optimization, such as with filters proposed in [22], a minimum feature size may not necessarily need to be linked with the mesh size, and having a larger problem space to work with may improve designs.

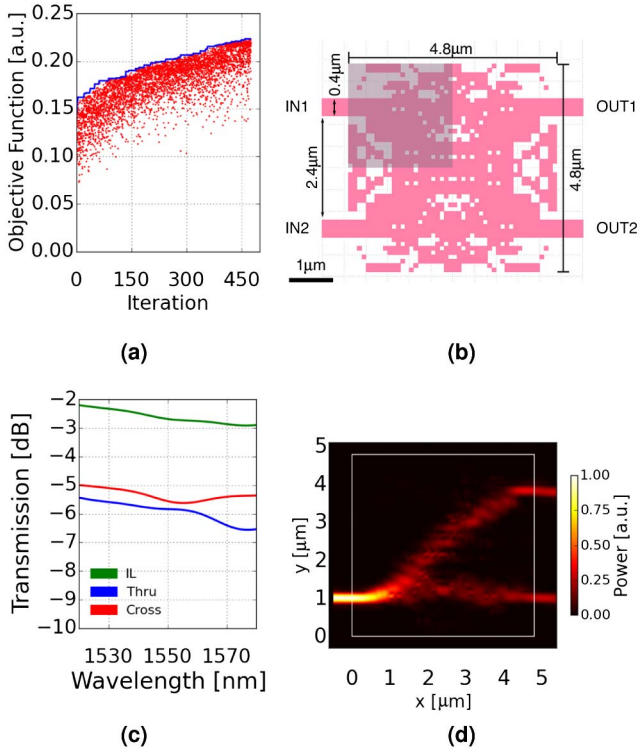

Fig. 4. (a) Plot of the figure of merit at each iteration for the 100 nm cell device. Red dots are the individual values, and the blue line is the best value at each iteration. (b) Device with the best figure merit of 0.223. (c) Simulated transmission and insertion loss (IL) spectra of (b). Insertion loss is calculated as the sum of transmitted powers of the two arms with respect to input power. (d) Normalized intensity profile of the device.

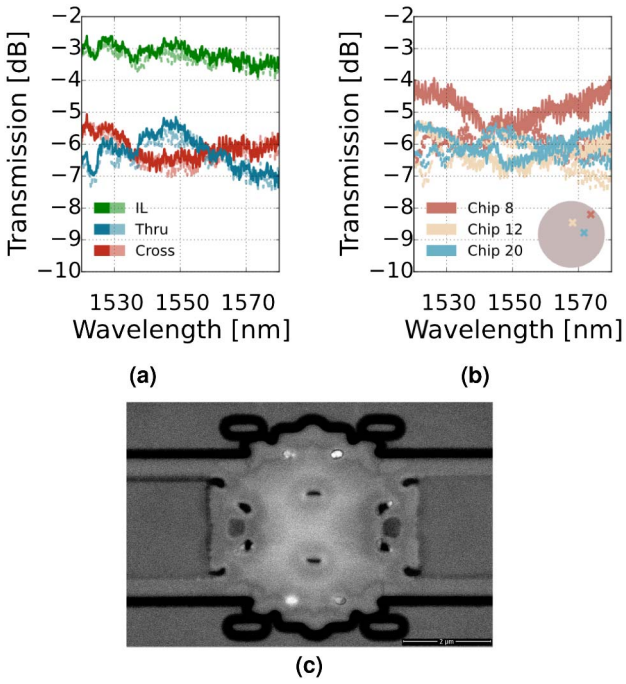

Fig. 5. (a) Measured through (blue) and cross (red) port transmission, and insertion loss (green) of the 100 nm cell device for input from IN1 (solid) and IN2 (faded, dashed). (b) Measured through and cross port spectra from a few dies across the wafer. The die locations are indicated in the inset wafer map. (c) Backscattered electron SEM of the fabricated device with most of the oxide cladding removed.

Our work highlights directions for improving *ab initio* optimized photonic devices in foundry platforms. First, the devices have impractically high insertion losses compared with conventional devices, which are on the order of 0.01 dB for directional couplers and 0.1 dB for MMIs [11]. It is possible that there is no physical mechanism to perform the power splitting within the imposed area constraint. Thus, rather than fixing an area for the optimization, one may start with a conventional design and explore the optimal trade-off between insertion loss and device footprint through a multiobjective optimization [23]. In addition to device footprint, the multiobjective approach in general can be used to incorporate other significant performance parameters, such as the splitting imbalance between the arms, which need to be considered for practical devices. Second, to address the problem that using cells slightly above the minimum allowable feature size was insufficient to guarantee manufacturability, further studies on the minimum cell size are needed. In conventional devices, the minimum feature size is usually applicable to edges along one dimension, for waveguide gaps, tapers, and gratings. However, the optimization-based device has features that approach the minimum feature size in two dimensions. In particular alternating patterns and isolated features were problematic. Systematic characterization of worst case 2D patterns, such as checkerboards and isolated cells, can provide better guidelines to inform minimum cell size. Incorporating this information into the optimization through lithography simulation [21] can help avoid problematic features. Also, transformations to the device mask to compensate for lithography effects, as in [24], can enable more accurate fabrication when small features are needed.

In conclusion, we have presented the first foundry Si photonic 2 × 2 power splitters designed by binary particle swarm optimization of a design area of 4.8 μm × 4.8 μm parameterized by square cells that have sizes chosen according to design rules. Power splitting is demonstrated, but to reduce the insertion loss and to have a better match with the design, multiobjective optimization, deeper studies of the 2D minimum feature size, and lithography simulations can be incorporated into future work.

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