Multi-beam, Scalable 28 GHz Relay Array with Frequency and Spatial Division Multiple Access Using Passive, High-Order N-Path Filters

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Abstract — A 28 GHz scalable relay array that independently re-routes multiple beamformed data-channels in different frequency bands is presented, allowing for frequency and spatial division multiple access. The array is implemented at the element-level with a 65 nm CMOS RFIC that has two transmit-and-receive branches. Each transmit-and-receive branch provides phase delay, true time delay, and amplitude control for up to 3 frequency channels independently and simultaneously. The baseband signal chain is enabled by a dual function N-path filter architecture that is passive and inductorless yet provides high-order filtering with complex roll-off and performs phase shifting. The resulting array consists of a 2-chip, 4-branch prototype that independently steers 3 frequency multiplexed incident data beams into different spatial directions, with true time delay control in each beam. A radiative measurement shows the router supporting a simultaneous throughput of 625 Mb/s 32-QAM data across 3 frequency channels that are independently spatially steered.

Keywords — scalable router, 5G, multi-beam, N-path filter.

I. INTRODUCTION

The trend towards mm-wave and higher frequencies is continuing through and beyond the deployment of 5G networks. While offering high bandwidth channels, their line-of-sight behavior due to higher absorption hampers their use in indoor and urban environments. To extend the range and improve the versatility of communication networks at these frequencies, several signal re-routing systems have been proposed [1][2]. These systems are arrays which receive an incident signal, apply signal conditioning within each element, such as phase or time delay, and then re-radiate incident signals in a new direction via beamforming. Intelligent reflecting surfaces (IRS) typically use passive tunable reflecting elements [1], whilst scalable routers use a full active transmit and receive chain in each receive and transmit pair in the array (called a branch) [2]. While the simplicity, linearity, and low power consumption of IRS are appealing, the active components in scalable routers offer several capabilities that have not been shown in IRS, such as gain and true time delay. Notably, true time delay is required to maintain data coherence for arrays that are comparable in size to the data bandwidth. Furthermore, frequency-division multiplexed (FDM) users require independent re-routing control over frequency channels, which has not been shown in IRS or scalable routers until now. This work presents a scalable router at 28 GHz, demonstrating for the first time 3 independently and simultaneously steered FDM receive/transmit channel pairs each with true time delay, enabling array scalability with a total measured data rate of 625 Mb/s, as well as frequency and spatial multiplexing for robust multiple-user access. This capability is enabled by a novel dual function N-path filter architecture within each frequency channel. These fully passive N-path filters provide separate time and phase delay control and inductorless higher order filtering, with tunable center frequency and bandwidth.

II. SYSTEM IMPLEMENTATION

The system architecture of the presented integrated circuit is shown in Fig. 1. The received signal to be re-directed is first amplified by an LNA, and then is down-converted by a...
Fig. 2. Baseband architecture that performs filtering, phase shifting, and true time delay with two different N-path filters.

28 GHz LO signal. The down-converted signal is processed by 3 separate baseband channels, which filter the signal by frequency and provide programmable amplitude and timing control. The outputs of each channel are summed together and then up-converted to 28 GHz, where an IQ summer, driver, and power amplifier (PA) complete the output path. The chip includes two separate branches which share LO generation and reference distribution circuitry. The LO generation circuitry uses a 1.75 GHz reference to generate 28 GHz IQ LO signals and 3.5 GHz IQ signals which are used in the baseband circuitry. Notably, since up- and down-conversion are performed using the same LO, multiple integrated circuits do not need to share a timing reference to perform beamforming and can be physically detached from each other. Differential I and Q signals at 3.5 GHz are tapped from the LO generation circuitry and are used to feed vector sum phase rotators which provide tunable clock signals to the baseband N-path filters.

To independently and simultaneously steer multiple receive and transmit beams over a large/spatially separated array aperture, both wideband phase and true time delay control are required, as well as channel discrimination in the frequency domain for independent signal conditioning/FDM. The design of the baseband chain should prioritize multi-function, reconfigurable stages and a passive implementation that is amenable to CMOS scaling. In this work, a baseband architecture that uses N-path filters with a combination of both discrete-time (DT) and continuous-time (CT) filter kernels is used to meet the above requirements and is shown in Fig. 2.

It has been shown in [7] that a two-port N-path filter with delayed input and output sampling clocks can behave as a BPF with embedded narrowband phase shifting when the CT-LPF kernel is operating in the averaging mode. The phase shift is, however, a narrowband approximation of a time-delay, and in the presence of wide channel bandwidths does not provide the independent phase and group delay control that multi-channel scalable routers require. To alleviate this issue, we consider the generalized N-path filter system, as shown in Fig. 3. It can be shown that if the signal is bandlimited, a time-invariant impulse response for the system can be derived. The system transfer function can be further simplified if the lowpass filter kernel is also bandlimited, and the resulting frequency response, \( F^0(j\omega) \) in Fig. 3, reveals a frequency-independent phase shift that is dependent on the delay between the input and output modulating functions, \( p(t) \) and \( q(t) \). If the input and output modulators are implemented as series switches, the filter kernel must be isolated so that \( p(t) \) and \( q(t) \) modulate the input/output signal as modeled in the transfer function analysis— otherwise analytical techniques that consider the port impedances of \( h(t) \) must be used [7]. The conditions required for the wideband phase shift— that the filter kernel is isolated and sufficiently bandlimited, are intuitively satisfying. The input modulation acts as a down-conversion mixer, and the bandlimited filter kernel suppresses all but the harmonic of interest. The subsequent output modulation acts as an up-conversion mixer with LO phase shifting, which provides a wideband phase shift to the up-converted signal.

The requirement for filter kernel isolation necessitates the use of unilateral elements. To accomplish this without resorting to active elements, we note that the charge transfer action in a switched capacitor network is non-reciprocal due to the
Fig. 4. The 3-channel response, individual channel response and channel 2 phase and time delay control are shown for a single branch. The two N-path filters decouple phase and time delay control, since the DT-kernel filter group delay does not vary as the phase code is swept, in contrast to an equivalent CT-kernel filter. Channel 2 phase sweep isolation is also shown.

staggered switch phases. The subsequent equivalent model is thus a unilateral resistor, and can be used within the N-path kernel to create high order filters with the necessary isolation.

To achieve passive, high-order, reconfigurable bandpass filtering with embedded wideband phase shifting, a switched-capacitor LPF is used as the DT-LPF kernel. A global feedback is applied around a cascade of real poles via the use of the differential paths [8]. To allow for higher than second order filtering with no peaking, the implemented DT-LPF reduces the feedback factor via charge sharing action in capacitor $C_F$. The implemented third-order filter has close to Butterworth roll-off with no passband peaking. The DT-LPF kernel is placed inside a 4-path N-path filter with differential sampling to eliminate the even harmonic response. The filter center frequencies are at 218.75 MHz and 437.5 MHz, and were designed to have 80 MHz of bandwidth. Due to the DT-LPF kernel, both the center frequency and channel bandwidth are, in principle, independently tunable by only varying the clock frequency— in this work, however, all clocks are generated from the same source with fixed divider ratios. The true time delay unit consists of a CT-kernel N-path filter operating in the sampling regime. The sinc magnitude response (ideal sampling) of the time delay unit causes an equilizable roll-off in the third channel, as seen in Fig. 4.

The lowpass baseband channel is frequency discriminated by a two-stage cascade of the DT-LPF kernels. Its wideband phase steering is controlled by LO phase shifting at the 28 GHz RX mixer. VGAs with 10 dB of programmable gain are placed prior to each DT-kernel N-path filter and after each true time delay unit. An anti-aliasing lowpass buffer, implemented as a Butterworth source follower biquad, is placed between the DT-kernel N-path filter and the true time delay unit to filter the harmonic responses generated by the DT-kernel N-path filter.

To verify the proposed dual function N-path filter architecture, Fig. 4 shows a coarse phase sweep of the middle channel and its effect on the phase of adjacent channels— the channel isolation is >15 dB. The effect of the DT-kernel N-path filter’s phase sweep on the group delay is shown and contrasted with the expected variation for the CT-kernel equivalent. The minimal group delay change supports the proposed architecture, decoupling phase and group delay variation. A coarse sweep of the tunable group delay of the CT-kernel N-path filter also agrees with theory.

III. ROUTER ARRAY MEASUREMENTS

A two-chip, four-branch radiative scalable router array was constructed. The circuit board, measurement set up, and beam-steering demonstration measurements are depicted in Fig. 5. Patch antennas are placed at a pitch of $3\lambda$, with the transmit and receive antennas orthogonally polarized. A source

Fig. 5. Scalable router array demonstrating simultaneous, independent steering of three beams. Two separate patch antenna circuit boards are used to form the 4-branch router which is excited by a VNA. Grating lobes for channels 2 and 3 have been removed in the independent steering for readability.
antenna illuminates the scalable router, which re-radiates the signal towards a probe antenna mounted on a mechanical linear scanning track. The three beams are simultaneously and independently steered: shown in Fig. 5 steered to broadside and steered to offsets of 12 degrees. The two chips do not share a common frequency/phase reference but still perform coherent far-field combining. This capability, vital for router scalability, is granted by the system architecture which uses the same LO for down-conversion and up-conversion. A data transmission demonstration is shown in Fig. 6. A M8199A AWG is used to generate a single aggregate data stream that contains independent 32-QAM data on 3 channels centered at 28.3, 28.1, and 27.9 GHz, with respective data rates of 250 Mb/s, 275 Mb/s, and 100 Mb/s. The aggregate data stream is connected to a transmit antenna that illuminates the scalable router array. The individual data streams are simultaneously and independently steered by the scalable router. A N9030B PXA is connected to a receive antenna and used to receive the individual data streams, with the receive antenna position varied to coincide with the different beam-steered directions corresponding to each data stream. Due to measurement limitations, the data rate of the third channel is limited by multipath/reflection effects, and can be increased by varying the multipath environment at the expense of the other channels.

IV. CONCLUSION

The presented integrated circuit uses a novel dual function N-path filter architecture to enable simultaneous, and independently controlled, frequency and spatially multiplexed beams within a scalable router. A 2-chip, 4-branch, scalable router at 28 GHz operating without a shared timing reference is used to perform far-field beamforming and beam-steering and demonstrates wireless data transmission of 600+ Mb/s.

REFERENCES


