Monolithic Optical Clock Distribution in Bulk CMOS Using I-Beam Waveguides

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Abstract

Optical clock distribution is presented for the first time in an unmodified bulk CMOS chip. An H-tree distributes the signal using I-beam photonic waveguides operating at 780 nm, and avalanche photodiodes and transimpedance amplifiers bring the signal back to the electronic domain. All components are monolithically integrated on a 180nm bulk CMOS chip. The I-beam waveguides are also demonstrated in 22nm FDSOI CMOS technology without process modifications or design rule violations, making it the most advanced commercial process to monolithically demonstrate photonic waveguiding.

Keywords: clock distribution, photonics, photonic waveguide, monolithic integration, optical interconnect, H-tree, CMOS

Introduction

Interconnect scaling poses a substantial constraint on the size, complexity, and speed of VLSI chips [1,2]. Optical clock distribution networks, in which the signal is modulated onto an optical carrier and distributed via photonic waveguides, have been proposed as an evolution of electronic clock distribution networks for VLSI [3]. Optical distribution may mitigate many of the drawbacks of metal interconnects, such as high power consumption, crosstalk, and sensitivity to PVT.

Subtractive photonics currently offers the lowest loss photonic waveguide in unmodified bulk CMOS technology, making it a promising option for the monolithic integration of optical clock distribution [4]. Subtractive photonic waveguides are formed through the wet etching of metal interconnects, leaving behind freestanding intermetal-dielectric (IMD) structures that guide light using the refractive index contrast of the dielectric-air interface. However, the waveguide structures demonstrated in [4] are unsuitable for optical clock distribution due to multi-mode operation and design rule violations leading to mechanical fragility.

Building on the subtractive photonics platform, this paper describes an optical clock distribution network with electronics and photonics implemented in the same unmodified 180nm bulk CMOS chip. To achieve robust performance over PVT, a low-loss, single-mode "I-beam" waveguide and distribution network is presented. To demonstrate the viability of the distribution technique in more advanced nodes, optical waveguiding in 22nm FDSOI CMOS technology is reported.

System Design

Fig. 1 illustrates the system-level design of the optical clock distribution chip, employing the proposed I-beam waveguide for all photonic components. An optical carrier is modulated at the clock frequency, edge-coupled into the chip, and distributed using photonic Y-junctions that form an H-tree. Several branches of the tree terminate in a waveguide-to-photodiode coupler that directs the light into an avalanche photodiode (APD). Transimpedance amplifiers (TIA) amplify the signal further in two of the branches, while the other branches are used for characterizing the photonics and observing an extended H-tree.

The I-beam waveguide consists of two dielectric slabs providing mechanical support and a dielectric core ensuring lateral mode confinement after etching (Fig. 2). Subtractive photonic rib waveguides and waveguides composed of fewer layers frequently experience shear failure and buckling, respectively, while the I-beam shape mitigates both failure mechanisms [5]. The dimensions are chosen to ensure single-mode operation at the operating wavelength of 780 nm, which is critical to ensuring the well-controlled behavior of every photonic component (Fig. 3).

Implementation

The I-beam waveguide is designed to have a small footprint, fitting within a 10 μm street in the interconnect layers of a 180nm bulk CMOS process. Only a subset of the interconnect layers are consumed, leaving the area available for devices and routing. Y-junctions use the same layers as the nominal waveguide, and their curvature follows an Euler curve with a maximum radius of 90 μm to balance loss and footprint, although bends down to 10 μm are possible at the cost of slightly higher insertion loss (Fig. 4). The waveguide-to-photodiode coupler is implemented as a multilayer structure to maximize the amount of light directed into the silicon APD (Fig. 5). FDTD simulations yield coupling losses of 0.36 and 1.87 dB for the Y-junction and waveguide-to-photodiode coupler, respectively.

The N+/P-well junction of the photodiode is avalanche biased to improve responsivity while adding minimal excess multiplication noise compared to germanium photodiodes, and the deep N-well is used to block slower diffusion currents [6]. The N+ terminal of the APD is connected to a single-ended TIA composed of a regulated-cascode transimpedance stage and a Cherry-Hooper amplification stage (Fig. 6). A class AB output buffer is also included in the TIA to drive the 50 Ω input impedance of measurement equipment.

As an indication of its feasibility in more advanced processes, the waveguide is implemented using the IMD of a 22nm FDSOI CMOS chip (Fig. 7). In SOI processes, waveguides have previously been demonstrated using the silicon immediately above the buried-oxide (BOX) layer, but that silicon is too small to support a mode beyond the 32nm node [7]. Therefore, the presented waveguide in 22nm FDSOI CMOS technology demonstrates photonic waveguiding in the most advanced CMOS process to date without process modifications.

Measurement Results

The clock distribution chip is fabricated in a 180nm bulk CMOS process, and the chip is etched in Aluminum Etch Type A at 80°C for 8 hours to expose the photonic circuits [4]. All optoelectronic measurements are performed with intensity-modulated light at 780 nm that is coupled into the chip using lensed fiber with a 2 μm spot size. The waveguide loss is too low to be accurately measured.

The APD bandwidth and responsivity are plotted in Fig. 8. Measuring the APD-only branch gives an excess loss of 4.4 dB through the photonic chain, which includes the edge-coupler to the photodiode-coupler, with an additional 6 dB of loss inherent to the 1-to-4 splitting of the H-tree. The response of the full system, including both photonics and electronics, is plotted in Fig. 9. The phase noise is plotted in Fig. 10, with an RMS jitter of 841 fs when integrated over a 1 MHz bandwidth for a 1 GHz carrier. Each TIA consumes 13 mW from a 1.8 V supply, each APD consumes <0.5 mW, and 3 mW or less of average optical power is used for all measurements. The chip is 1.5 by 1.5 mm^2, and a die photo can be seen in Fig. 11.

Conclusion

This work successfully demonstrates optical clock distribution in a foundry-fabricated 180nm bulk CMOS process while also showing that the proposed waveguides can be made without design rule violations in more advanced processes.

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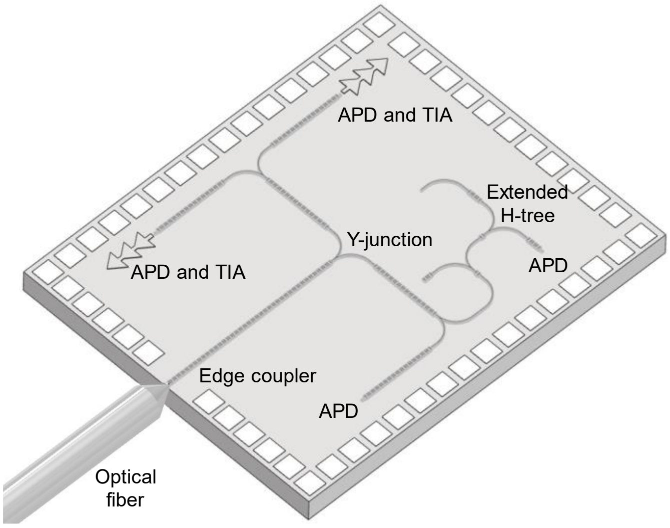

Fig. 1. Diagram of the optical clock distribution chip with key components labelled.

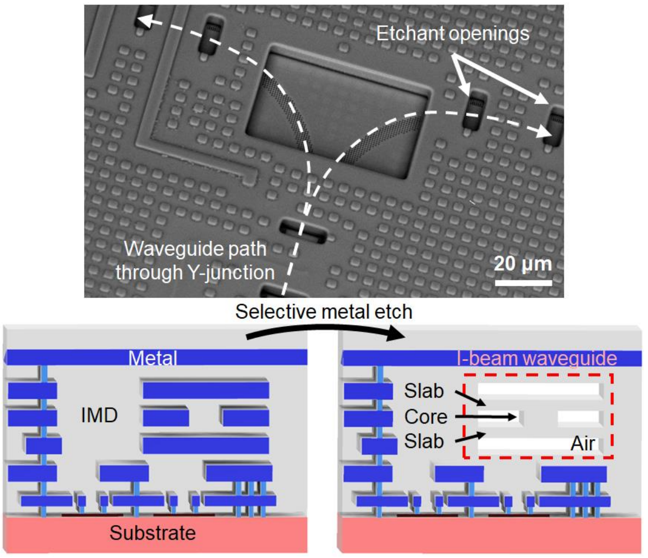

Fig. 2. SEM of the surface of the chip after etching, and illustration of the waveguide cross-section (etchant path not shown).

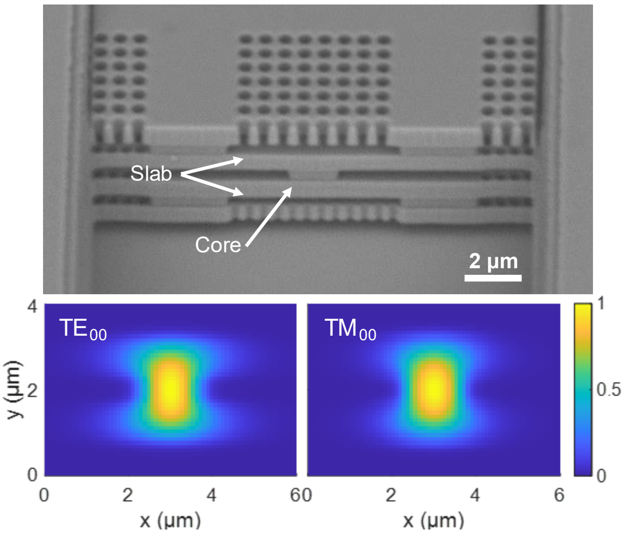

Fig. 3. SEM of the I-beam waveguide cross-section and confined modes at a wavelength of 780 nm.

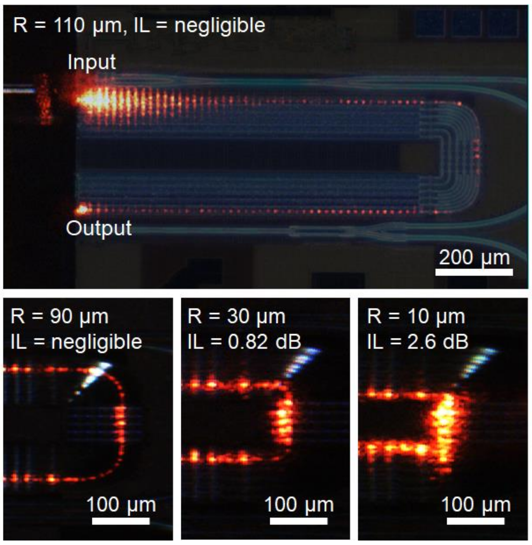

Fig. 4. Micrographs of light scattering from the bend loss test structures with simulated insertion loss at 780 nm annotated. A short straight section connects two 90° bends for various radii.

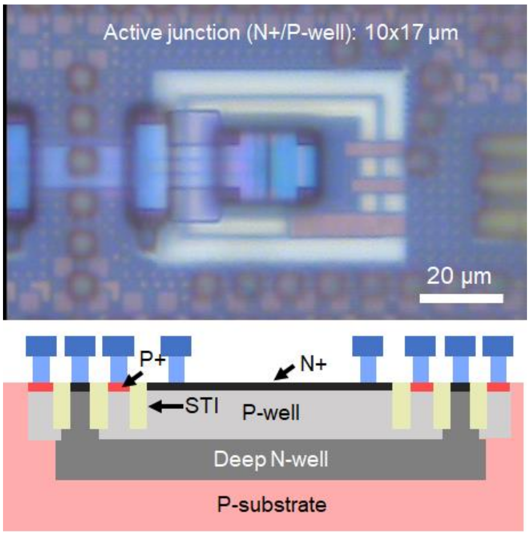

Fig. 5. Micrograph of the APD and waveguide-to-photodiode coupler, with the waveguide entering from the left and electronic routing of the photodiode to the TIA to the right.

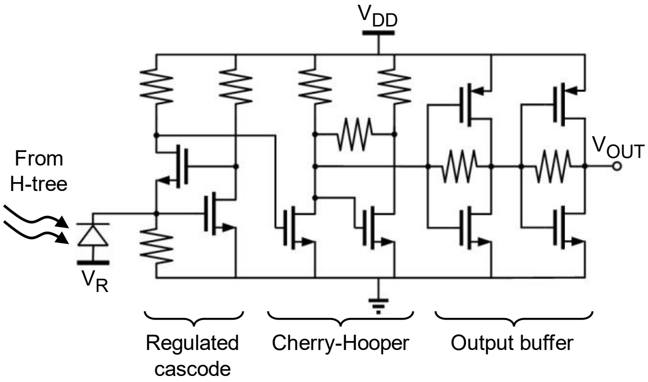

Fig. 6. Schematic of the transimpedance amplifier used in the clock distribution chip, which consumes 13 mW from a 1.8 V supply.

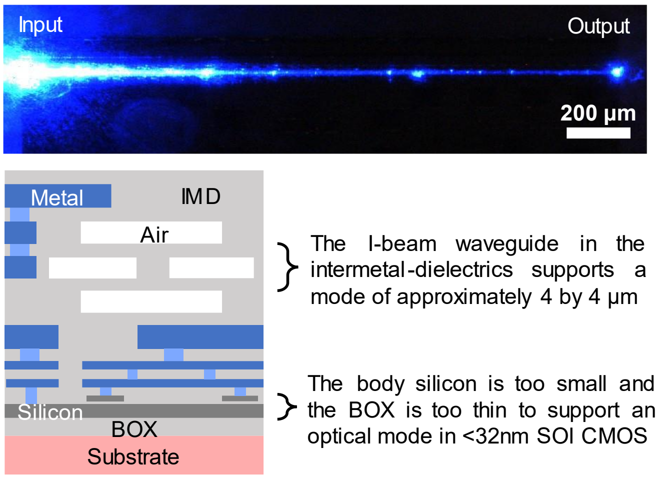

Fig. 7. Scattering from the 22nm SOI CMOS waveguide when blue light is coupled in for visualization. Its upper-bound loss is 14.4 dB/cm based on insertion loss measurements.

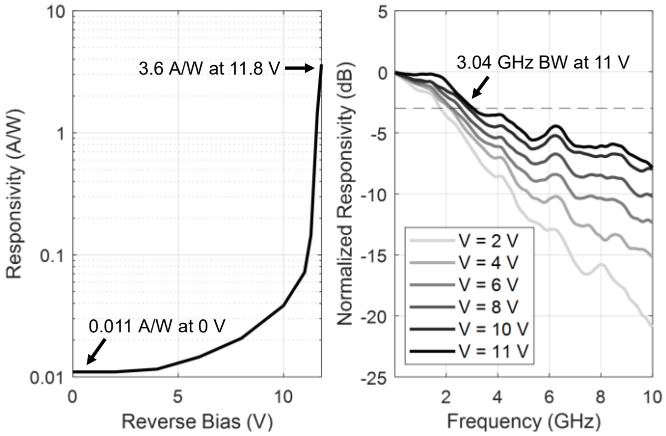

Fig. 8. Responsivity and normalized frequency response for the APD versus reverse bias.

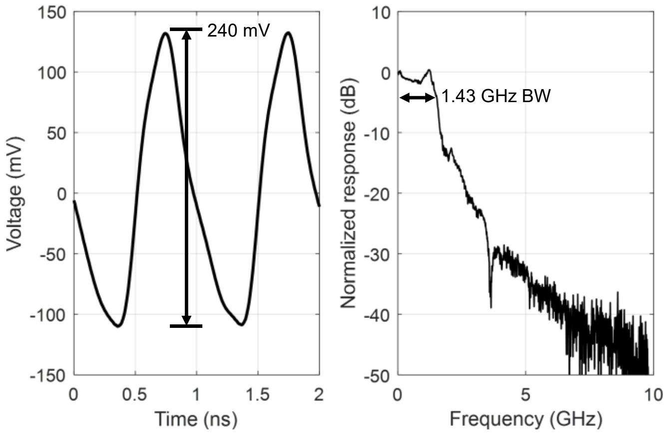

Fig. 9. System transient waveform and normalized frequency response. The APD reverse bias is set to 11 V, and the transient waveform is measured with 6 dBm of optical power.

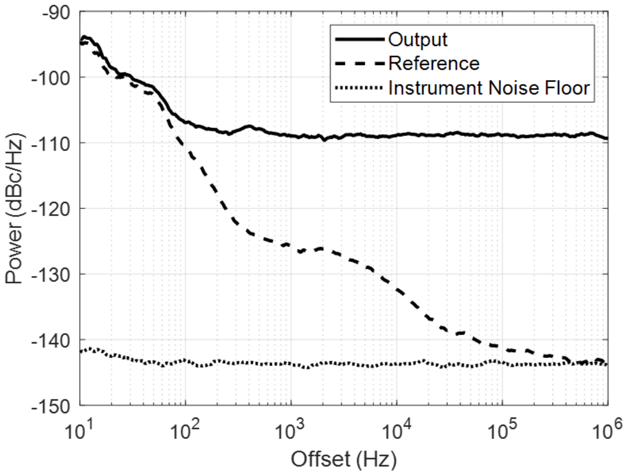

Fig. 10. Phase noise at the output of a TIA for a 1 GHz carrier and APD reverse bias of 11 V. 4 dBm of optical power is used.

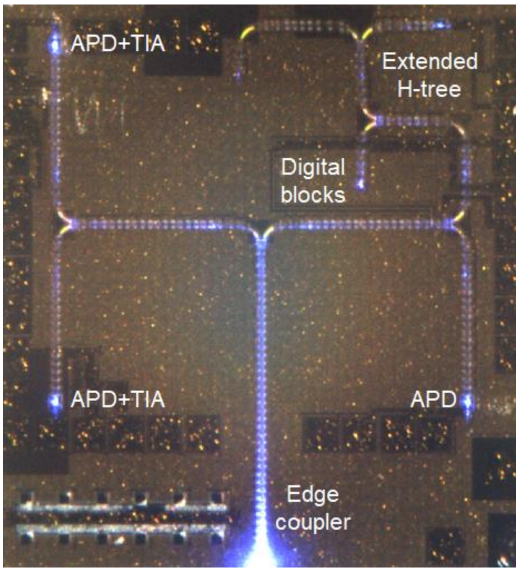

Fig. 11. Die photo of the 180nm bulk CMOS chip with blue light coupled in for visualization.

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